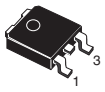
STD40NF10

N-channel 100 V, 0.025 Ω, 50 A DPAK low gate charge STripFET™ II Power MOSFET

Features

Order code	V_{DSS}	$R_{DS(on)}$ max.	I_D
STD40NF10	100 V	< 0.028 Ω	50 A

- Exceptional dv/dt capability
- Low gate charge
- 100% avalanche tested



DPAK

Application

Switching applications

Description

This N-channel 100 V Power MOSFET is the latest development of STMicroelectronics unique single feature size strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps allowing remarkable manufacturing reproducibility.

Figure 1. Internal schematic diagram

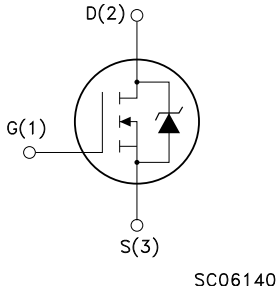


Table 1. Device summary

Order code	Marking	Package	Packaging
STD40NF10	D40NF10	DPAK	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (v_{gs} = 0)	100	V
V_{GS}	Gate- source voltage	±20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	50	A
I_D	Drain current (continuous) at T_C = 100 °C	35	A
I_{DM} (2)	Drain current (pulsed)	200	A
P_{TOT}	Total dissipation at T_C = 25 °C	125	W
	Derating factor	0.83	W/°C
dv/dt(3)	Peak diode recovery voltage slope	27	V/ns
E_{AS} (4)	Single pulse avalanche energy	385	mJ
T_{stg}	Storage temperature	- 55 to 175	°C
T_j	Max. operating junction temperature		

1. Limited by wire bonding
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 50$ A, di/dt ≤ 600 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.
4. Starting T_j= 25 °C, I_D= 50 A, V_{DD} = 25 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.2	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient max	62.5	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 250 µA, V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS}=Max rating,T_C=125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 25 A		0.025	0.028	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D= 28 A		22		S
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		2180		pF
C_{oss}	Output capacitance			298		pF
C_{rss}	Reverse transfer capacitance			83.7		pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 40 A, V_{GS} = 10 V *(see Figure 15)*		46.5	62	nC
Q_{gs}	Gate-source charge			13.3		nC
Q_{gd}	Gate-drain charge			17.5	22.5	nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 25 A R_G = 4.7 Ω V_{GS} = 10 V *(see Figure 14)*		21		ns
t_r	Rise time			46		ns
$t_{d(off)}$	Turn-off-delay time			54		ns
t_f	Fall time			13		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current				80	A
I_{SDM} (1)	Source-drain current (pulsed)				320	A
V_{SD} (2)	Forward on voltage	I_{SD} = 50 A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 50 A, V_{DD} = 25 V di/dt = 100 A/µs, T_j = 150 °C *(see Figure 16)*		80 250 6.4		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

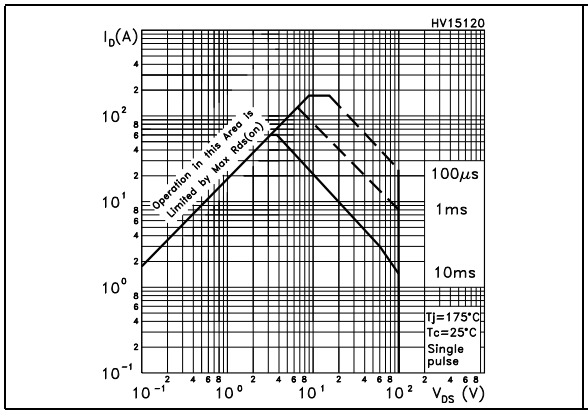


Figure 3. Thermal impedance

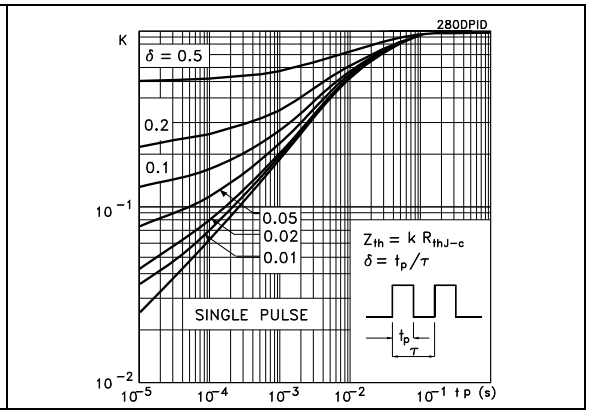


Figure 4. Output characteristics

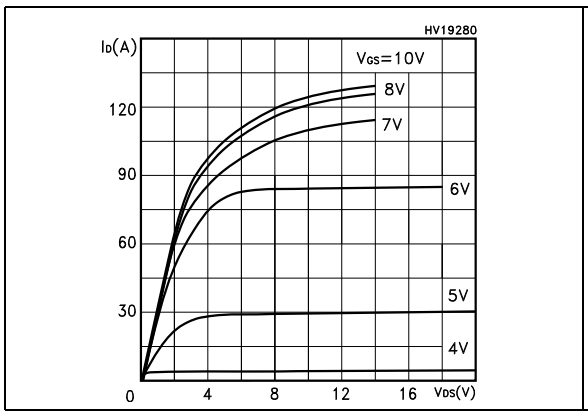


Figure 5. Transfer characteristics

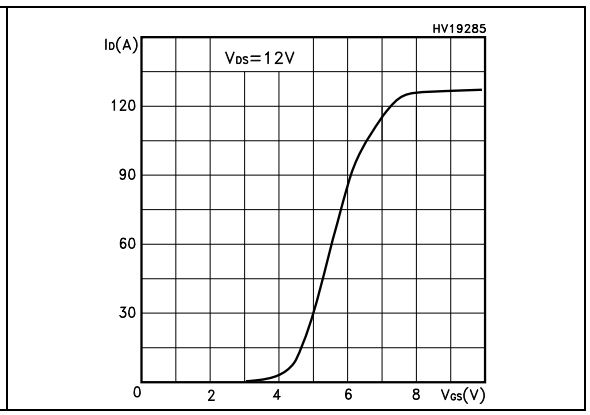


Figure 6. Transconductance

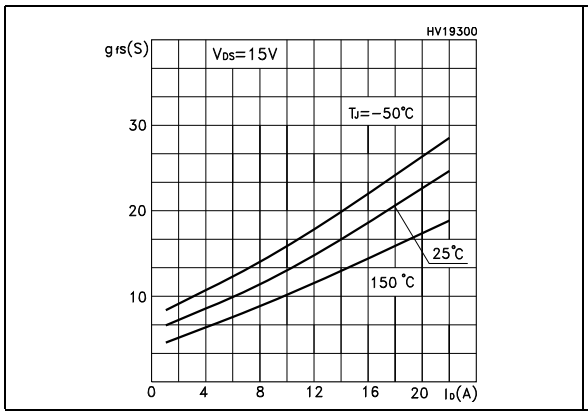


Figure 7. Static drain-source on resistance

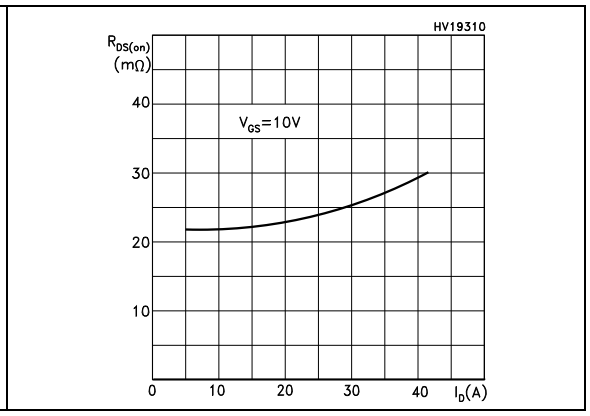


Figure 8. Gate charge vs. gate-source voltage

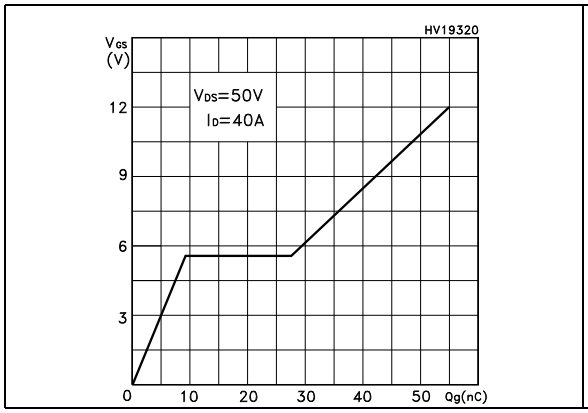


Figure 9. Capacitance variations

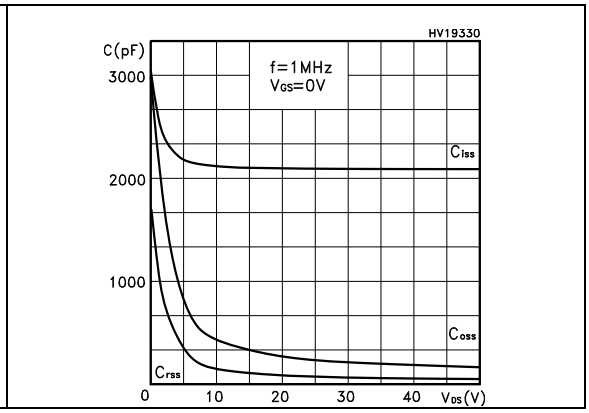


Figure 10. Normalized gate threshold voltage vs. temperature

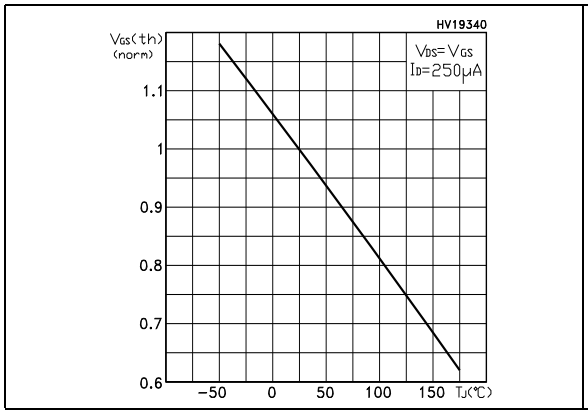


Figure 11. Normalized on resistance vs. temperature

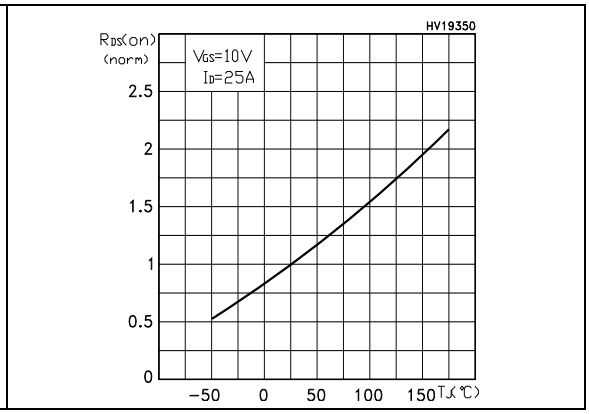


Figure 12. Source-drain diode forward characteristics

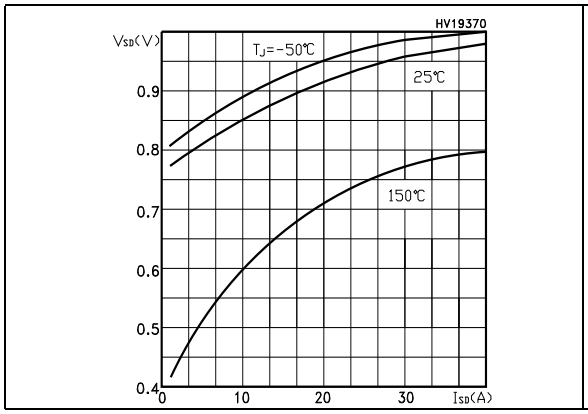
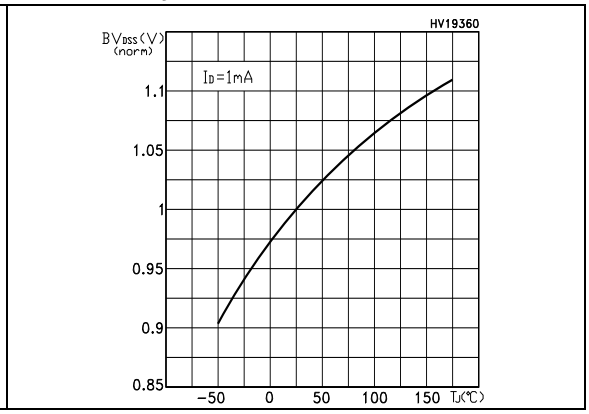


Figure 13. Normalized breakdown voltage vs. tj



3 Test circuit

Figure 14. Switching times test circuit for resistive load

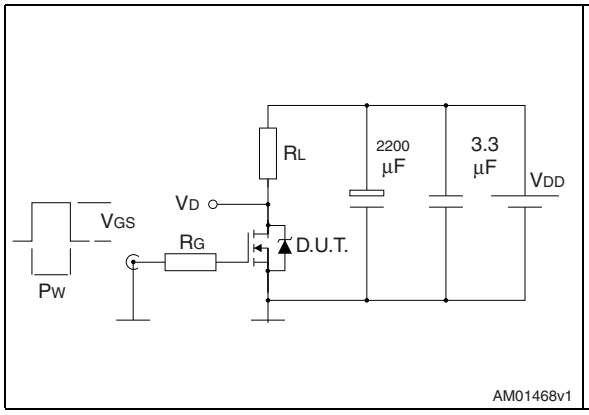


Figure 15. Gate charge test circuit

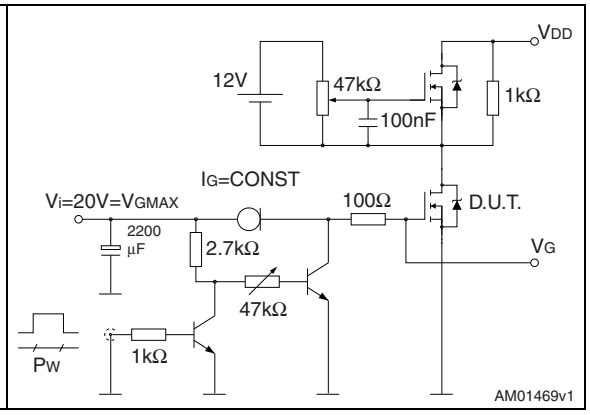


Figure 16. Test circuit for inductive load switching and diode recovery times

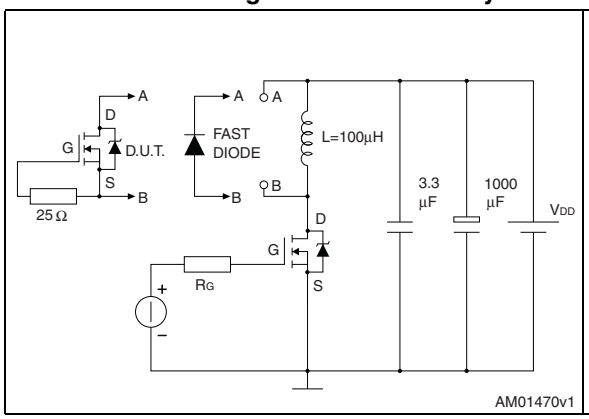


Figure 17. Unclamped Inductive load test circuit

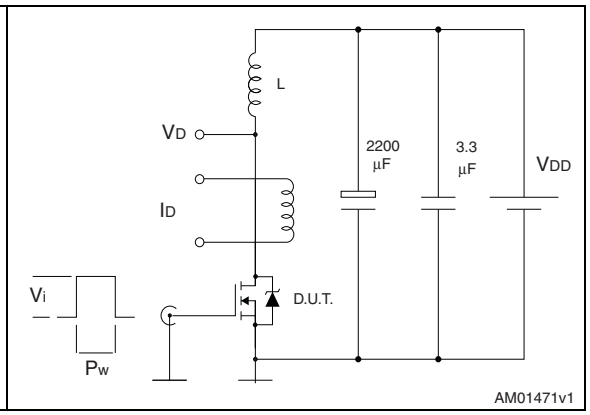


Figure 18. Unclamped inductive waveform

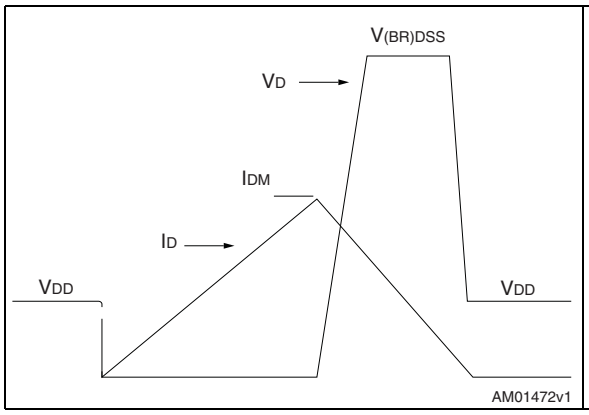
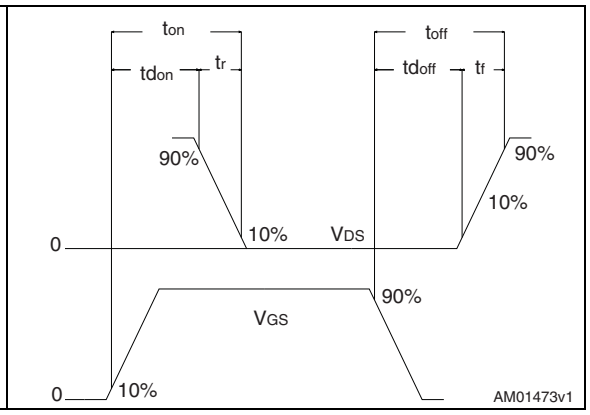


Figure 19. Switching time waveform

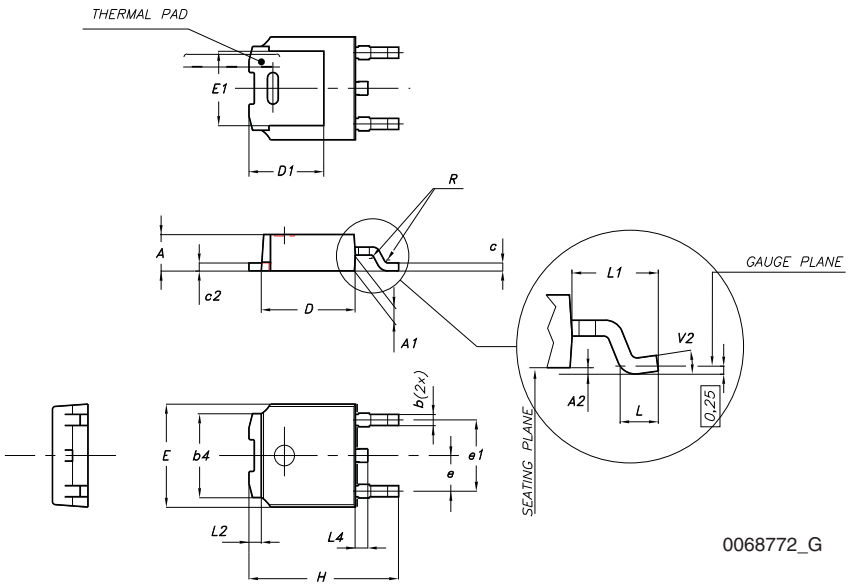


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

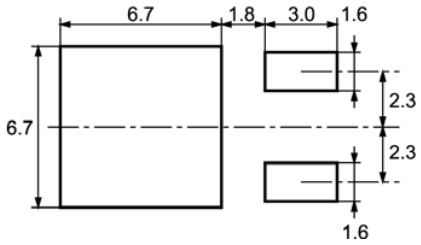
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °



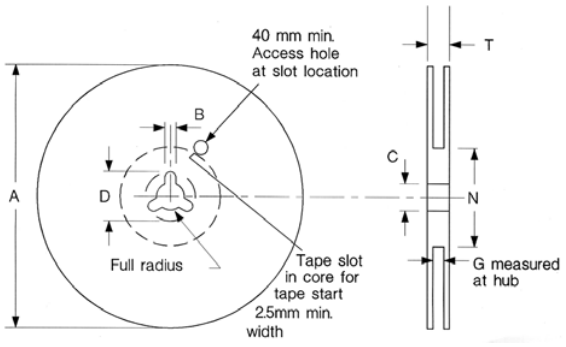
5 Packaging mechanical data

DPAK FOOTPRINT



All dimensions are in millimeters

TAPE AND REEL SHIPMENT



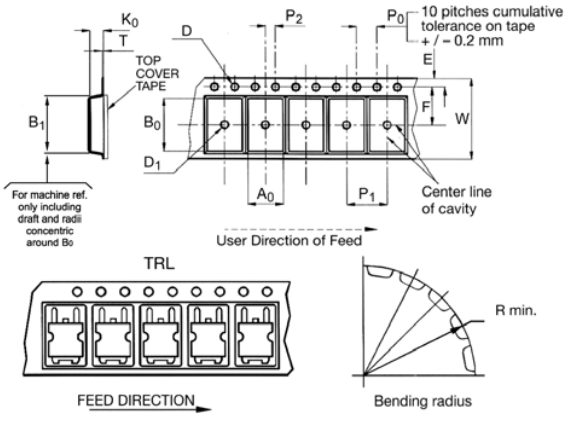
REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641



6 Revision history

Table 8. Document revision history

Date	Revision	Changes
19-Nov-2010	1	First issue.

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