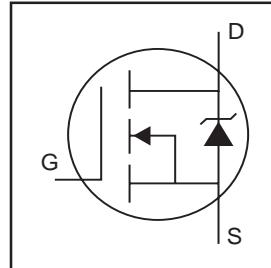


# International **IR** Rectifier

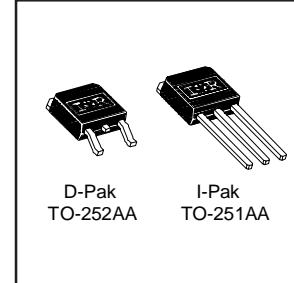
PD - 95062A

## **IRLR2705PbF** **IRLU2705PbF**

HEXFET® Power MOSFET



$V_{DSS} = 55V$   
 $R_{DS(on)} = 0.040\Omega$   
 $I_D = 28A^{(5)}$



- Logic-Level Gate Drive
- Ultra Low On-Resistance
- Surface Mount (IRLR2705)
- Straight Lead (IRLU2705)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

### Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	28	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	20	
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	110	
$P_D @ T_C = 25^\circ C$	Power Dissipation	68	W
	Linear Derating Factor	0.45	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 16	V
$E_{AS}$	Single Pulse Avalanche Energy <sup>②</sup>	110	mJ
$I_{AR}$	Avalanche Current <sup>①</sup>	16	A
$E_{AR}$	Repetitive Avalanche Energy <sup>①</sup>	6.8	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ <sup>③</sup>	5.0	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

### Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{0JC}$	Junction-to-Case	—	2.2	°C/W
$R_{0JA}$	Case-to-Ambient (PCB mount)**	—	50	
$R_{0JA}$	Junction-to-Ambient	—	110	

\*\* When mounted on 1" square PCB (FR-4 or G-10 Material) .

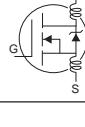
For recommended footprint and soldering techniques refer to application note #AN-994

[www.irf.com](http://www.irf.com)

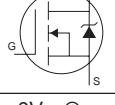
1

1/11/05

Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	—	0.065	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	—	0.040	W	$V_{\text{GS}} = 10\text{V}, I_D = 17\text{A}$ ④
		—	—	0.051		$V_{\text{GS}} = 5.0\text{V}, I_D = 17\text{A}$ ④
		—	—	0.065		$V_{\text{GS}} = 4.0\text{V}, I_D = 14\text{A}$ ④
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$
$g_{\text{fs}}$	Forward Transconductance	11	—	—	S	$V_{\text{DS}} = 25\text{V}, I_D = 16\text{A}$ ⑦
$I_{\text{DSS}}$	Drain-to-Source Leakage Current	—	—	25	$\mu\text{A}$	$V_{\text{DS}} = 55\text{V}, V_{\text{GS}} = 0\text{V}$
		—	—	250		$V_{\text{DS}} = 44\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 150^\circ\text{C}$
$I_{\text{GSS}}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{\text{GS}} = 16\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{\text{GS}} = -16\text{V}$
$Q_g$	Total Gate Charge	—	—	25	nC	$I_D = 16\text{A}$
$Q_{\text{gs}}$	Gate-to-Source Charge	—	—	5.2		$V_{\text{DS}} = 44\text{V}$
$Q_{\text{gd}}$	Gate-to-Drain ("Miller") Charge	—	—	14		$V_{\text{GS}} = 5.0\text{V}, \text{See Fig. 6 and 13}$ ④⑦
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	8.9	—	ns	$V_{\text{DD}} = 28\text{V}$
$t_r$	Rise Time	—	100	—		$I_D = 16\text{A}$
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	21	—		$R_G = 6.5\Omega, V_{\text{GS}} = 5.0\text{V}$
$t_f$	Fall Time	—	29	—		$R_D = 1.8\Omega, \text{See Fig. 10}$ ④⑦
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact ⑥
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{\text{iss}}$	Input Capacitance	—	880	—		$V_{\text{GS}} = 0\text{V}$
$C_{\text{oss}}$	Output Capacitance	—	220	—	pF	$V_{\text{DS}} = 25\text{V}$
$C_{\text{rss}}$	Reverse Transfer Capacitance	—	94	—		$f = 1.0\text{MHz}, \text{See Fig. 5}$ ⑦

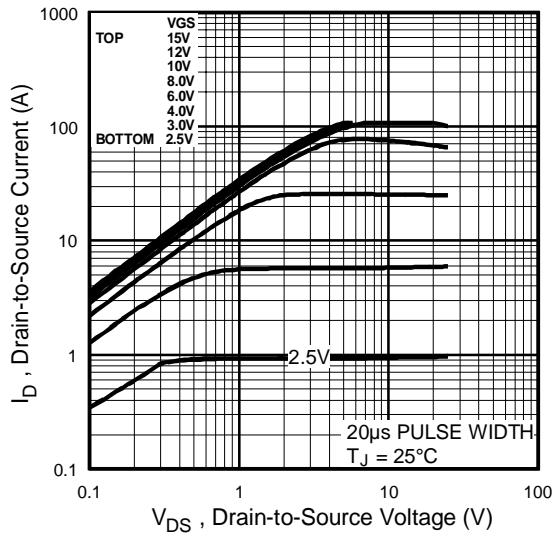
## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	28	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{\text{SM}}$	Pulsed Source Current (Body Diode) ①	—	—	110		
$V_{\text{SD}}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 17\text{A}, V_{\text{GS}} = 0\text{V}$ ④
$t_{\text{rr}}$	Reverse Recovery Time	—	76	110	ns	$T_J = 25^\circ\text{C}, I_F = 16\text{A}$
$Q_{\text{rr}}$	Reverse Recovery Charge	—	190	290	nC	$dI/dt = 100\text{A}/\mu\text{s}$ ④⑦
$t_{\text{on}}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

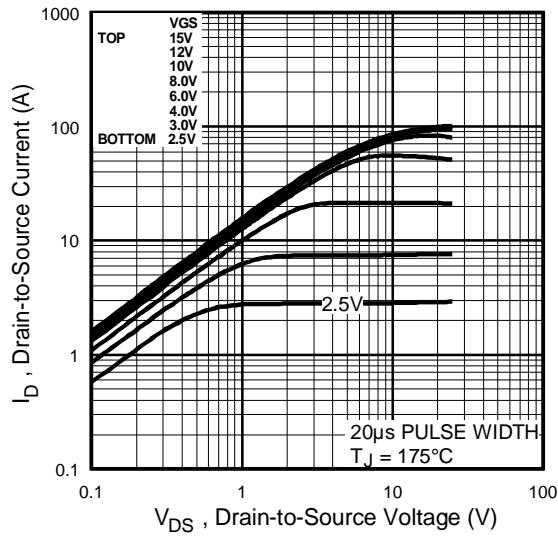
## Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ②  $V_{\text{DD}} = 25\text{V}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 610\mu\text{H}$   
 $R_G = 25\Omega, I_{AS} = 16\text{A}$ . ( See Figure 12 )
- ③  $I_{SD} \leq 16\text{A}$ ,  $dI/dt \leq 270\text{A}/\mu\text{s}$ ,  $V_{\text{DD}} \leq V_{(\text{BR})\text{DSS}}$ ,  
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

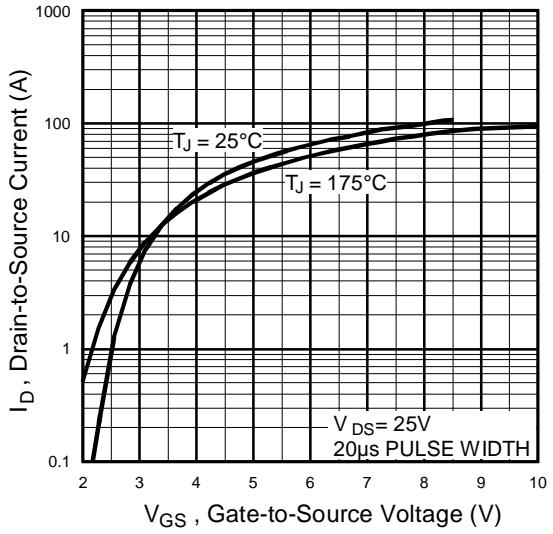
- ⑤ Calculated continuous current based on maximum allowable junction temperature; Package limitation current = 20A.
- ⑥ This is applied for I-PAK,  $L_S$  of D-PAK is measured between lead and center of die contact.
- ⑦ Uses IRLZ34N data and test conditions.



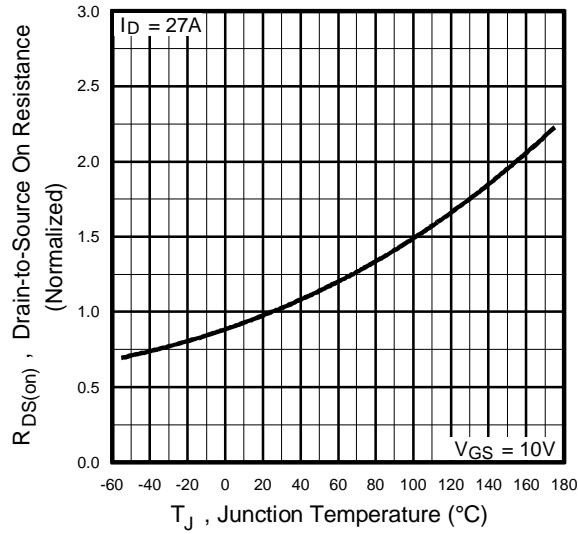
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics



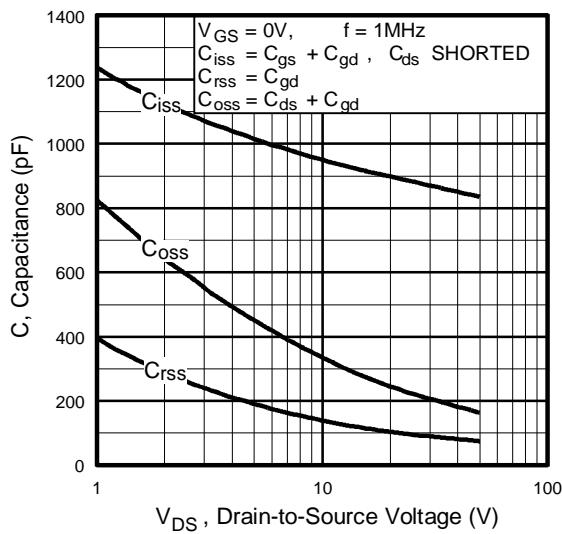
**Fig 3.** Typical Transfer Characteristics



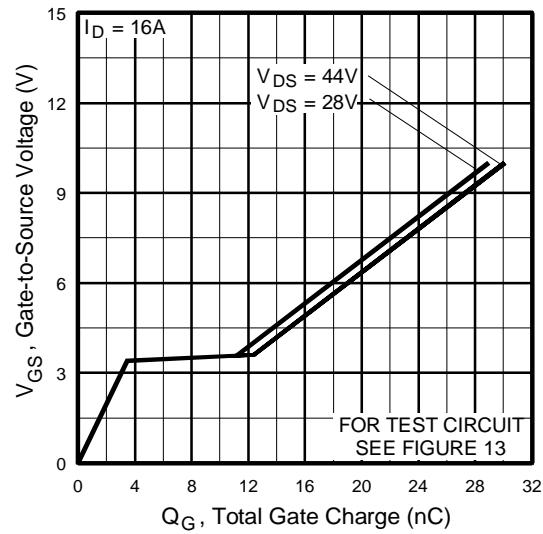
**Fig 4.** Normalized On-Resistance  
Vs. Temperature

# IRLR/U2705PbF

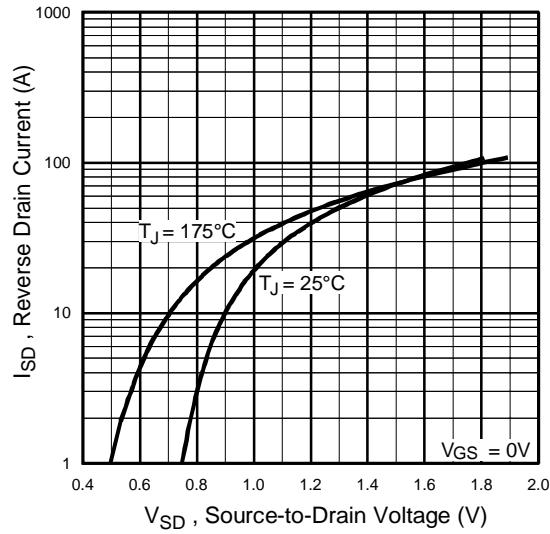
International  
**IR** Rectifier



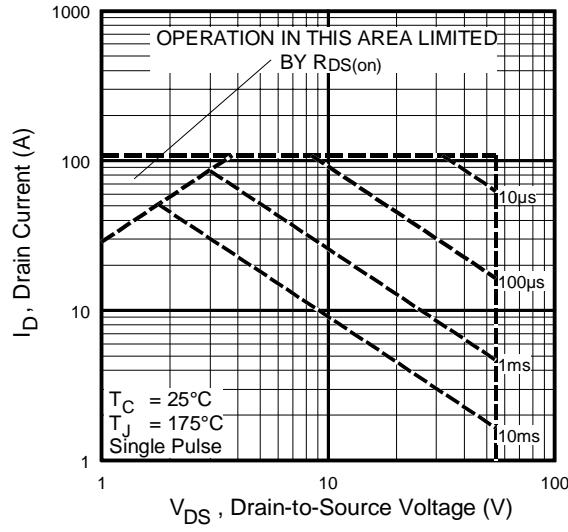
**Fig 5.** Typical Capacitance Vs.  
Drain-to-Source Voltage



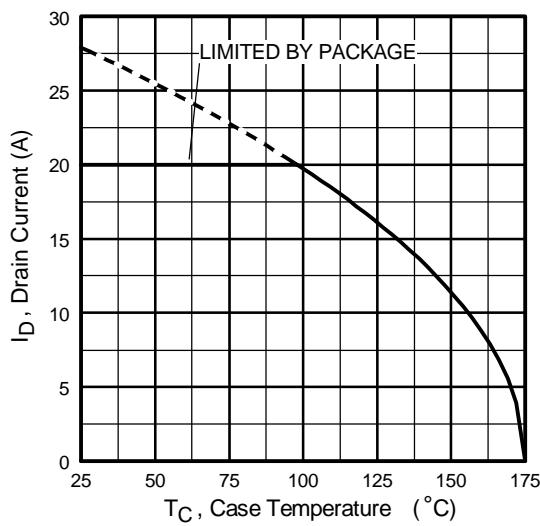
**Fig 6.** Typical Gate Charge Vs.  
Gate-to-Source Voltage



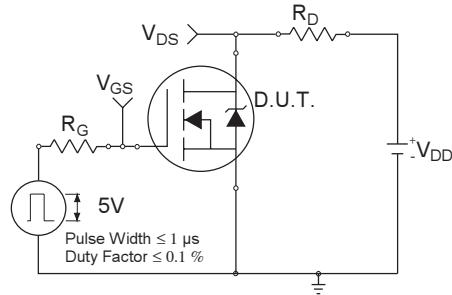
**Fig 7.** Typical Source-Drain Diode  
Forward Voltage



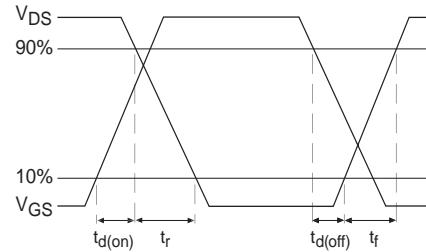
**Fig 8.** Maximum Safe Operating Area



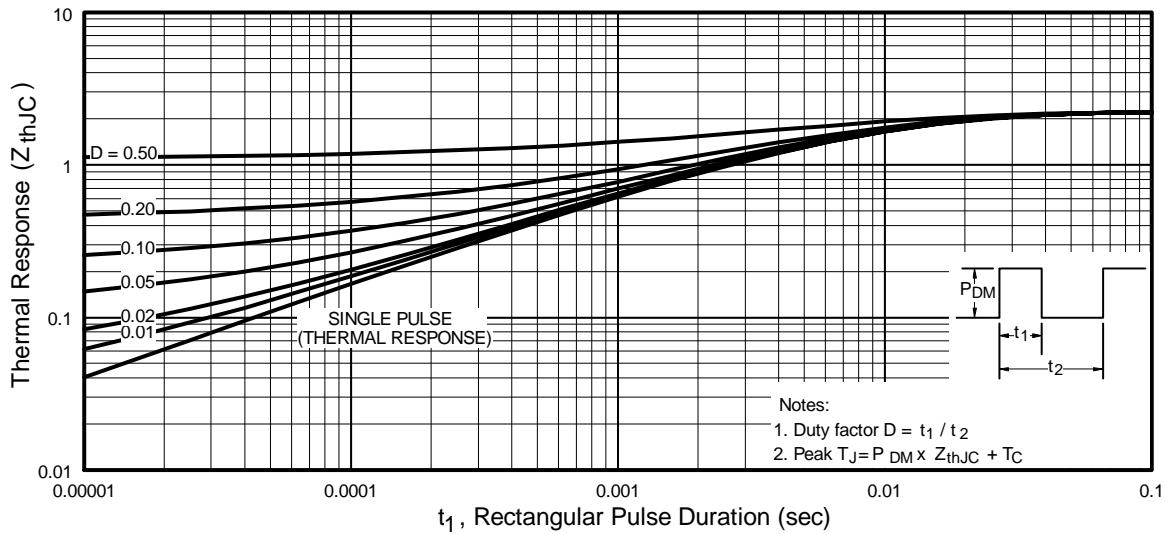
**Fig 9.** Maximum Drain Current Vs.  
Case Temperature



**Fig 10a.** Switching Time Test Circuit



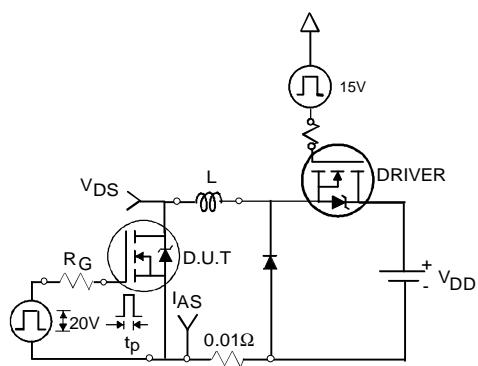
**Fig 10b.** Switching Time Waveforms



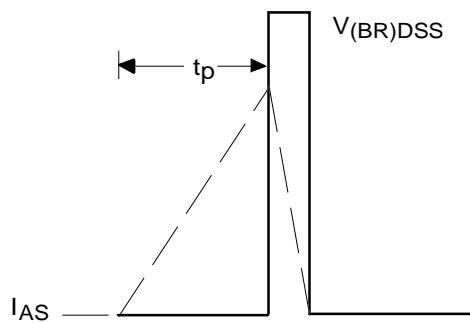
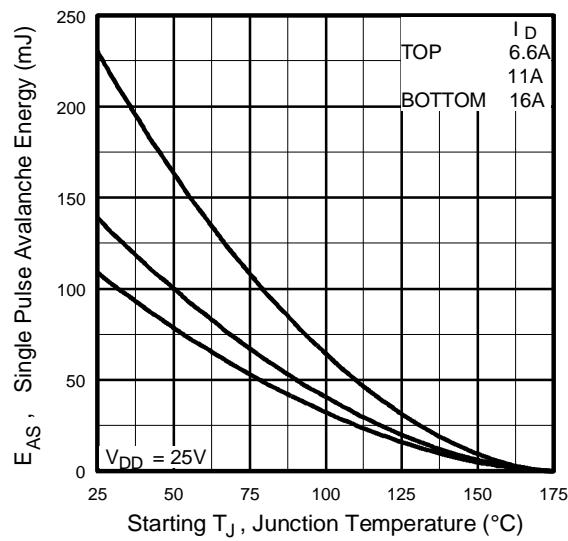
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

# IRLR/U2705PbF

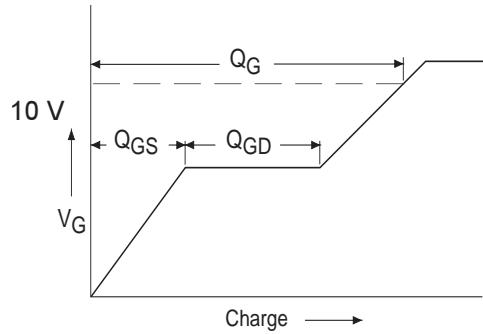
International  
**IR** Rectifier



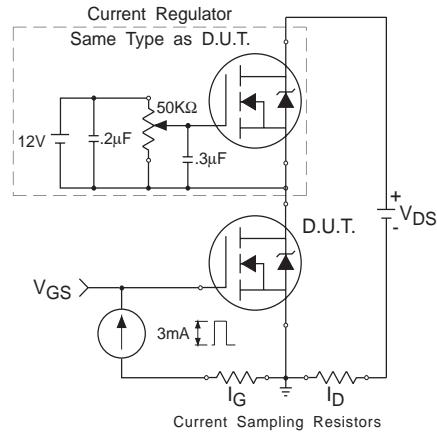
**Fig 12a.** Unclamped Inductive Test Circuit



**Fig 12b.** Unclamped Inductive Waveforms

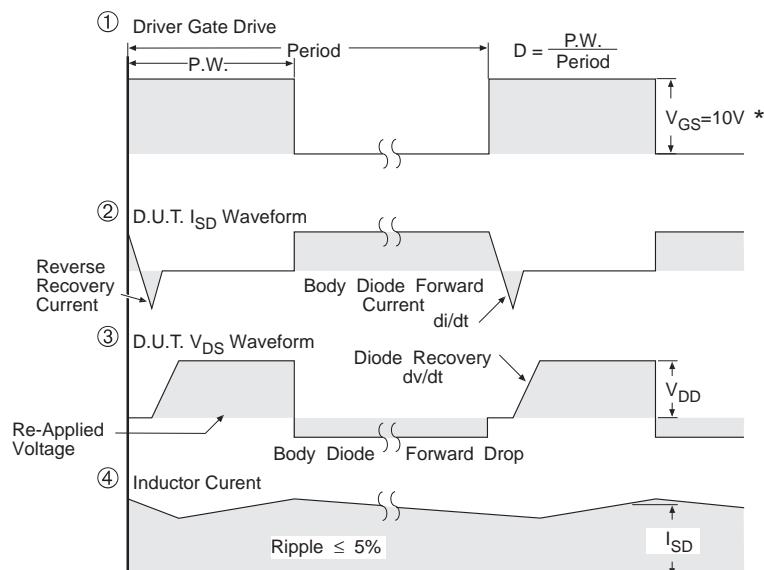
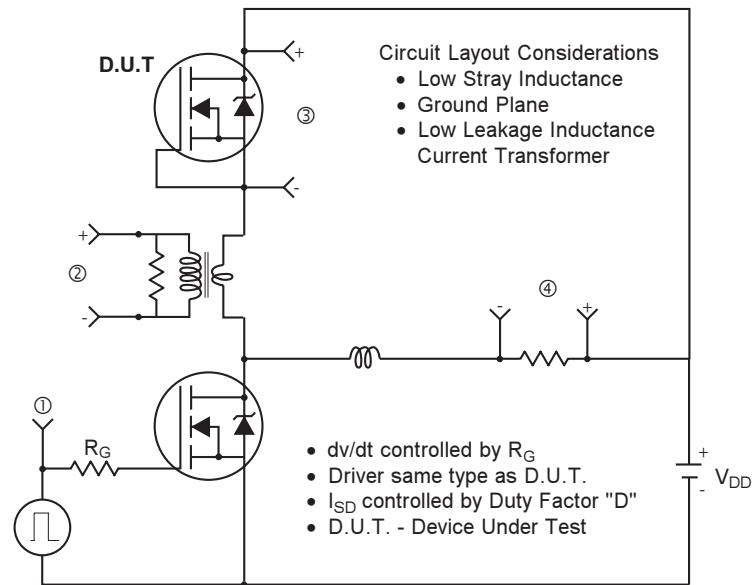


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

### Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

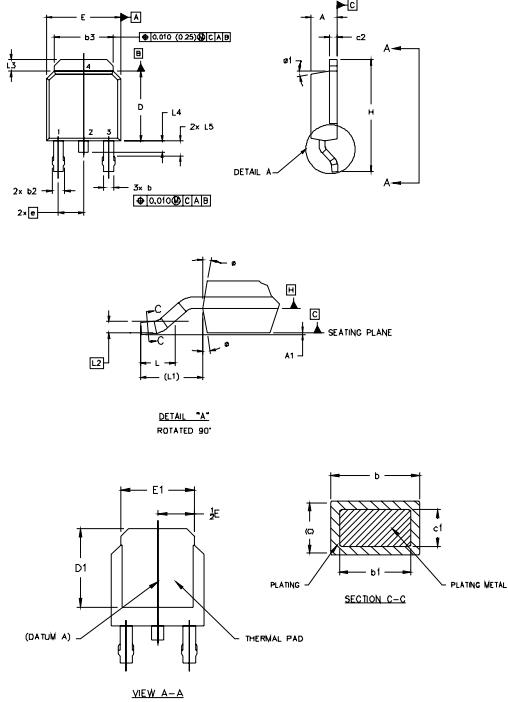
**Fig 14.** For N-Channel HEXFETs

# IRLR/U2705PbF

International  
**IR** Rectifier

## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5M- 1994.
- 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.0 LEAD DIMENSION UNCONTROLLED IN LS.
- 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.254] FROM THE LEAD TIP.
- 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

**LEAD ASSIGNMENTS**

SYMBOL	DIMENSIONS		NOTES
	MILLIMETERS	INCHES	
	MM. MN.	IN. MAX.	
A	2.18	.239	.086 .094
A1		.15	.005
b	.64	.089	.026 .035
b1	.64	.79	.026 .031
b2	.76	1.14	.030 .045
b3	4.95	5.46	.195 .215
c	.46	.61	.018 .024
c1	.41	.56	.016 .022
c2	.046	.89	.016 .035
D	5.97	6.22	.235 .245
D1	5.21	—	.205 —
E	6.35	6.73	.250 .265
E1	4.32	—	.170 —
e	2.29	—	.090 BSC
H	3.40	10.41	.370 .410
L	1.40	1.78	.055 .070
L1	2.74 REF	—	.108 REF
L2	0.051 BSC	—	.020 BSC
L3	0.89	1.27	.035 .050
L4		1.02	.040
L5	1.14	1.52	.045 .060
•	0"	10"	0" 10"
•1	0"	15"	0" 15"

**IGBTs, CoPACK**

1 - GATE
2 - COLLECTOR
3 - Emitter
4 - DRain

**LEAD ASSIGNMENTS**

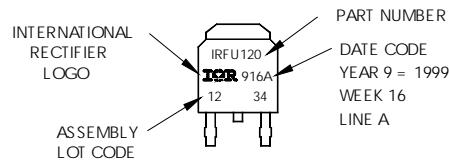
- 1 - GATE
- 2 - COLLECTOR
- 3 - Emitter
- 4 - DRain

**SECTION C-C**

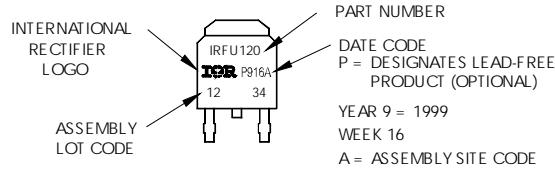
## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 1999  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates "Lead-Free"

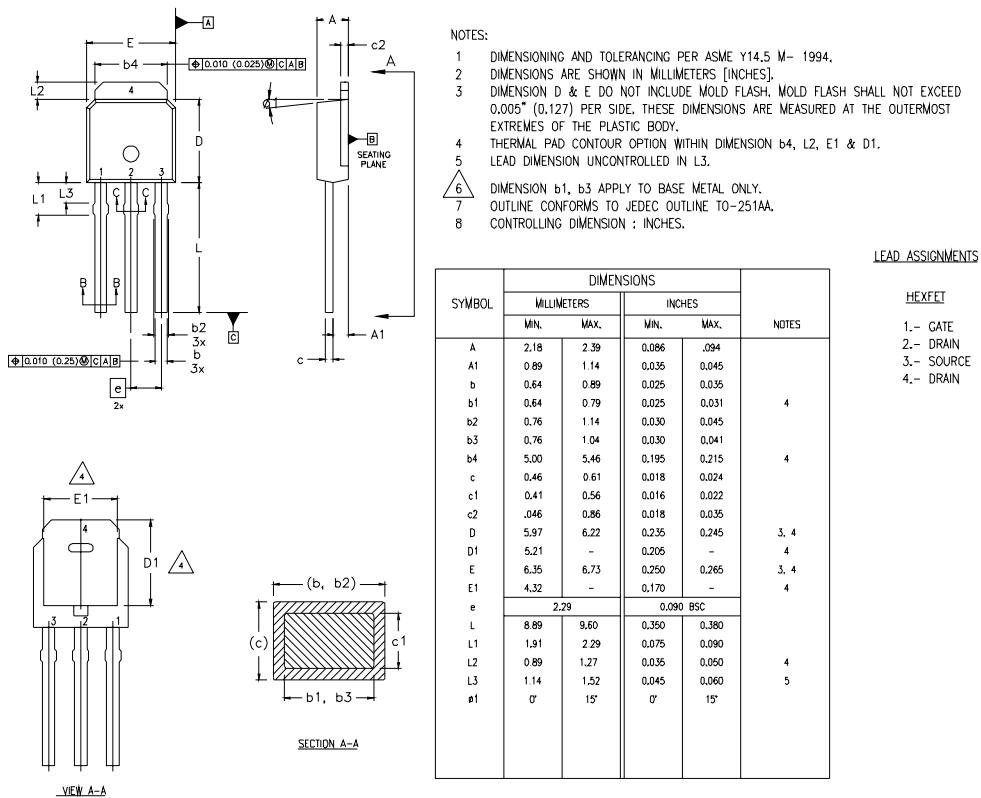


OR



## I-Pak (TO-251AA) Package Outline

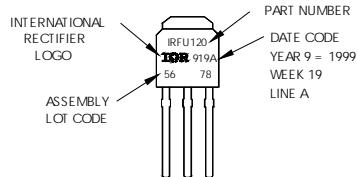
Dimensions are shown in millimeters (inches)



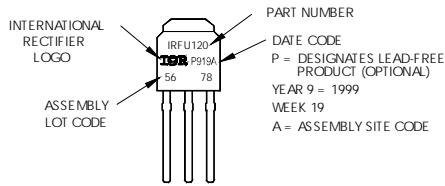
## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
 WITH ASSEMBLY  
 LOT CODE 5678  
 ASSEMBLED ON WW 19, 1999  
 IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line  
 position indicates "Lead-Free"



OR

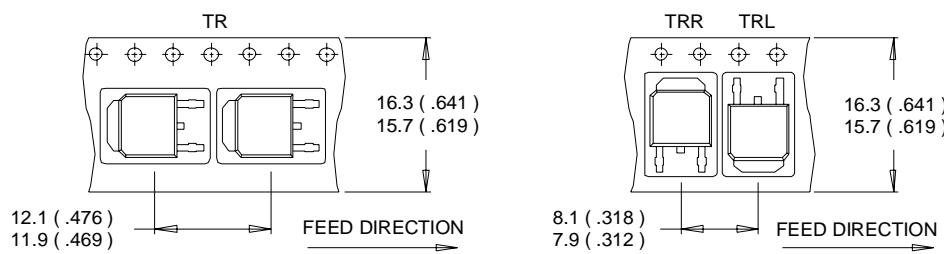


# IRLR/U2705PbF

International  
**IR** Rectifier

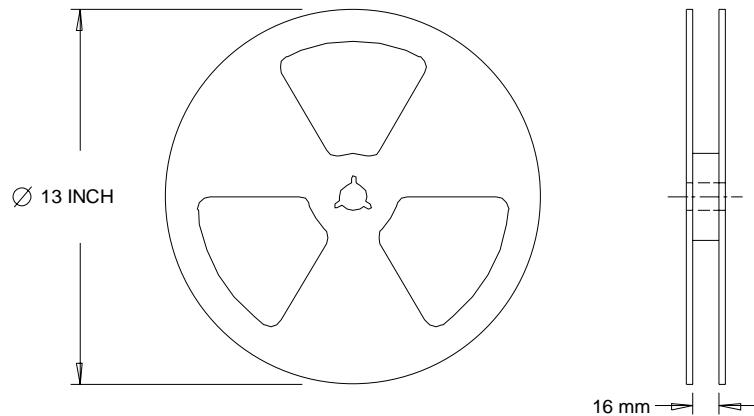
## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

Visit us at [www.irf.com](http://www.irf.com) for sales contact information. 01/05

Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>