



# STB11NK50Z - STP11NK50ZFP STP11NK50Z

N-channel 500 V, 0.48  $\Omega$ , 10 A TO-220, TO-220FP, D<sup>2</sup>PAK  
Zener-protected SuperMESH™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>	P <sub>w</sub>
STB11NK50Z	500 V	< 0.52 $\Omega$	10 A	125 W
STP11NK50ZFP	500 V	< 0.52 $\Omega$	10 A	30 W
STP11NK50Z	500 V	< 0.52 $\Omega$	10 A	125 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances

## Application

- Switching applications

## Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications.

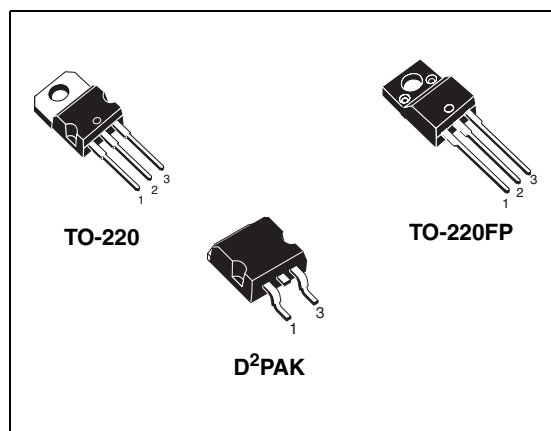


Figure 1. Internal schematic diagram

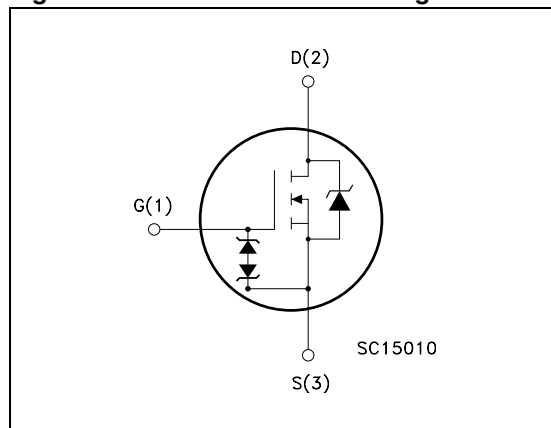


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB11NK50ZT4	B11NK50Z	D <sup>2</sup> PAK	Tape and reel
STP11NK50ZFP	P11NK50ZFP	TO-220FP	Tube
STP11NK50Z	P11NK50Z	TO-220	Tube

Contents

1      **Electrical ratings** ..... 3

2      **Electrical characteristics** ..... 5

      2.1    Electrical characteristics (curves) ..... 7

3      **Test circuit** ..... 10

4      **Package mechanical data** ..... 11

5      **Packaging mechanical data** ..... 15

6      **Revision history** ..... 16



# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220 D <sup>2</sup> PAK	TO-220FP	
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	500		V
$V_{GS}$	Gate-source voltage	$\pm 30$		V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	10	10 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	6.3	6.3 <sup>(1)</sup>	A
$I_{DM}^{(2)}$	Drain current (pulsed)	40	40 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	125	30	W
	Derating factor	1	0.24	W/ $^{\circ}\text{C}$
$V_{ESD(G-S)}$	Gate source ESD (HBM-C= 100 pF, R= 1.5 k $\Omega$ )	4000		V
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5		V/ns
$V_{ISO}$	Insulation withstand voltage (DC)	--	2500	V
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150		$^{\circ}\text{C}$

- Limited only by maximum temperature allowed
- Pulse width limited by safe operating area
- $I_{SD} \leq 10\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$ .

**Table 3. Thermal data**

Symbol	Parameter	Value		Unit
		TO-220 D <sup>2</sup> PAK	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	1	4.2	$^{\circ}\text{C}/\text{W}$
$R_{thj-a}$	Thermal resistance junction-ambient max	62.5		$^{\circ}\text{C}/\text{W}$
$T_I$	Maximum lead temperature for soldering purpose	300		$^{\circ}\text{C}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AS}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max)	10	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	190	mJ

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	500			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating, V <sub>DS</sub> = Max rating @ 125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±20 V			±10	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100 μA	3	3.75	4.5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.5 A		0.48	0.52	Ω

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 4.5 A		7.7		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0		1390 173 42		pF pF pF
C <sub>oss eq</sub> <sup>(2)</sup>	Equivalent output capacitance	V <sub>GS</sub> = 0, V <sub>DS</sub> = 0 to 400 V		110		pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 11.4 A V <sub>GS</sub> = 10 V (see Figure 18)		49 10 25	68	nC nC nC

1. Pulsed: pulse duration = 300 μs, duty cycle 1.5%

2. C<sub>oss eq</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}=250\text{ V}$ , $I_D=5.5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (see Figure 19)		14.5 18		ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD}=250\text{ V}$ , $I_D=5.5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (see Figure 19)		41 15		ns ns
$t_{r(Voff)}$ $t_f$ $t_c$	Off-voltage rise time Fall time Cross-over time	$V_{DD}=400\text{ V}$ , $I_D=11.4\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (see Figure 19)		11.5 12 27		ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				10	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				40	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=10\text{ A}$ , $V_{GS}=0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=10\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=45\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$		308 2.4 16		ns $\mu\text{C}$ A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

Table 9. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{gs}=\pm 1\text{ mA}$ (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220 / D<sup>2</sup>PAK

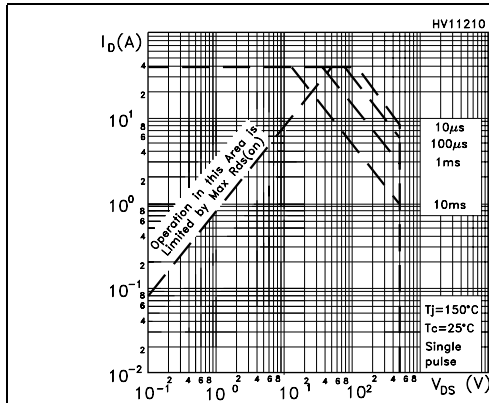


Figure 4. Safe operating area for TO-220FP

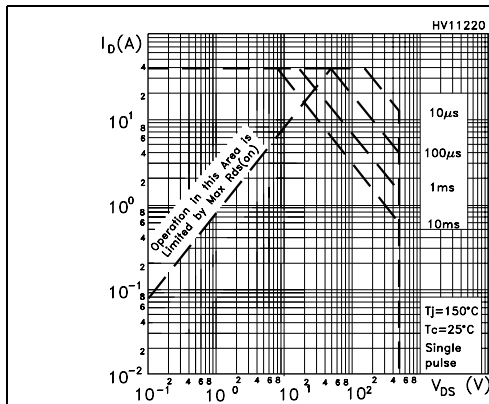


Figure 6. Output characteristics

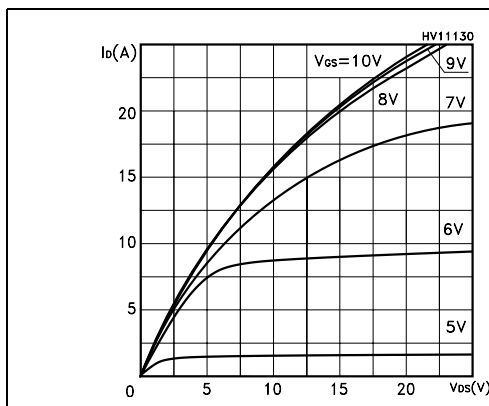


Figure 3. Thermal impedance for TO-220 / D<sup>2</sup>PAK

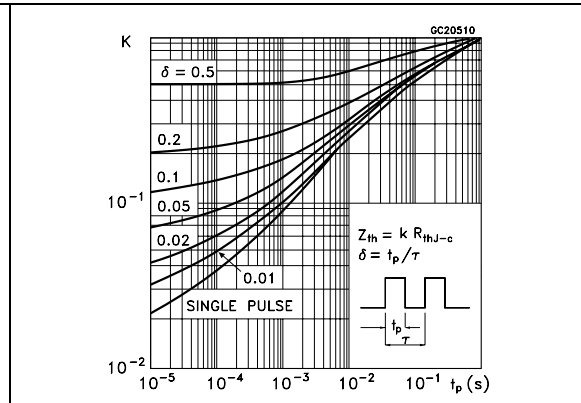


Figure 5. Thermal impedance for TO-220FP

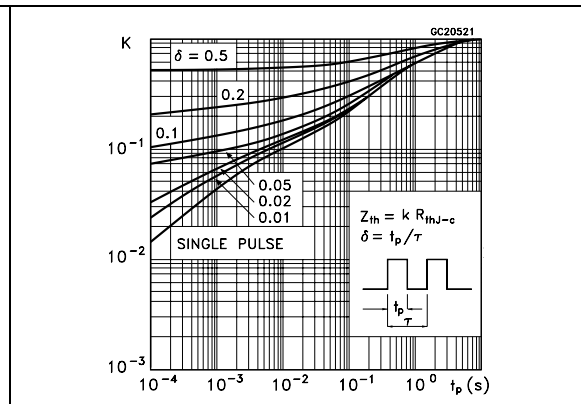


Figure 7. Transfer characteristics

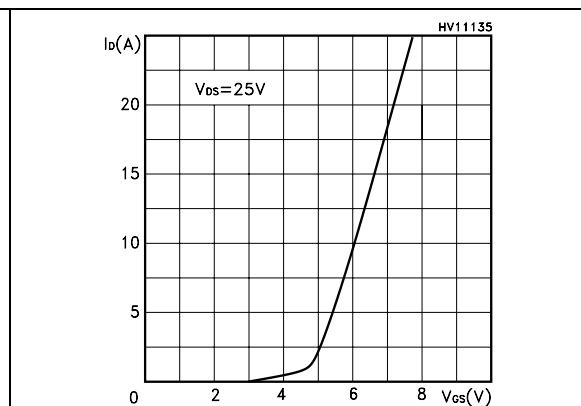


Figure 8. Transconductance

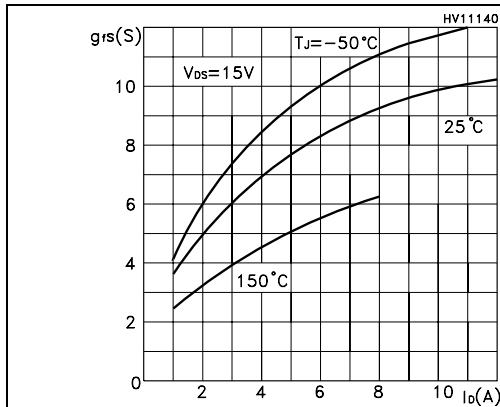


Figure 9. Static drain-source on resistance

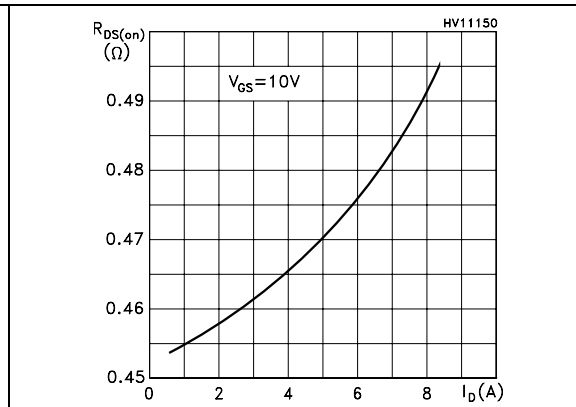


Figure 10. Gate charge vs gate-source voltage

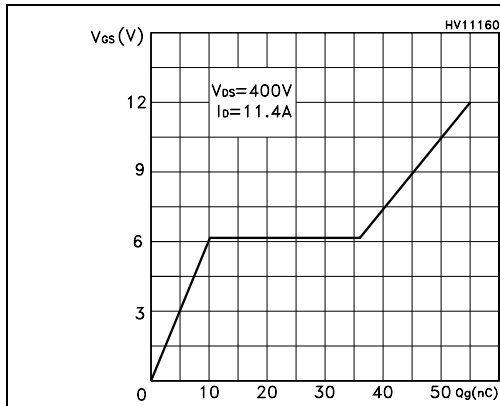


Figure 11. Capacitance variations

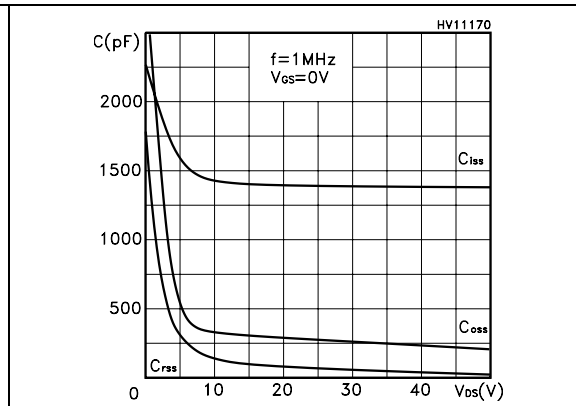


Figure 12. Normalized gate threshold voltage vs temperature

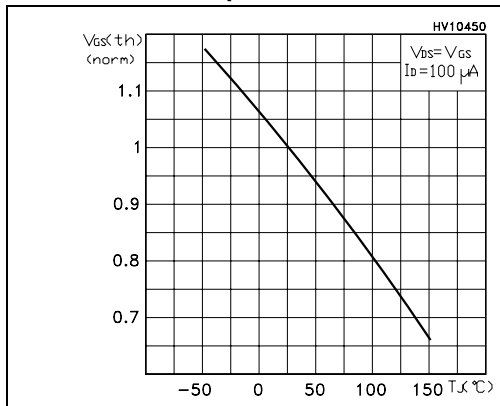


Figure 13. Normalized on resistance vs temperature

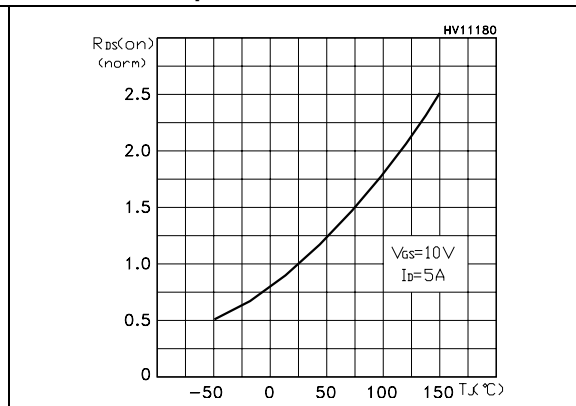


Figure 14. Source-drain diode forward characteristics

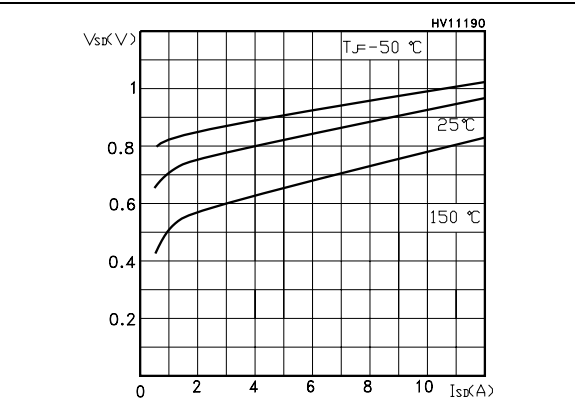


Figure 15. Normalized  $B_{VDSS}$  vs temperature

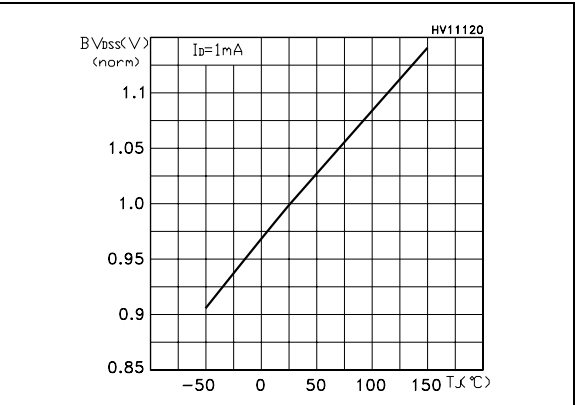
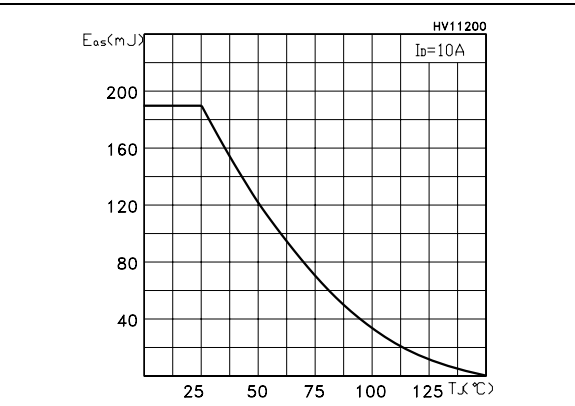


Figure 16. Maximum avalanche energy vs temperature





### 3 Test circuit

Figure 17. Switching times test circuit for resistive load

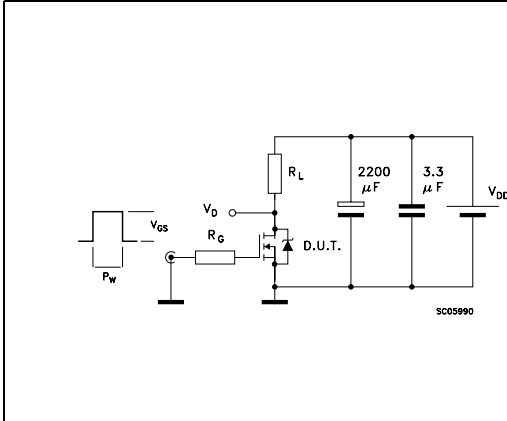


Figure 18. Gate charge test circuit

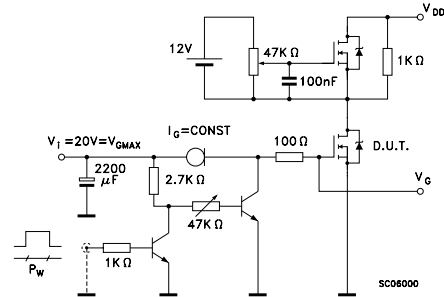


Figure 19. Test circuit for inductive load switching and diode recovery times

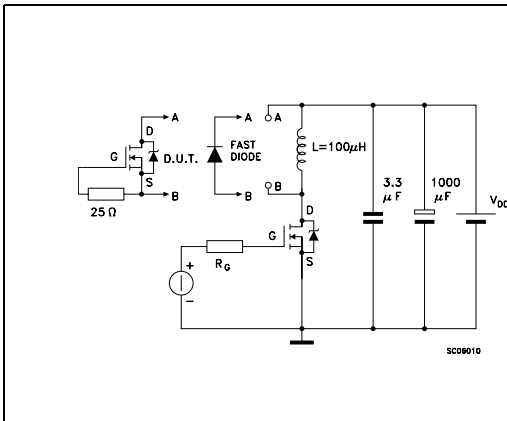


Figure 20. Unclamped Inductive load test circuit

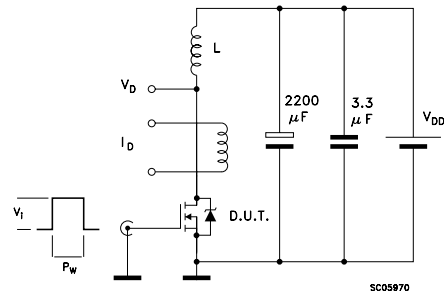


Figure 21. Unclamped inductive waveform

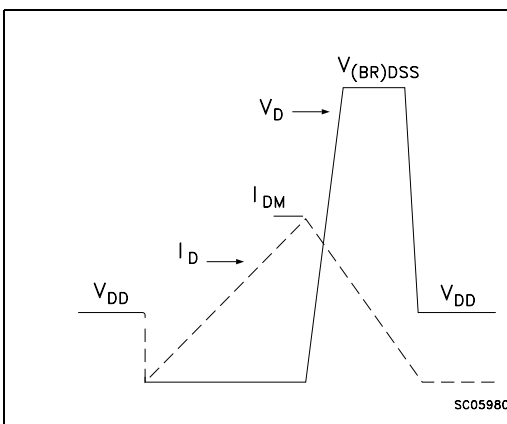
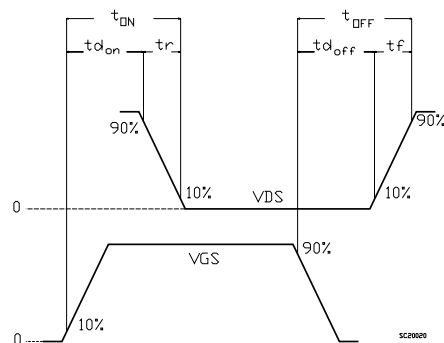


Figure 22. Switching time waveform

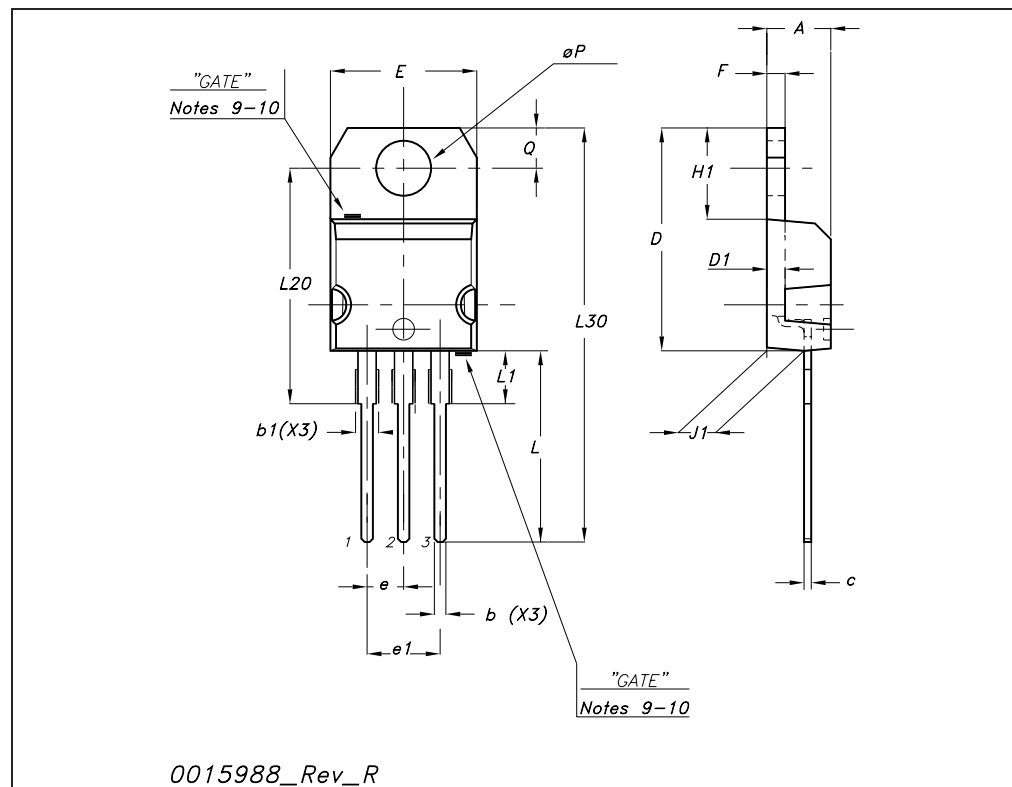


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

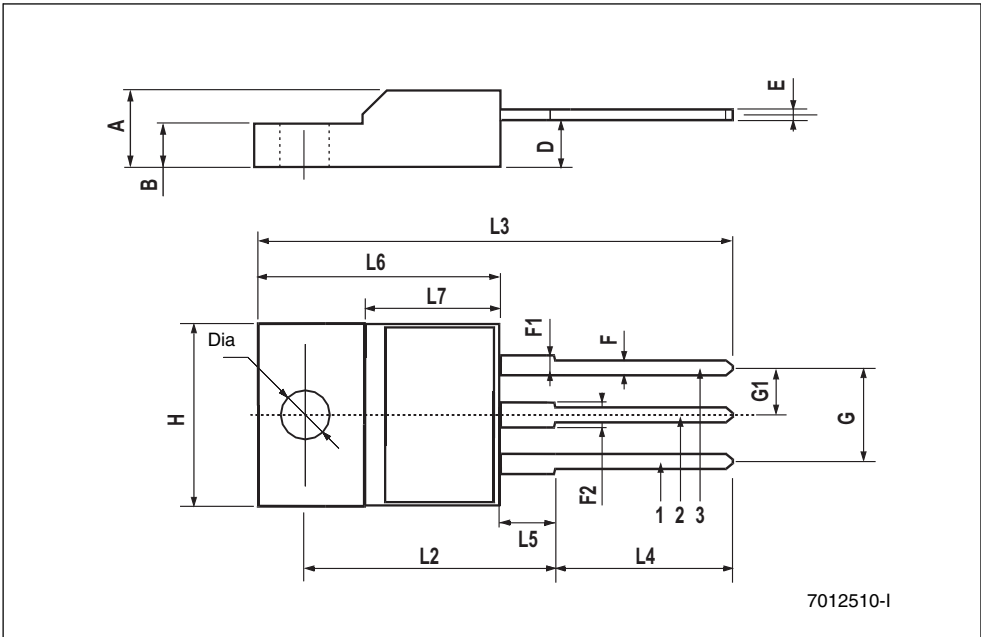
## TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
ØP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



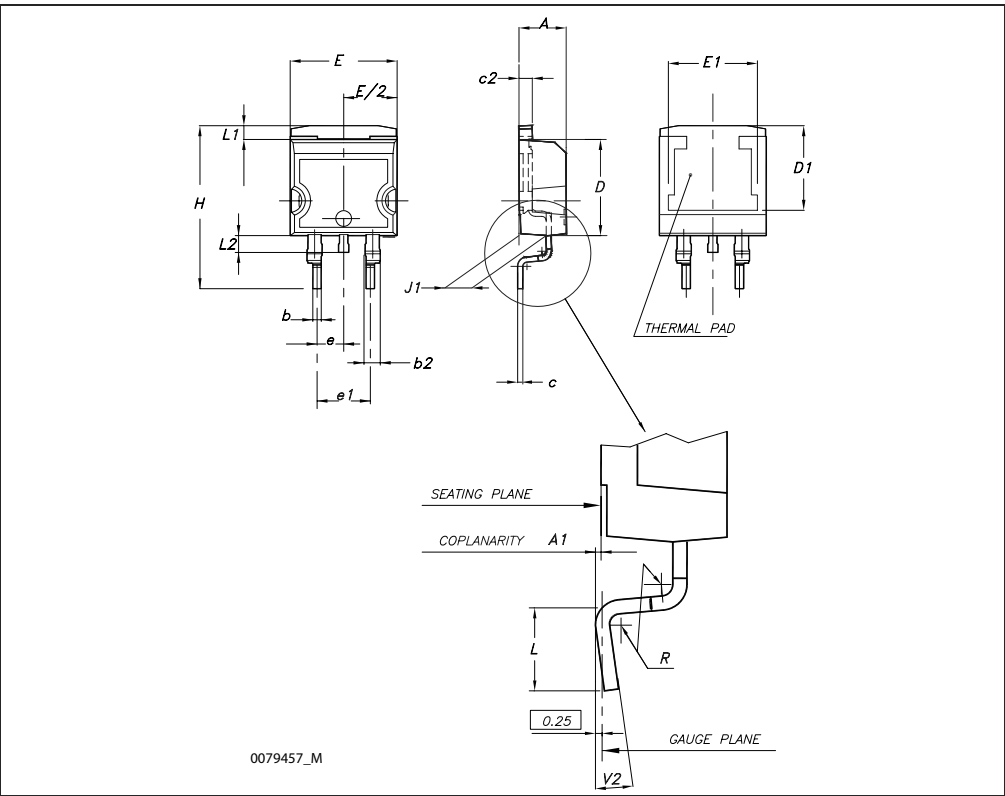
TO-220FP mechanical data

Dim.	mm.			inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.70	0.017		0.027
F	0.75		1.00	0.030		0.039
F1	1.15		1.50	0.045		0.067
F2	1.15		1.50	0.045		0.067
G	4.95		5.20	0.195		0.204
G1	2.40		2.70	0.094		0.106
H	10		10.40	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.80		10.60	0.385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.90		16.40	0.626		0.645
L7	9		9.30	0.354		0.366
Dia	3		3.2	0.118		0.126



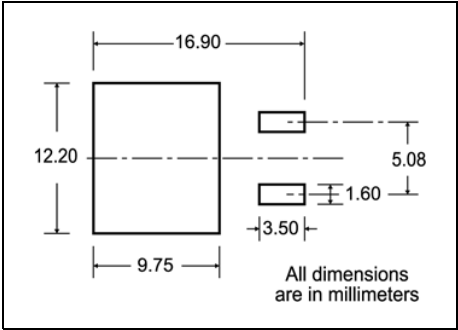
D<sup>2</sup>PAK (TO-263) mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	0.03		0.23	0.001		0.009
b	0.70		0.93	0.027		0.037
b2	1.14		1.70	0.045		0.067
c	0.45		0.60	0.017		0.024
c2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1	7.50			0.295		
E	10		10.40	0.394		0.409
E1	8.50			0.334		
e		2.54			0.1	
e1	4.88		5.28	0.192		0.208
H	15		15.85	0.590		0.624
J1	2.49		2.69	0.099		0.106
L	2.29		2.79	0.090		0.110
L1	1.27		1.40	0.05		0.055
L2	1.30		1.75	0.051		0.069
R		0.4			0.016	
V2	0°		8°	0°		8°

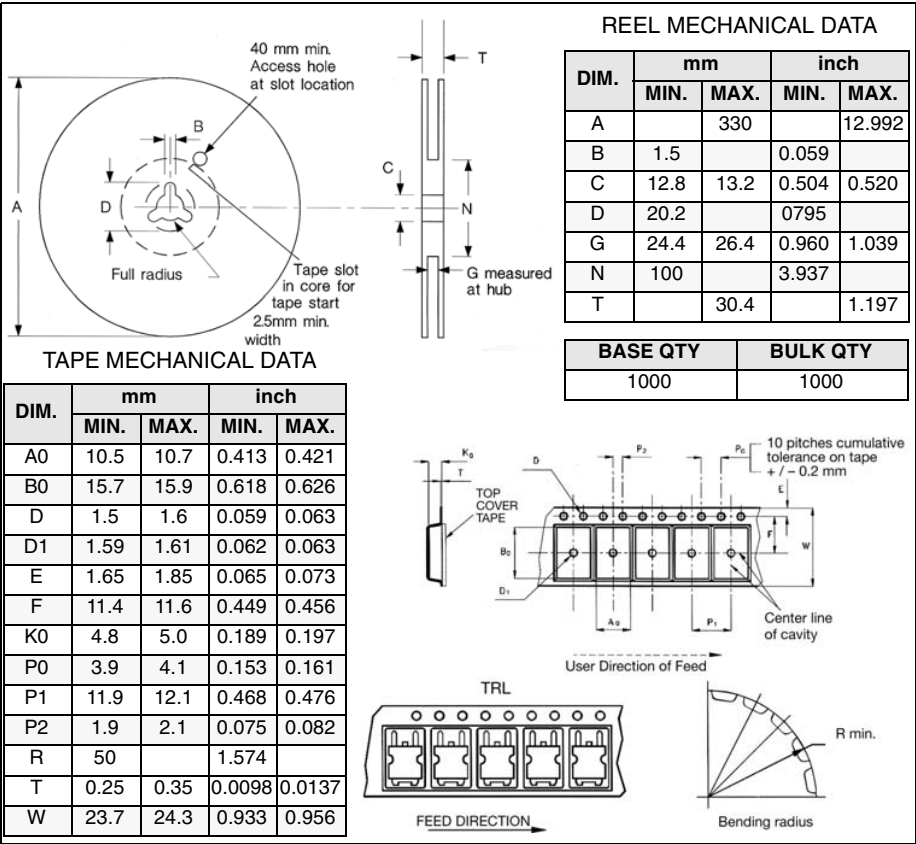


5 Packaging mechanical data

D<sup>2</sup>PAK FOOTPRINT



TAPE AND REEL SHIPMENT



\* on sales type

## 6 Revision history

Table 10. Revision history

Date	Revision	Changes
08-Sep-2005	3	Complete version with curves
14-Oct-2005	4	Inserted ecopack indication
26-Mar-2006	5	New template, no content change
29-Apr-2008	6	I <sub>GSS</sub> value changed in <a href="#">Table 6</a>

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2008 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)