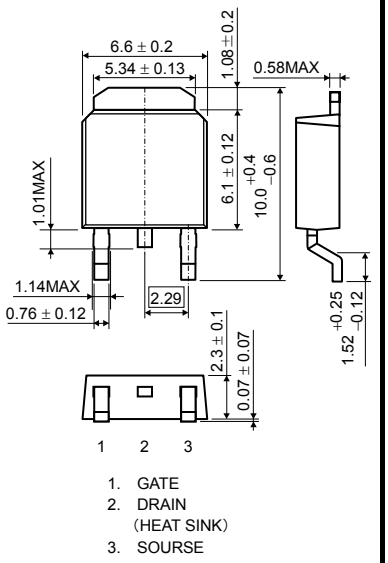
TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (U-MOSⅥ-H)

TK50P03M1

High-Efficiency DC-DC Converter Applications
Desktop PC Applications

- High-speed switching
- Small gate charge: Q_{SW} = 8.2 nC (typ.)
- Low drain-source ON-resistance: $R_{DS\ (ON)}$ = 5.8 mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 90 S (typ.)
- Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 30 V)
- Enhancement mode: V_{th} = 1.3 to 2.3 V (V_{DS} = 10 V, I_D = 0.2 mA)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-7K1A

Weight: 0.36 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	30	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	50	A
	Pulsed (Note 1)	I_{DP}	150	
Drain power dissipation (Tc = 25°C)		P_D	60	W
Single-pulse avalanche energy (Note 2)		E_{AS}	65	mJ
Avalanche current		I_{AR}	50	A
Repetitive avalanche energy (Tc=25℃) (Note 3)		E_{AR}	5.2	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: For Notes 1 to 3, refer to the next page.

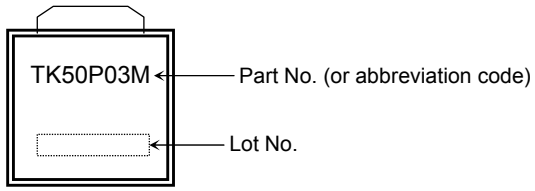
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Handle with care.

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	2.08	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	125	°C / W

Marking (Note 4)

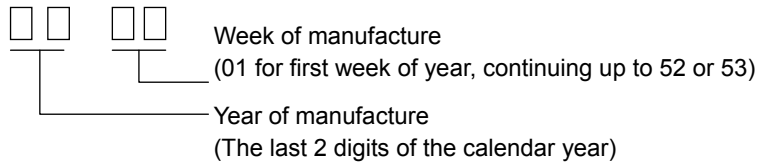


Note 1: The channel temperature should not exceed 150°C during use.

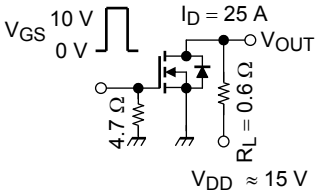
Note 2: V_{DD} = 24 V, T_{ch} = 25°C (initial), L = 20 μH, R_G = 25 Ω, I_{AR} = 50 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

Note 4: * Weekly code: (Four digits)



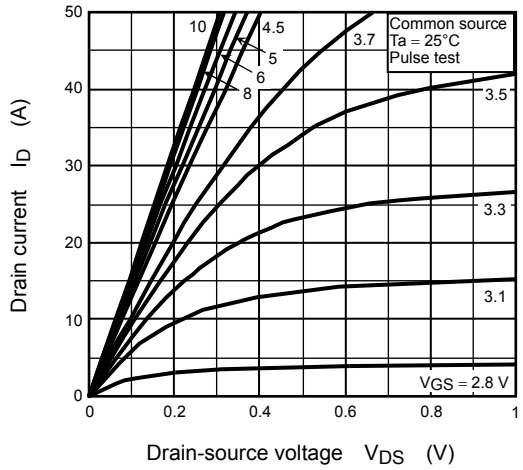
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±100	nA
Drain cutoff current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	30	—	—	V
		$V_{(BR)\ DSX}$	I_D = 10 mA, V_{GS} = −20 V	15	—	—	
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 0.2 mA	1.3	—	2.3	V
Drain-source ON-resistance		$R_{DS\ (ON)}$	V_{GS} = 4.5 V, I_D = 25 A	—	7.5	9.8	mΩ
			V_{GS} = 10 V, I_D = 25 A	—	5.8	7.5	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 25 A	45	90	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	1700	—	pF
Reverse transfer capacitance		C_{rss}		—	125	—	
Output capacitance		C_{oss}		—	380	—	
Gate resistance		rg	V_{DS} = 10 V, V_{GS} = 0 V, f = 5 MHz	—	1.7	—	Ω
Switching time	Rise time	t_r	 Duty ≤ 1%, t_w = 10 μs	—	20	—	ns
	Turn-on time	t_{on}		—	25	—	
	Fall time	t_f		—	22	—	
	Turn-off time	t_{off}		—	64	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ 24 V, V_{GS} = 10 V, I_D = 50 A	—	25.3	—	nC
			V_{DD} ≈ 24 V, V_{GS} = 5 V, I_D = 50 A	—	13.3	—	
Gate-source charge 1		Q_{gs1}	V_{DD} ≈ 24 V, V_{GS} = 10 V, I_D = 50 A	—	6.3	—	
Gate-drain (“Miller”) charge		Q_{gd}		—	4.6	—	
Gate switch charge		Q_{SW}		—	8.2	—	

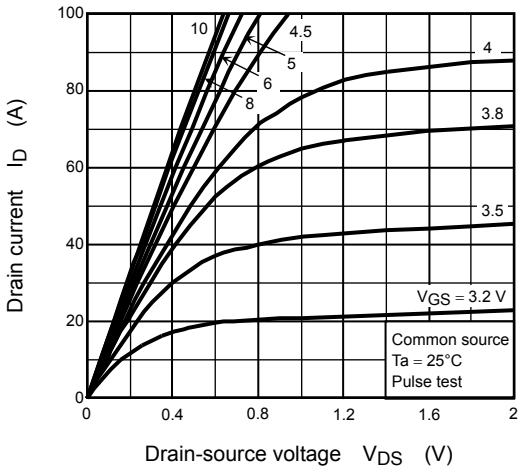
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	150	A
Forward voltage (diode)		V_{DSF}	I_{DR} = 50 A, V_{GS} = 0 V	—	—	−1.2	V

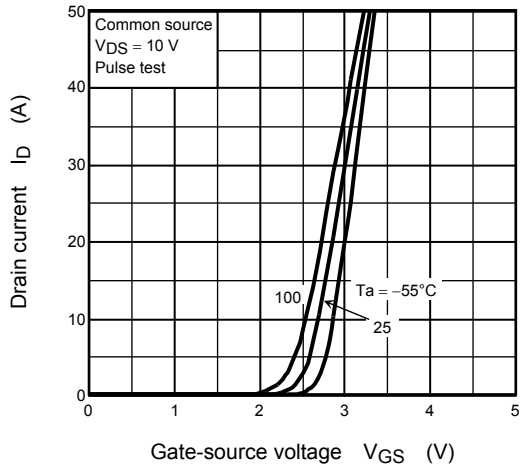
$I_D - V_{DS}$



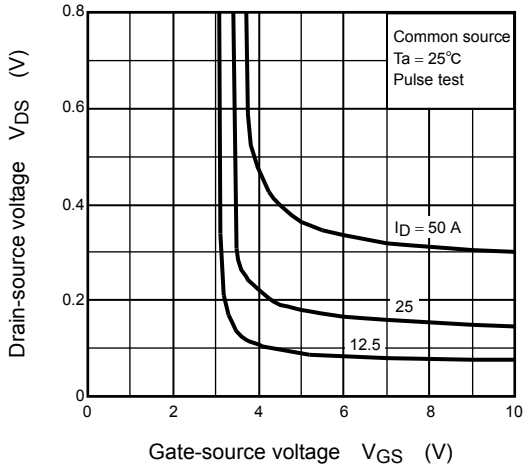
$I_D - V_{DS}$



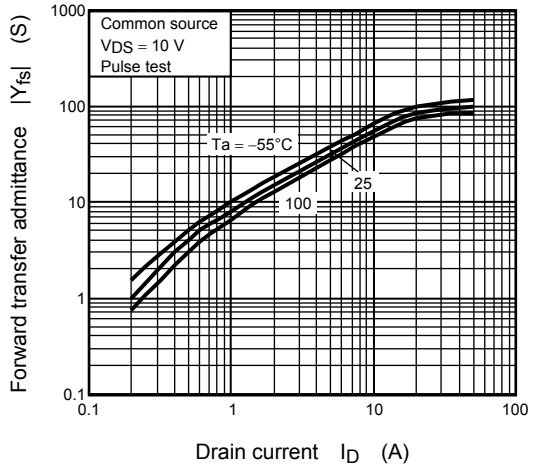
$I_D - V_{GS}$



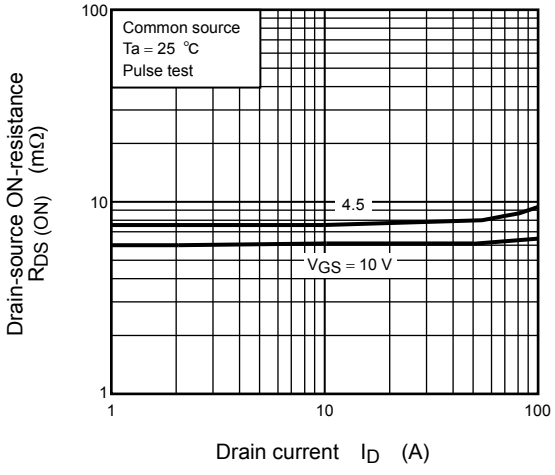
$V_{DS} - V_{GS}$



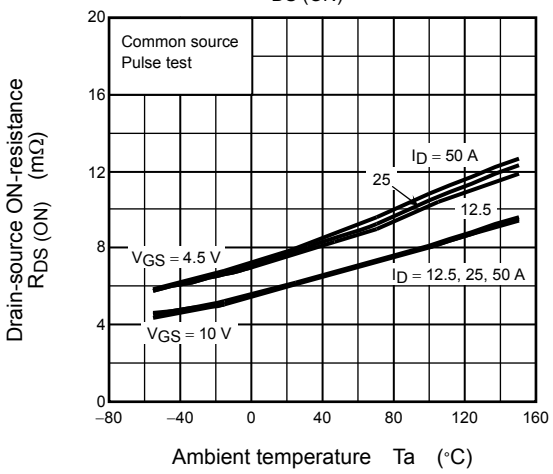
$|Y_{fs}| - I_D$



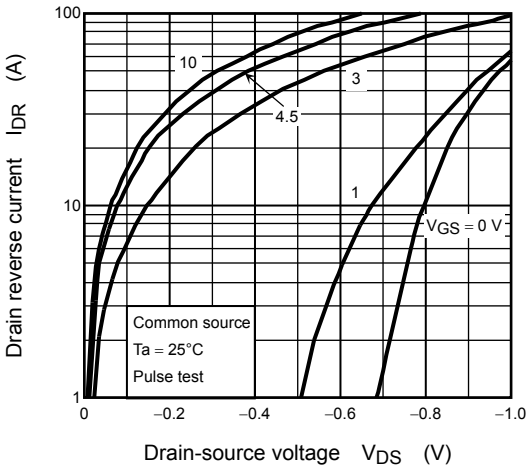
$R_{DS\ (ON)} - I_D$



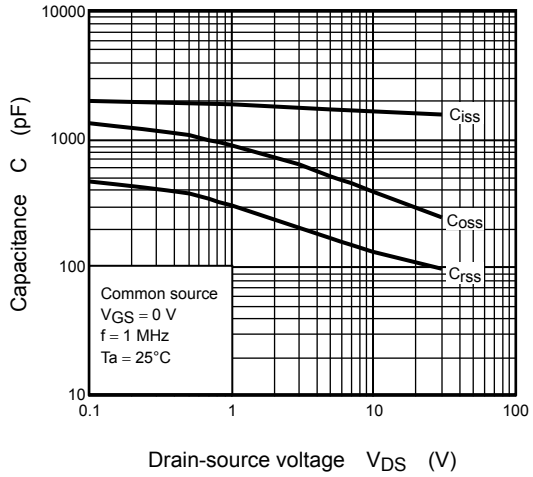
$R_{DS\ (ON)}$ – Ta



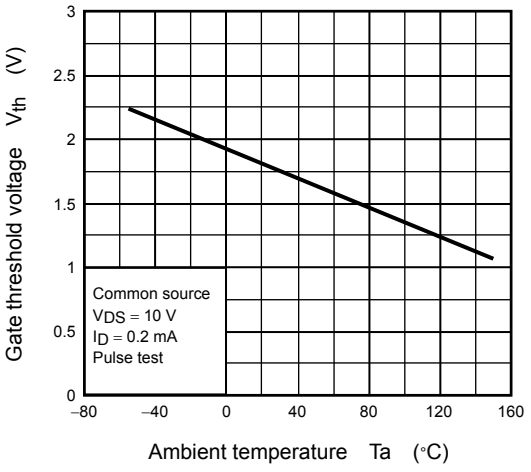
I_{DR} – V_{DS}



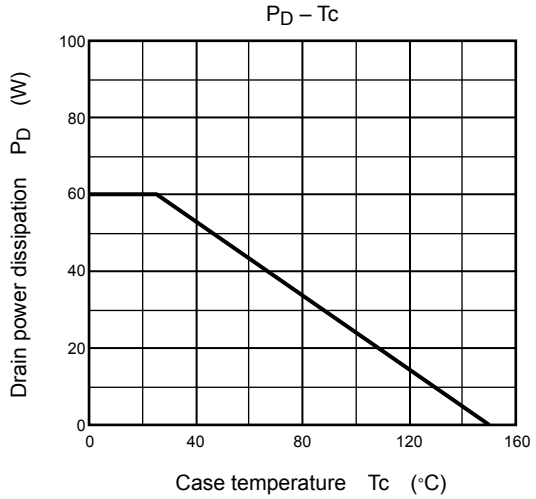
Capacitance – V_{DS}



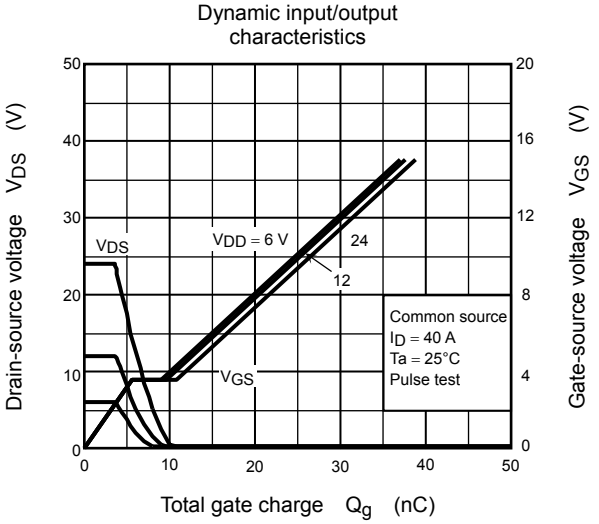
V_{th} – Ta



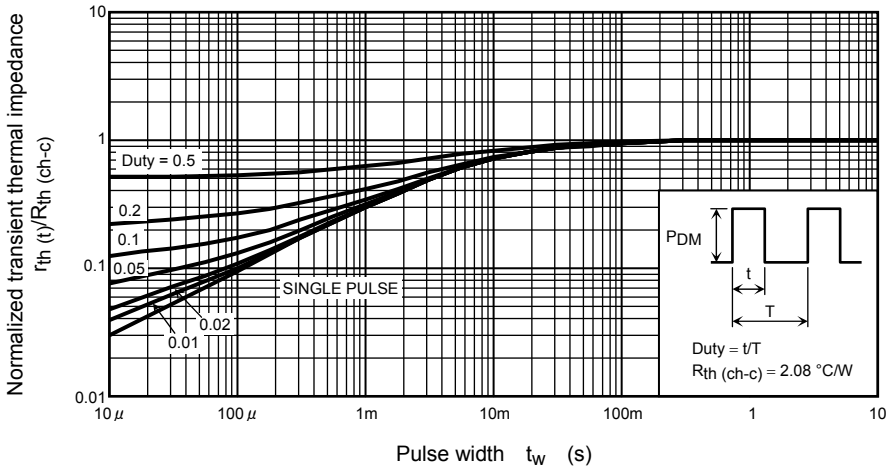
P_D – Tc



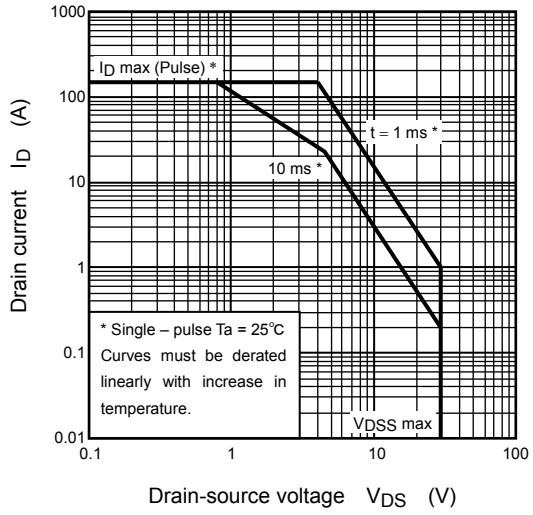
Dynamic input/output characteristics



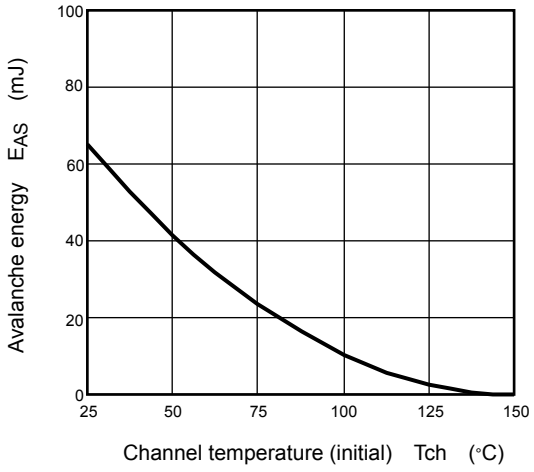
r_{th} /$R_{th\ (ch\text{-}c)}$ – t_w

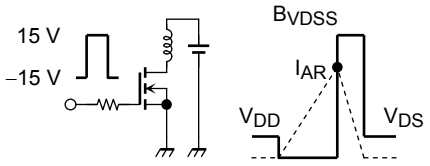


Safe operating area



E_{AS} – Tch





Test circuit Wave form

$R_G = 25\ \Omega$
$V_{DD} = 24$ V, L = 20 μH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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