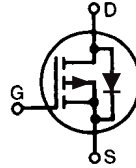


PolarP™
Power MOSFET

IXTK40P50P
IXTX40P50P

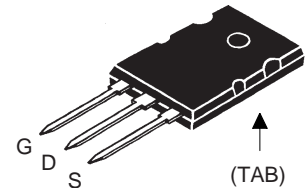
$V_{DSS} = -500V$
 $I_{D25} = -40A$
 $R_{DS(on)} \leq 230m\Omega$

P-Channel Enhancement Mode
Avalanche Rated

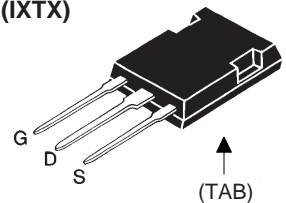


Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	- 500	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$	- 500	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ C$	- 40	A
I_{DM}	$T_C = 25^\circ C$, Pulse Width Limited by T_{JM}	- 120	A
I_A	$T_C = 25^\circ C$	- 40	A
E_{AS}	$T_C = 25^\circ C$	3.5	J
dV/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ C$	10	V/ns
P_D	$T_C = 25^\circ C$	890	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	1.6mm (0.062 in.) from Case for 10s	300	$^\circ C$
T_{SOLD}	Plastic Body for 10s	260	$^\circ C$
M_d	Mounting Force (PLUS247) Mounting Torque (TO-264)	20..120/4.5..27 1.13/10	N/lb. Nm/lb.in.
Weight	PLUS247 TO-264	6 10	g g

TO-264 (IXTK)



PLUS247 (IXTX)



G = Gate D = Drain
S = Source TAB = Drain

Features

- International Standard Packages
- Rugged PolarP™ Process
- Avalanche Rated
- Fast Intrinsic Diode
- Low Package Inductance

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- High-Side Switches
- Push Pull Amplifiers
- DC Choppers
- Automatic Test Equipment
- Current Regulators

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = -250\mu A$	- 500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -1mA$	- 2.0		- 4.0 V
I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ C$			- 50 μA - 250 μA
$R_{DS(on)}$	$V_{GS} = -10V$, $I_D = 0.5 \cdot I_{D25}$, Note 1			230 m Ω

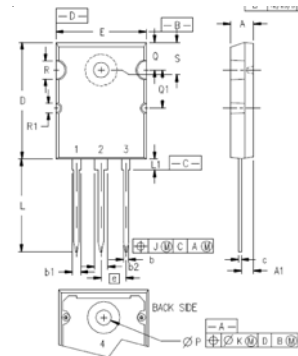
Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = -10\text{V}$, $I_D = 0.5 \cdot I_{D25}$, Note 1	23	38	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = -25\text{V}$, $f = 1\text{MHz}$		11.5	nF
C_{oss}			1150	pF
C_{rss}			93	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = -10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$ $R_G = 1\Omega$ (External)		37	ns
t_r			59	ns
$t_{d(off)}$			90	ns
t_f			34	ns
$Q_{g(on)}$	$V_{GS} = -10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$		205	nC
Q_{gs}			55	nC
Q_{gd}			75	nC
R_{thJC}			0.14	$^\circ\text{C/W}$
R_{thCS}		0.15		$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_s	$V_{GS} = 0\text{V}$			- 40 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			- 160 A
V_{SD}	$I_F = -20\text{A}$, $V_{GS} = 0\text{V}$, Note 1			- 3.0 V
t_{rr}	$I_F = -20\text{A}$, $-di/dt = -150\text{A}/\mu\text{s}$ $V_R = -100\text{V}$, $V_{GS} = 0\text{V}$		477	nS
Q_{RM}			14.5	μC
I_{RM}			- 61	A

Note 1: Pulse Test, $t \leq 300\mu\text{s}$; Duty Cycle, $d \leq 2\%$.

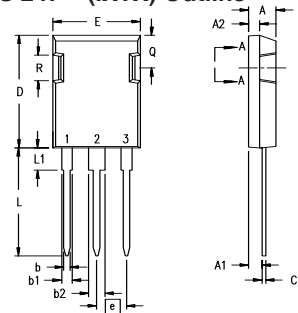
TO-264 (IXTK) Outline



1 - GATE
2, 4 - DRAIN (COLLECTOR)
3 - SOURCE (EMITTER)

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.209	4.70	5.31
A1	.102	.118	2.59	3.00
b	.037	.055	0.94	1.40
b1	.087	.102	2.21	2.59
b2	.110	.126	2.79	3.20
c	.017	.029	0.43	0.74
D	1.007	1.047	25.58	26.59
E	.760	.799	19.30	20.29
e	.215BSC		5.46 BSC	
J	.000	.010	0.00	0.25
K	.000	.010	0.00	0.25
L	.779	.842	19.79	21.39
L1	.087	.102	2.21	2.59
ØP	.122	.138	3.10	3.51
Q	.240	.256	6.10	6.50
Q1	.330	.346	8.38	8.79
ØR	.155	.187	3.94	4.75
ØR1	.085	.093	2.16	2.36
S	.243	.253	6.17	6.43

PLUS 247™ (IXTX) Outline



Terminals: 1 - Gate
2 - Drain (Collector)
3 - Source (Emitter)
4 - Drain (Collector)

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.83	5.21	.190	.205
A ₁	2.29	2.54	.090	.100
A ₂	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b ₁	1.91	2.13	.075	.084
b ₂	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	0.244
R	4.32	4.83	.170	.190

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ 25°C

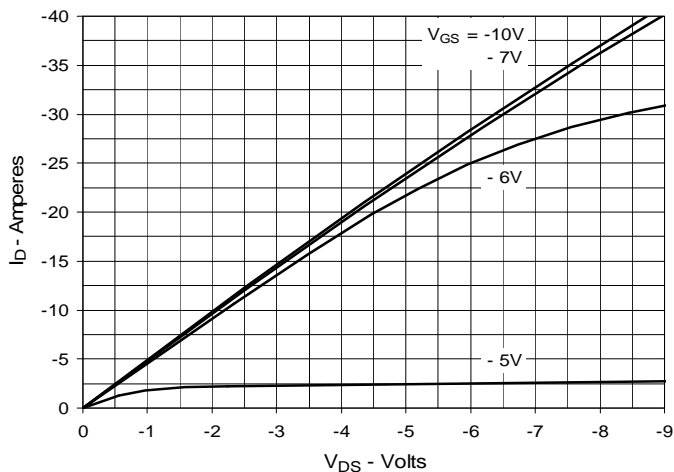


Fig. 2. Extended Output Characteristics @ 25°C

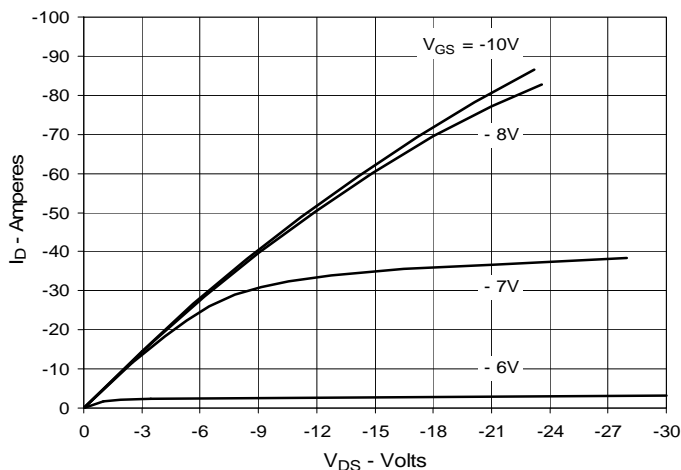


Fig. 3. Output Characteristics @ 125°C

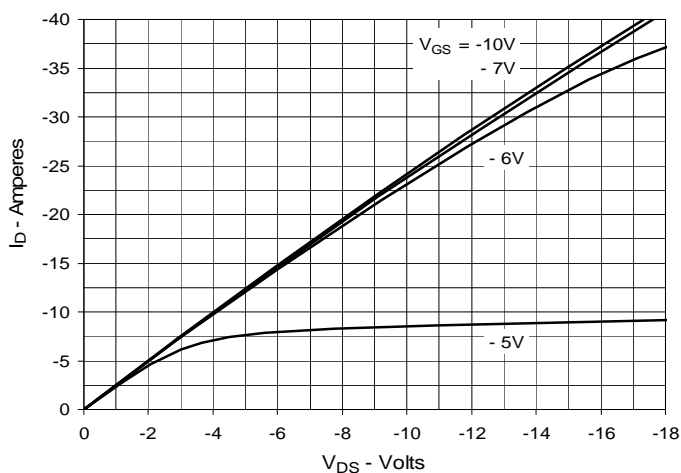


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = -20A$ vs. Junction Temperature

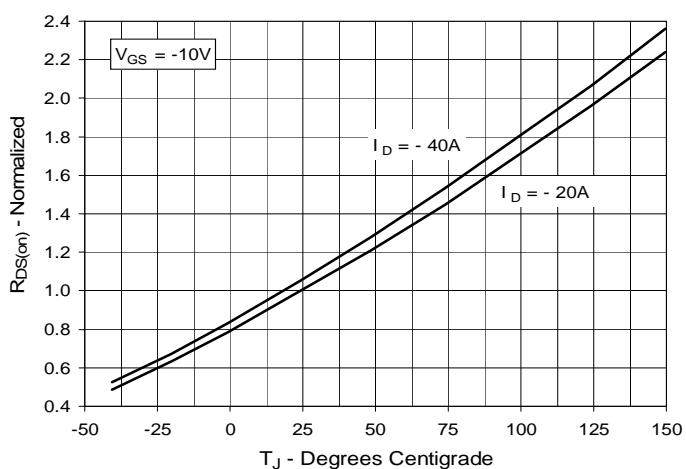


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = -20A$ vs. Drain Current

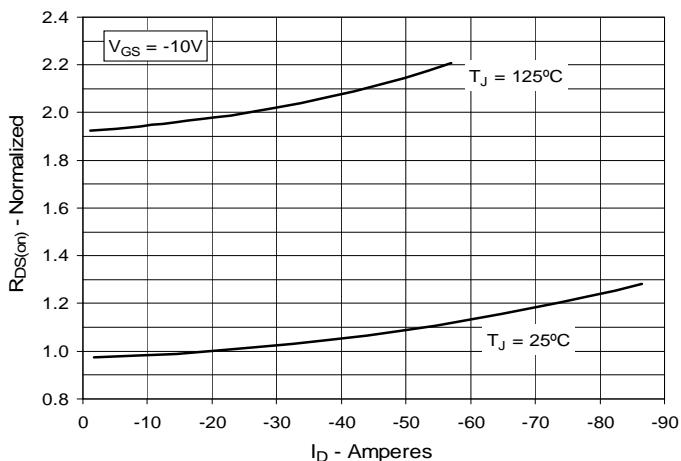


Fig. 6. Maximum Drain Current vs. Case Temperature

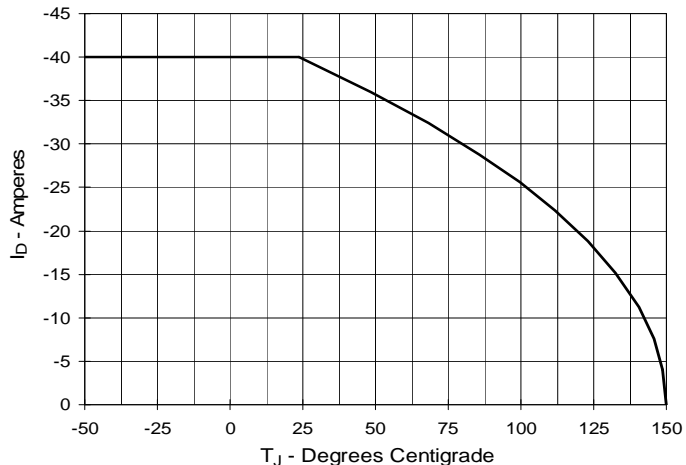


Fig. 7. Input Admittance

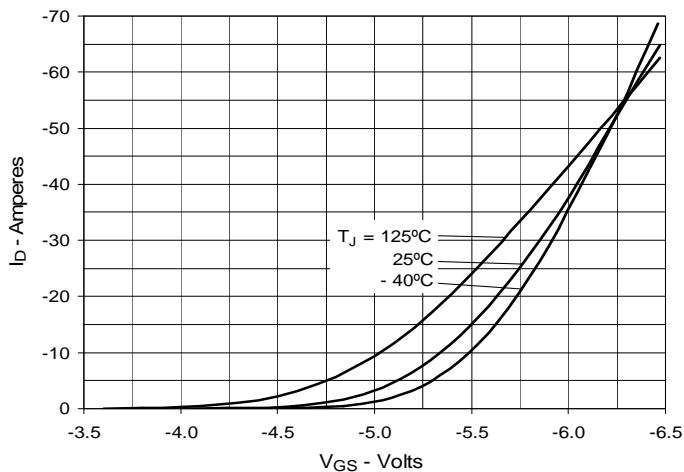


Fig. 8. Transconductance

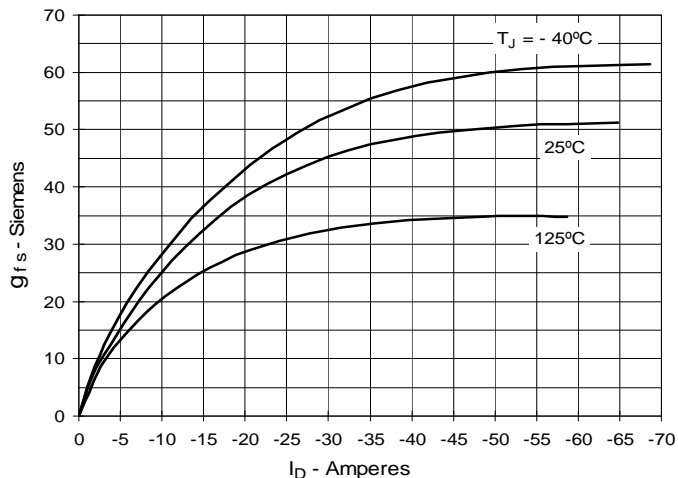


Fig. 9. Forward Voltage Drop of Intrinsic Diode

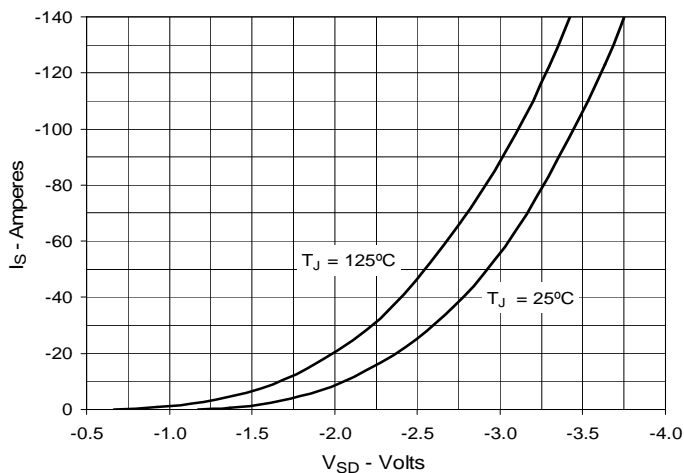


Fig. 10. Gate Charge

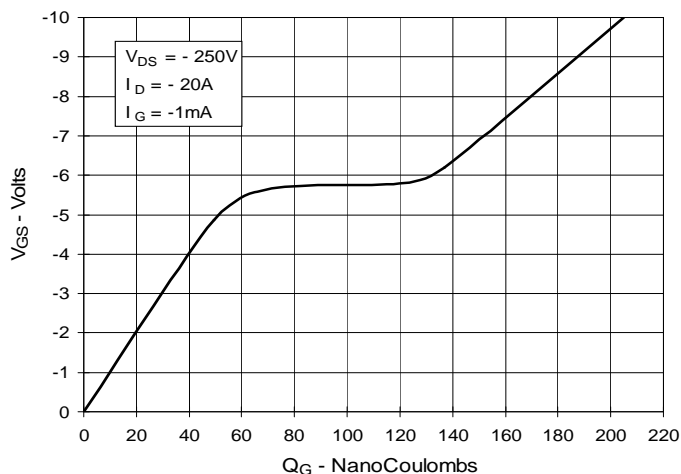


Fig. 11. Capacitance

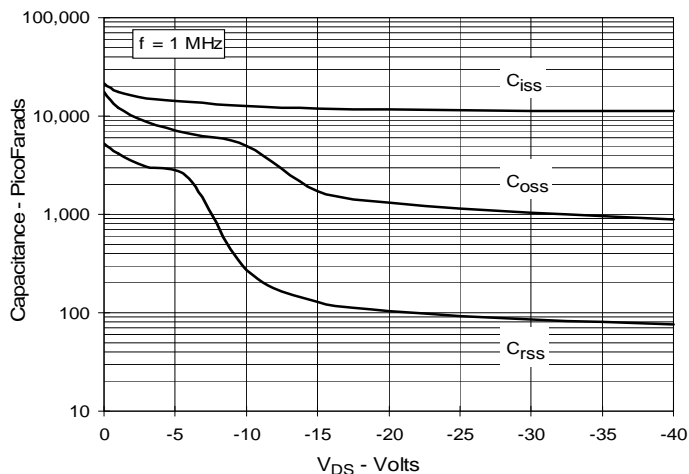


Fig. 12. Forward-Bias Safe Operating Area

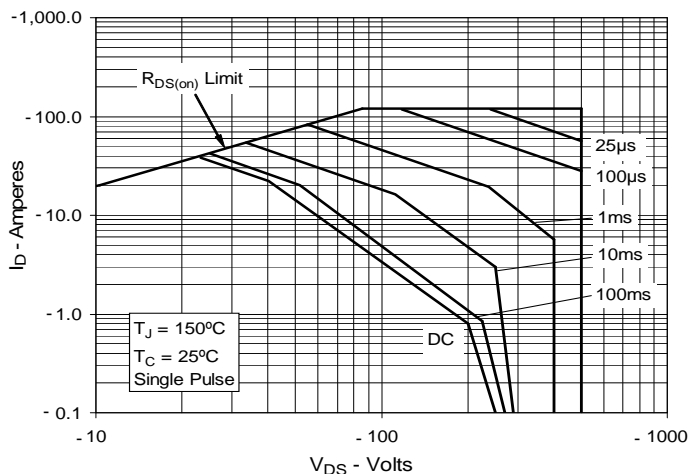


Fig. 13. Maximum Transient Thermal Impedance

