



# STW26NM50

N-channel 500 V, 0.10  $\Omega$ , 30 A TO-247  
MDmesh™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>
STW26NM50	500 V	< 0.12 $\Omega$	30 A

- High dv/dt and avalanche capabilities
- Improved ESD capability
- Low input capacitance and gate charge

## Application

- Switching applications

## Description

MDmesh™ technology applies the benefits of the multiple drain process to STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product offers low on-resistance, high dv/dt capability and excellent avalanche characteristics.

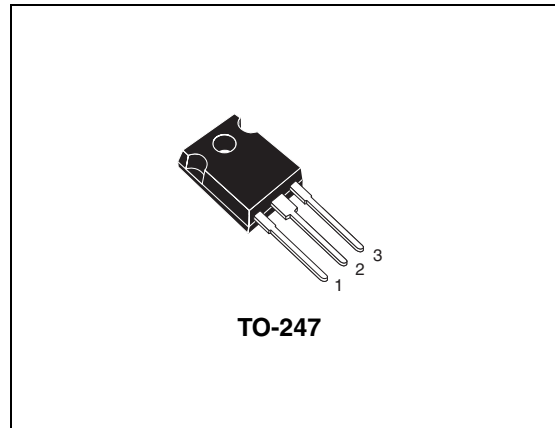


Figure 1. Internal schematic diagram

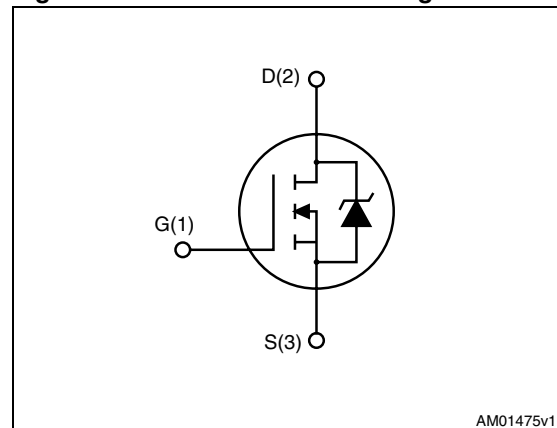


Table 1. Device summary

Order codes	Marking	Package	Packaging
STW26NM50	W26NM50	TO-247	Tube

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# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	500	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	30	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	18.9	A
$I_{DM}^{(1)}$	Drain current (pulsed)	120	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	313	W
	Derating factor	2.5	W/°C
$V_{ESD(G-S)}$	Gate source ESD (HBM-C=100 pF, R=1.5 k $\Omega$ )	6000	V
dv/dt <sup>(2)</sup>	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	-55 to 150	°C
$T_j$	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 26\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{jMAX}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.4	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	°C/W
$T_l$	Maximum lead temperature for soldering purpose	300	°C

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_{jmax}$ )	13	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$ , $I_D=I_{AR}$ , $V_{DD}=50\text{ V}$ )	740	mJ

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	500			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating V <sub>DS</sub> = Max rating, T <sub>C</sub> = 125 °C			10 100	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			± 10	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3	4	5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 13 A		0.10	0.12	Ω

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 13 A	-	20	-	S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer Capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0	-	3000 700 50	-	pF pF pF
C <sub>oss eq.</sub> <sup>(2)</sup>	Equivalent output capacitance	V <sub>GS</sub> = 0, V <sub>DS</sub> = 0 to 400 V	-	300	-	pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 26 A, V <sub>GS</sub> = 10 V, (see Figure 15)	-	76 20 36	-	nC nC nC

1. Pulsed: pulse duration = 300 μs, duty cycle 1.5%

2. C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DS</sub>

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 13 A,		28		ns
t <sub>r</sub>	Rise time	R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V,		15		ns
t <sub>d(off)</sub>	Turn-off-delay time	(see Figure 15)	-	13	-	ns
t <sub>f</sub>	Fall time			19		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		26	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		104	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 26\text{ A}, V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 26\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	400		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100\text{ V}$	-	5.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 16)	-	27.8		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 26\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	492		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 16)	-	28.8		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 9. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ (open drain)	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

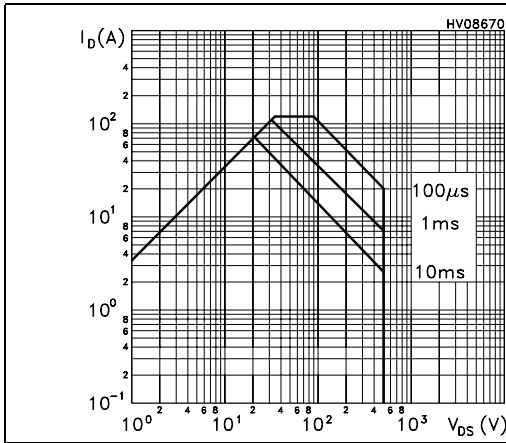


Figure 3. Thermal impedance

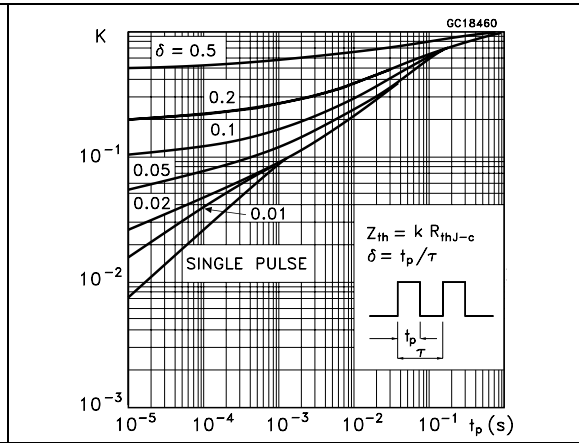


Figure 4. Output characteristics

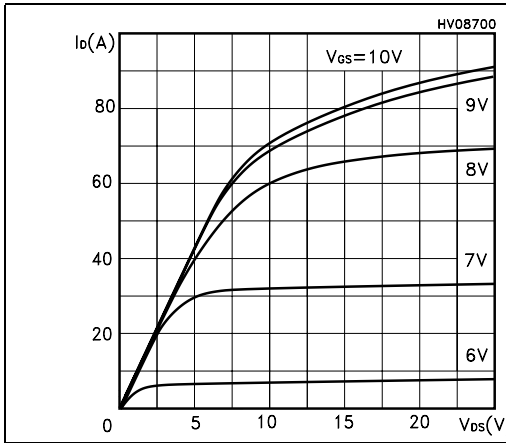


Figure 5. Transfer characteristics

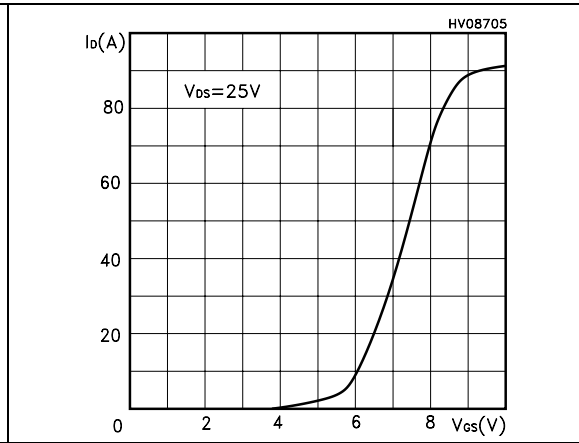


Figure 6. Transconductance

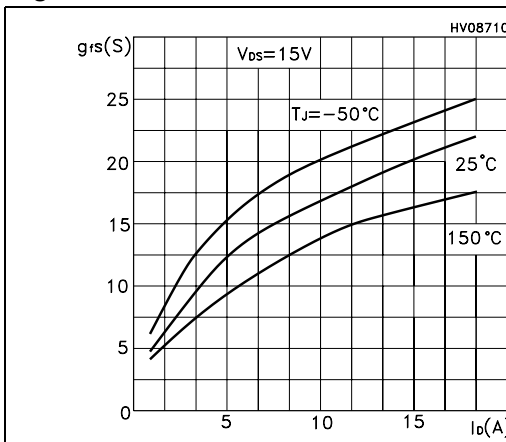


Figure 7. Static drain-source on resistance

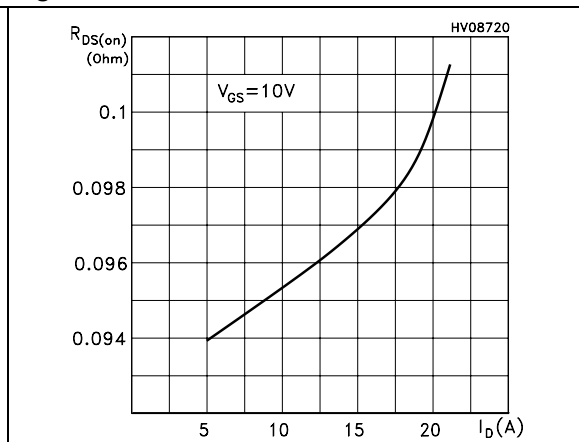


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

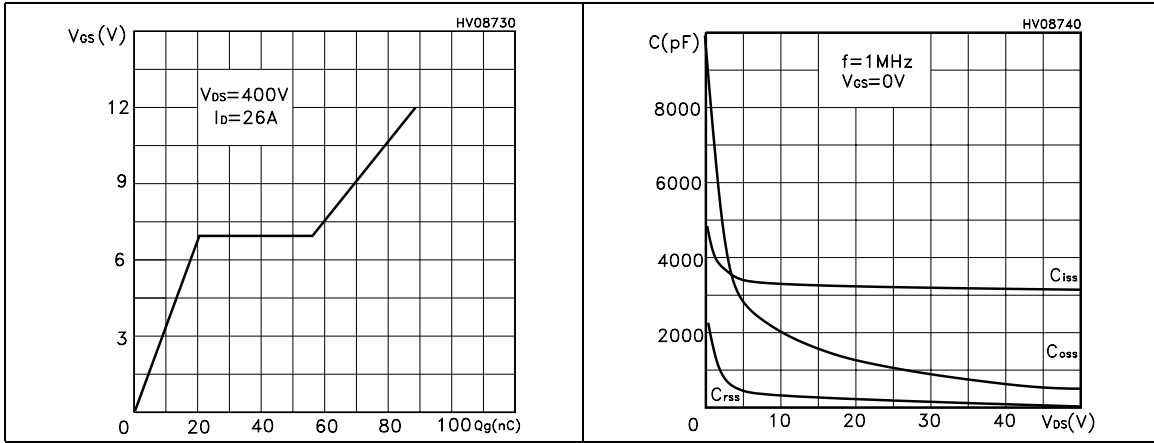


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

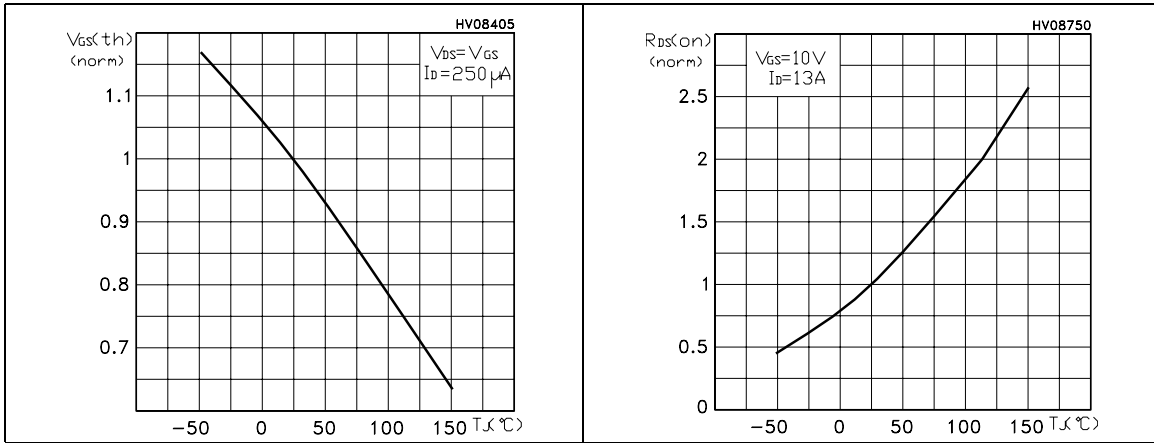
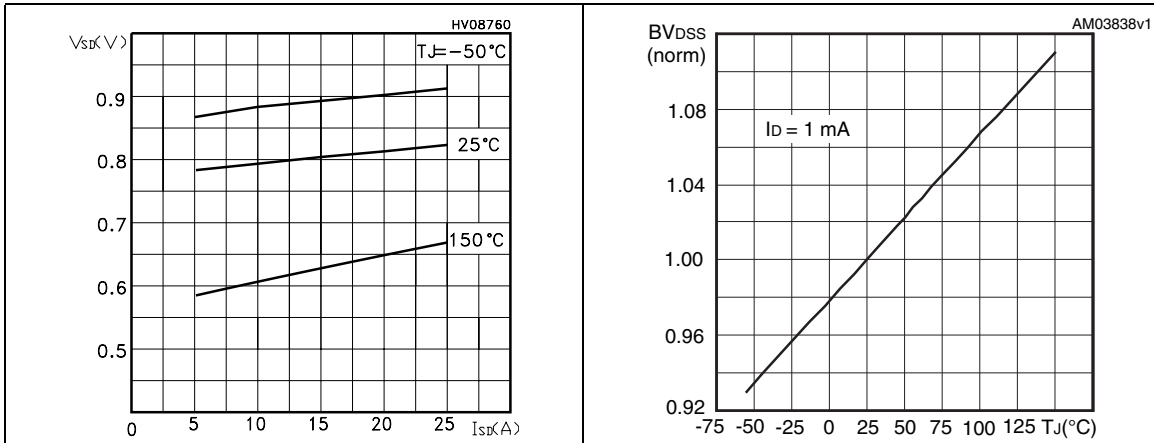


Figure 12. Source-drain diode forward characteristics Figure 13. Normalized  $B_{V_{DS}}$  vs temperature



### 3 Test circuits

Figure 14. Switching times test circuit for resistive load

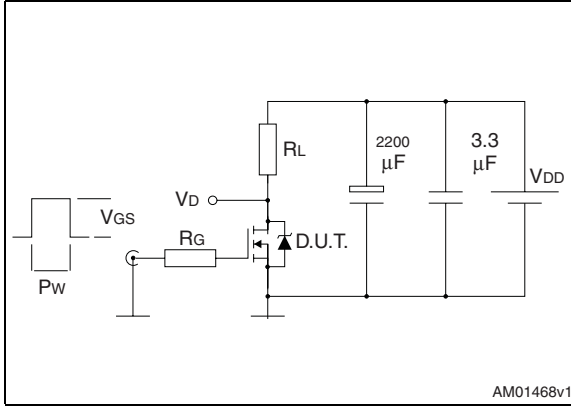


Figure 15. Gate charge test circuit

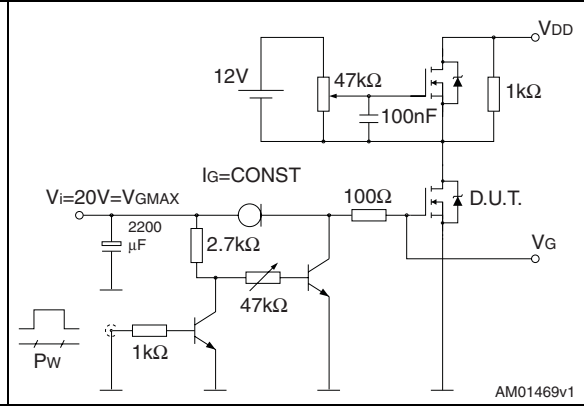


Figure 16. Test circuit for inductive load switching and diode recovery times

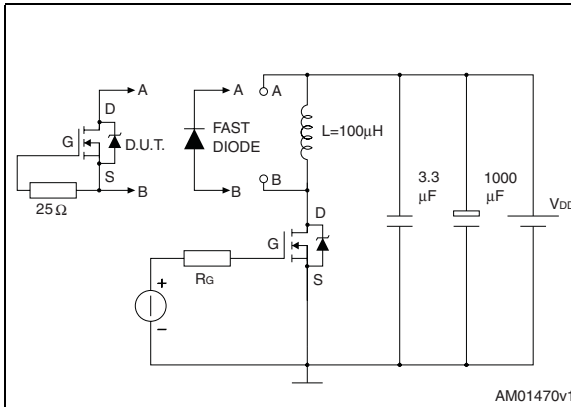


Figure 17. Unclamped inductive load test circuit

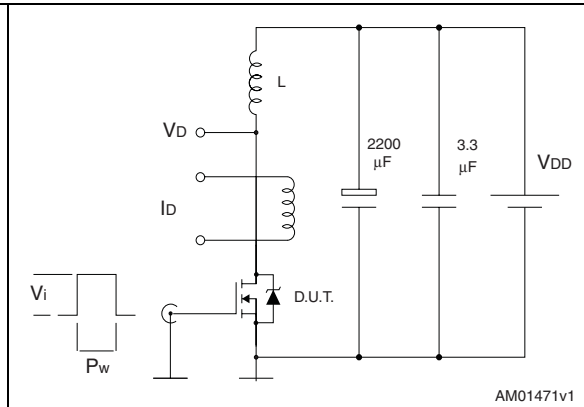


Figure 18. Unclamped inductive waveform

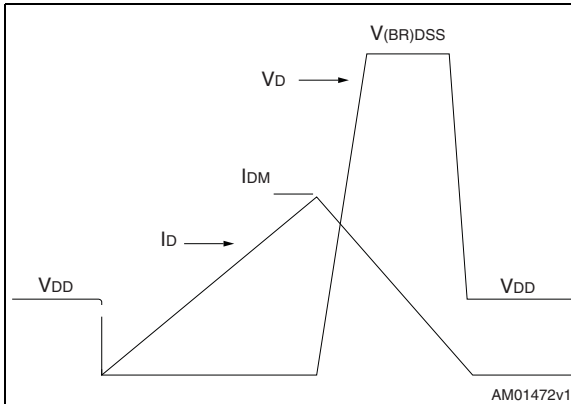
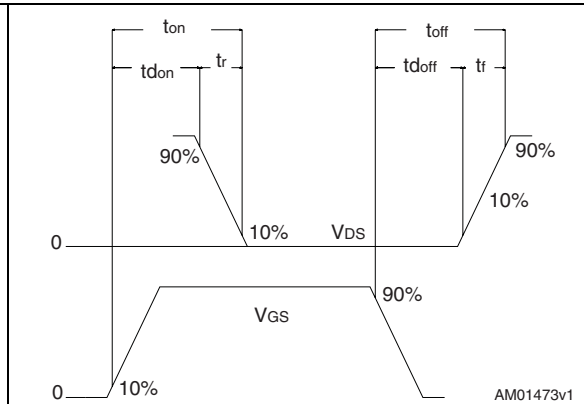


Figure 19. Switching time waveform



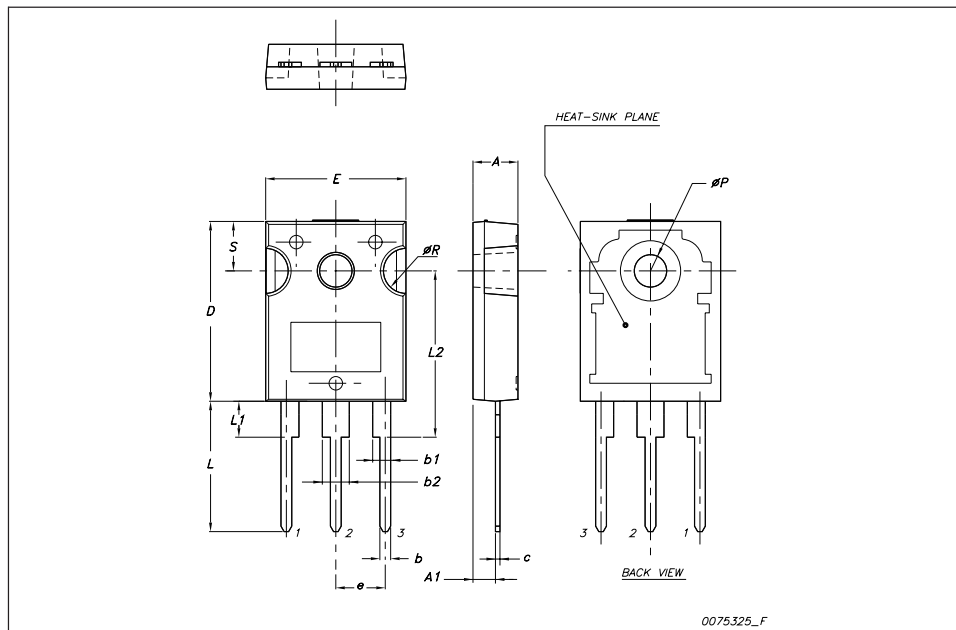


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**TO-247 mechanical data**

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



## 5 Revision history

Table 10. Document revision history

Date	Revision	Changes
24-Jun-2004	9	New stylesheet.
07-Feb-2005	10	I <sub>D</sub> value changed
02-Oct-2009	11	Modified: test condition of $V_{(BR)DSS}$ in <a href="#">Table 5</a>

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