



# STW11NK90Z

N-channel 900V - 0.82Ω - 9.2A - TO-247  
Zener-protected SuperMESH™ Power MOSFET

## General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STW11NK90Z	900V	<0.98Ω	9.2A	200W

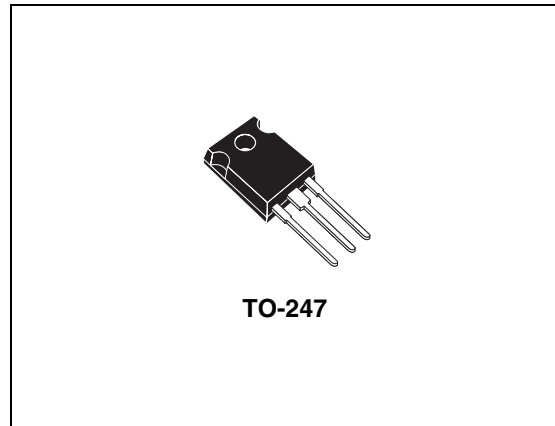
- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeability

## Description

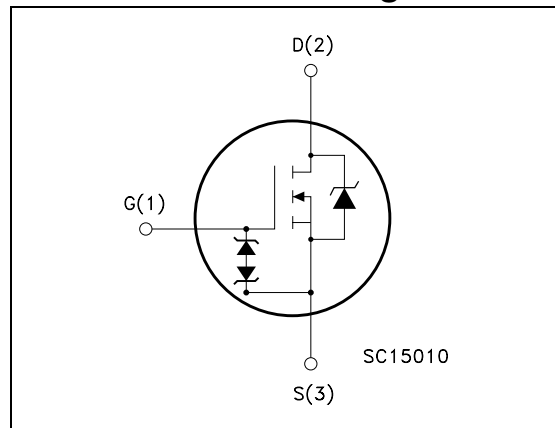
The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage Power MOSFETs including revolutionary MDmesh™ products

## Applications

- Switching application



## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STW11NK90Z	W11NK90Z	TO-247	Tube

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	5
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Revision history</b> .....	<b>11</b>

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	900	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20K\Omega$ )	900	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ C$	9.2	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ C$	5.8	A
$I_{DM}^{(1)}$	Drain current (pulsed)	36.8	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ C$	200	W
	Derating factor	1.51	W/ $^\circ C$
$V_{ESD(G-D)}$	Gate source ESD(HBM-C=100pF, R=1.5K $\Omega$ )	6000	V
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ C$

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 9.2A$ ,  $di/dt \leq 200A/\mu s$ ,  $V_{DD} = 80\%V_{(BR)DSS}$

**Table 2. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	0.66	$^\circ C/W$
$R_{thj-a}$	Thermal resistance junction-ambient Max	50	$^\circ C/W$
$T_l$	Maximum lead temperature for soldering purpose	300	$^\circ C$

**Table 3. Avalanche data**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ Max)	9.2	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25^\circ C$ , $I_d = I_{AR}$ , $V_{DD} = 50V$ )	400	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1mA, V_{GS} = 0$	900			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 50	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 10$	$\mu A$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 4.6A$		0.82	0.98	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 4.6A$		11		S
$C_{iss}$	Input capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		3000		pF
$C_{oss}$	Output capacitance			240		pF
$C_{rss}$	Reverse transfer capacitance			48		pF
$C_{oss \text{ eq}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0V \text{ to } 720V$		83		pF
$Q_g$	Total gate charge	$V_{DD} = 720V, I_D = 9.2A$		95	115	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10V$		14		nC
$Q_{gd}$	Gate-drain charge	(see Figure 14)		49		nC

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

2.  $C_{oss \text{ eq}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 450V, I_D = 4.6A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 13)		30		ns	
$t_r$	Rise time			19		ns	
$t_{d(off)}$	Turn-off delay time				76		ns
$t_f$	Fall time				50		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				9.2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				36.8	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=9.2A, V_{GS}=0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=9.2A,$ $di/dt = 100A/\mu s,$ $V_{DD}=50V, T_j=25^\circ C$ <i>(see Figure 18)</i>		584 6 21		ns $\mu C$ A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=9.2A,$ $di/dt = 100A/\mu s,$ $V_{DD}=50V, T_j=150^\circ C$ <i>(see Figure 18)</i>		790 8.7 22		ns $\mu C$ A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

**Table 8. Gate-source zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{GS}=\pm 1mA$ (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

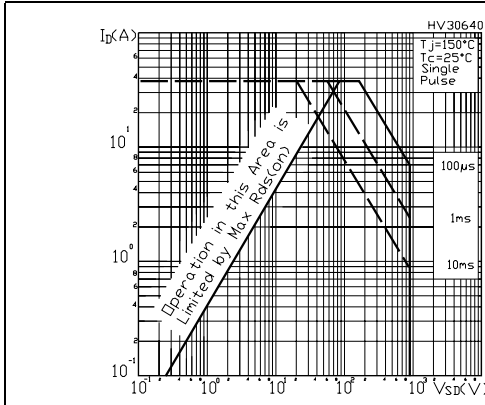


Figure 2. Thermal impedance

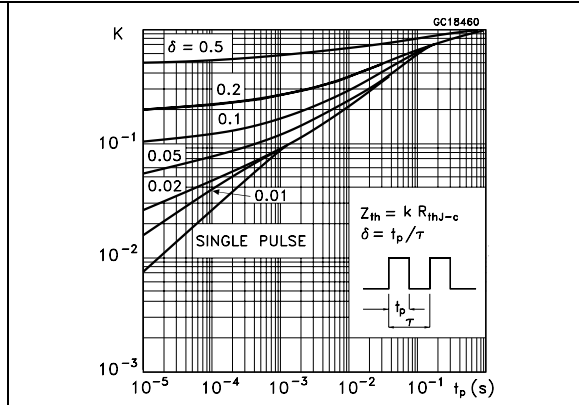


Figure 3. Output characteristics

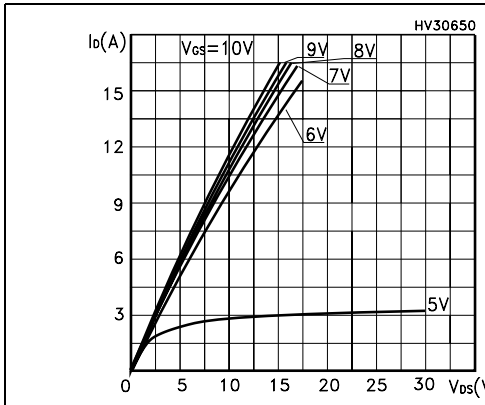


Figure 4. Transfer characteristics

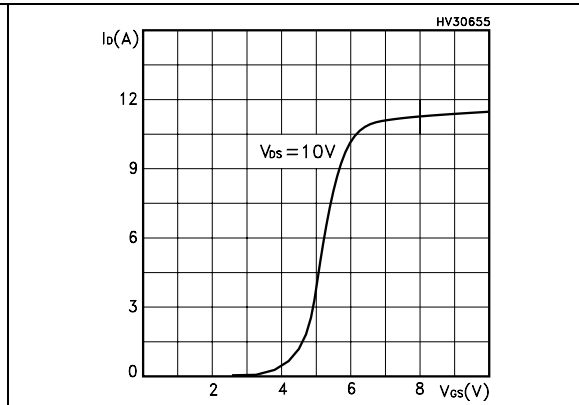


Figure 5. Normalized  $B_{V_{DS}}$  vs temperature

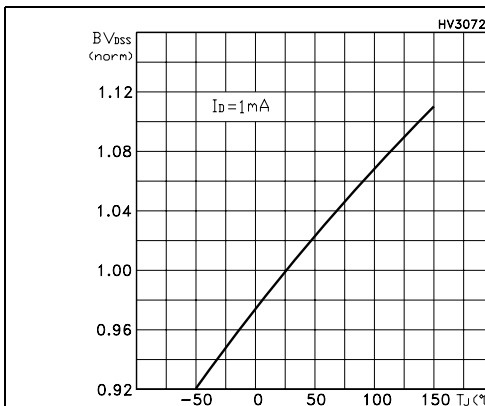


Figure 6. Static drain-source on resistance

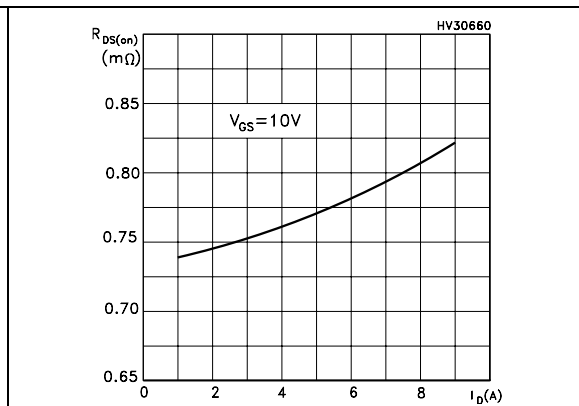


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

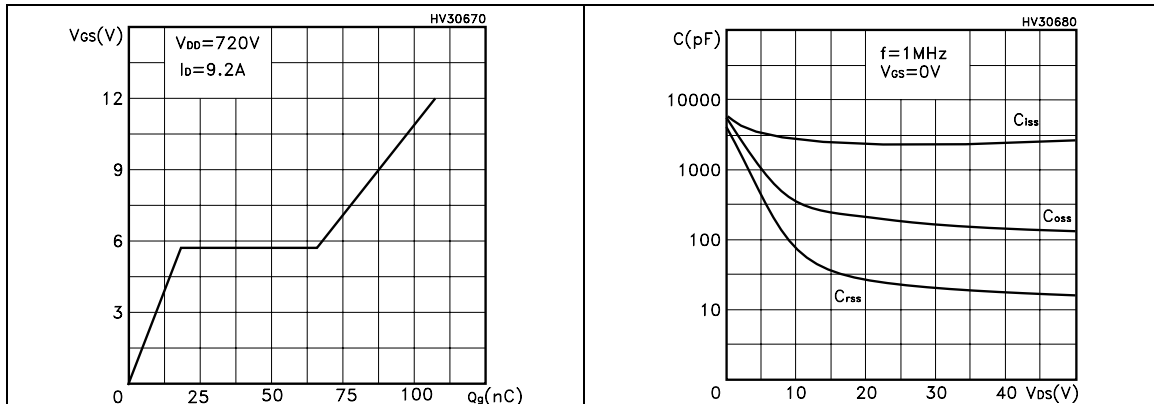


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

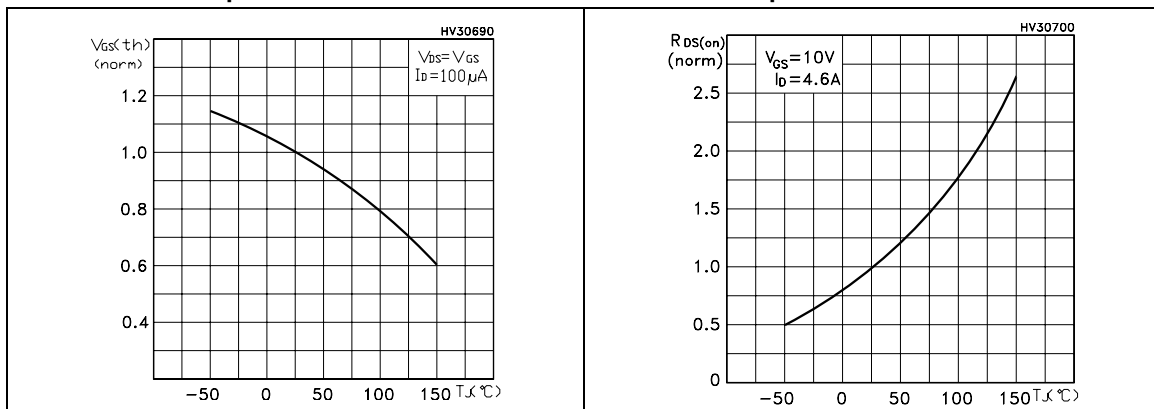
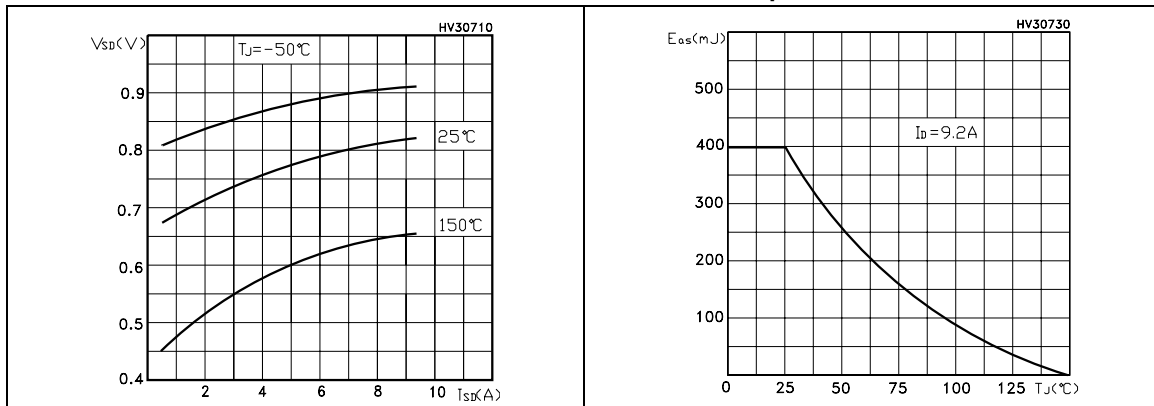


Figure 11. Source-drain diode forward characteristics Figure 12. Maximum avalanche energy vs temperature



### 3 Test circuits

Figure 13. Switching times test circuit for resistive load

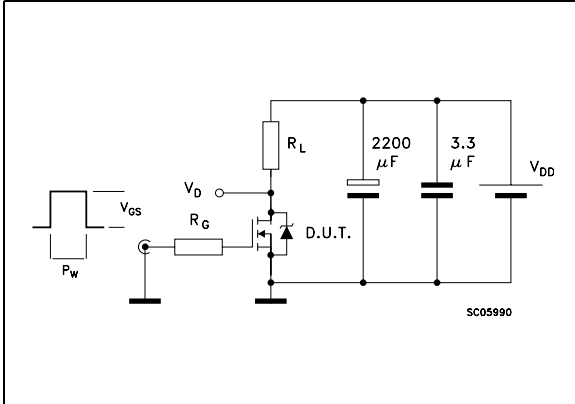


Figure 14. Gate charge test circuit

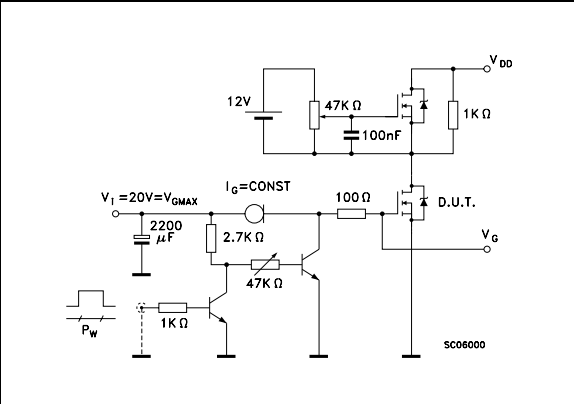


Figure 15. Test circuit for inductive load switching and diode recovery times

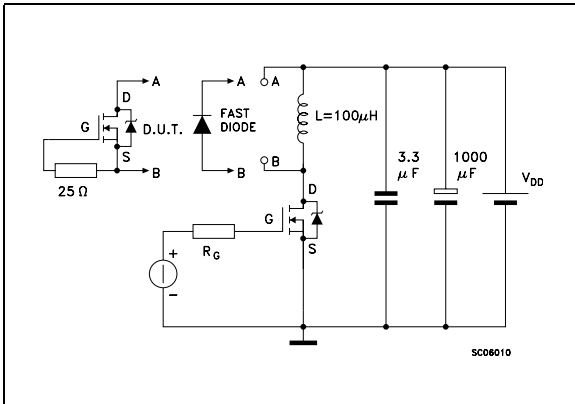


Figure 16. Unclamped Inductive load test circuit

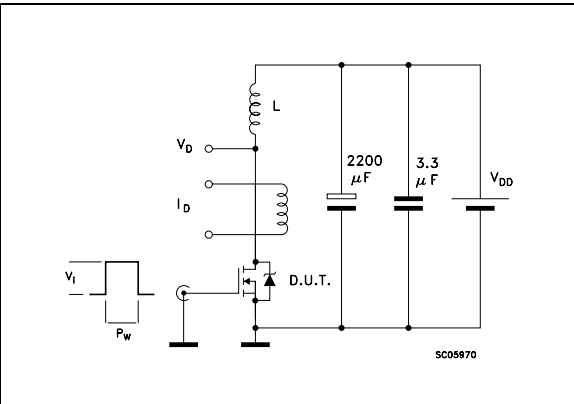


Figure 17. Unclamped inductive waveform

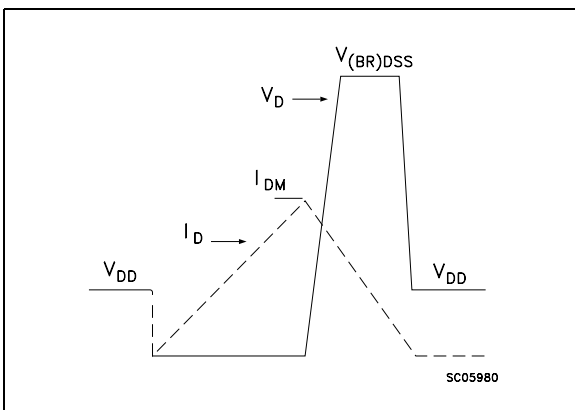
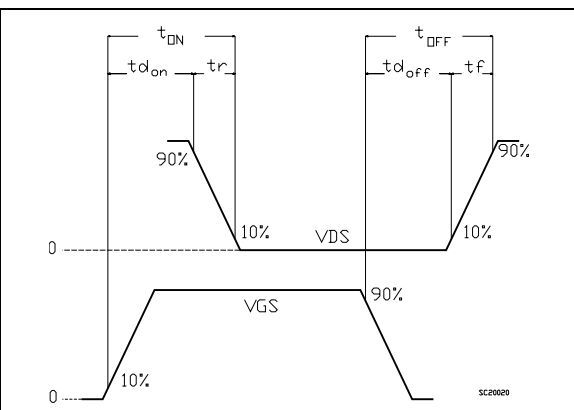


Figure 18. Switching time waveform



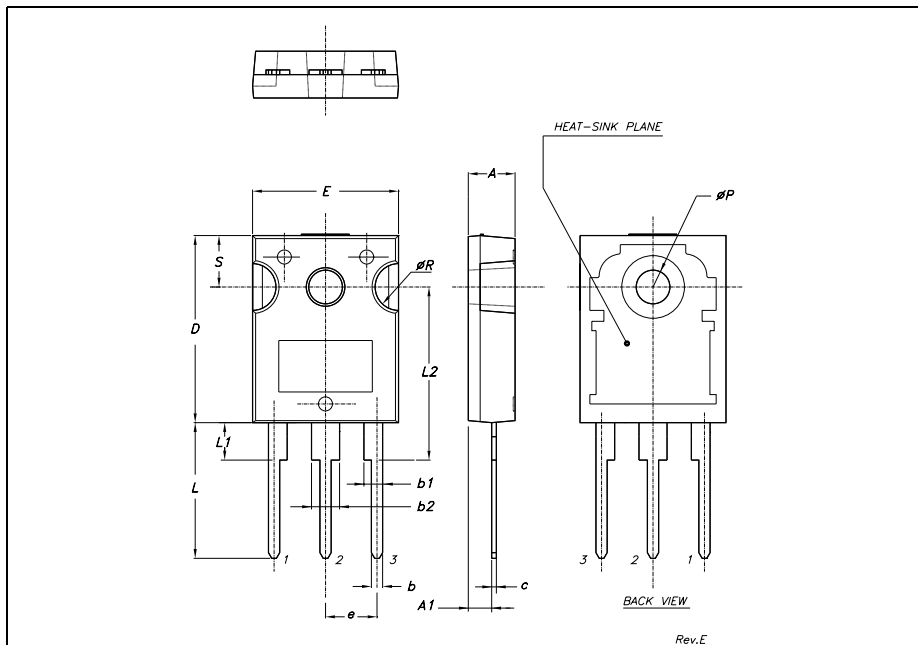


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : [www.st.com](http://www.st.com)

**TO-247 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



## 5 Revision history

Table 9. Revision history

Date	Revision	Changes
30-Mar-2006	1	First release
25-Jul-2006	2	Modified value on <i>Avalanche data</i>

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