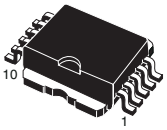
STV250N55F3

N-channel 55 V, 1.5 mΩ, 250 A, PowerSO-10 STripFET™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STV250N55F3	55 V	< 2.2 mΩ	250 A

- Conduction losses reduced
- Low profile, very low parasitic inductance



PowerSO-10

Application

- Switching applications

Description

This n-channel enhancement mode Power MOSFET is the latest refinement of STMicroelectronics unique “single feature size” strip-based process with less critical alignment steps and therefore a remarkable manufacturing reproducibility. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and low gate charge.

Figure 1. Internal schematic diagram and connection diagram (top view)

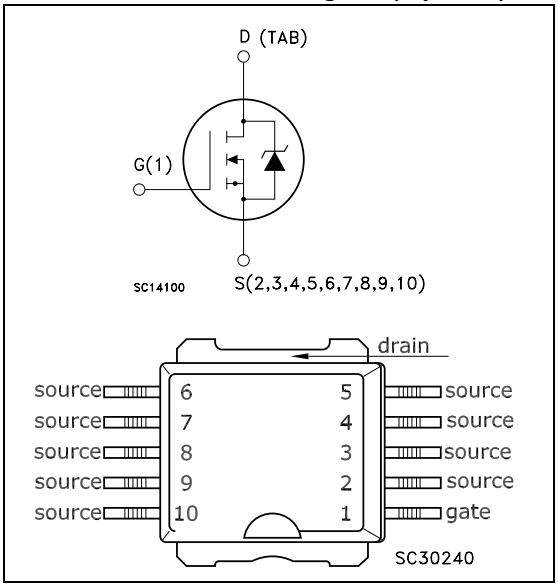


Table 1. Device summary

Order code	Marking	Package	Packaging
STV250N55F3	250N55F3	PowerSO-10	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	55	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25 °C	250	A
I_D	Drain current (continuous) at T_C = 100 °C	175	A
I_{DM} (1)	Drain current (pulsed)	1000	A
P_{TOT} (2)	Total dissipation at T_C = 25 °C	300	W
	Derating factor	2.0	W/°C
E_{AS} (3)	Single pulse avalanche energy	1	J
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Operating junction temperature		

1. Pulse width limited by safe operating area
2. This value is rated according to Rthj-c
3. Starting Tj = 25 °C, I_D = 60 A, V_{DD} = 35 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max.	0.5	°C/W
Rthj-pcb(1)	Thermal resistance junction-pcb max.	50	°C/W

1. When mounted on 1 inch^2 FR-4 2 oz Cu

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	55			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating, T_c = 125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{DS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 75 A		1.5	2.2	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		6800 1450 15		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 44 V, I_D = 120 A, V_{GS} = 10 V *Figure 14*		100 30 26		nC nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 27.5 V, I_D = 60 A R_G = 4.7 Ω, V_{GS} = 10 V, *Figure 13*		25 150		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD} = 27.5 V, I_D = 60 A R_G = 4.7 Ω, V_{GS} = 10 V, *Figure 13*		110 50		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SD} (1)	Source-drain current Source-drain current (pulsed)				250 1000	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 120 A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 120 A, di/dt = 100 A/µs V_{DD} = 35 V, T_j = 150 °C *Figure 18*		60 110 3.5		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

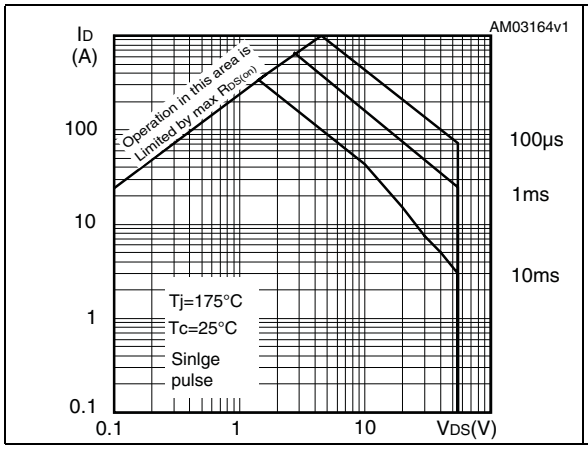


Figure 3. Thermal impedance

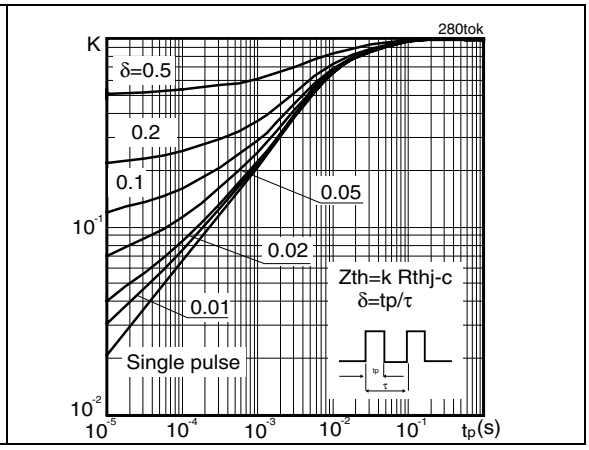


Figure 4. Output characteristics

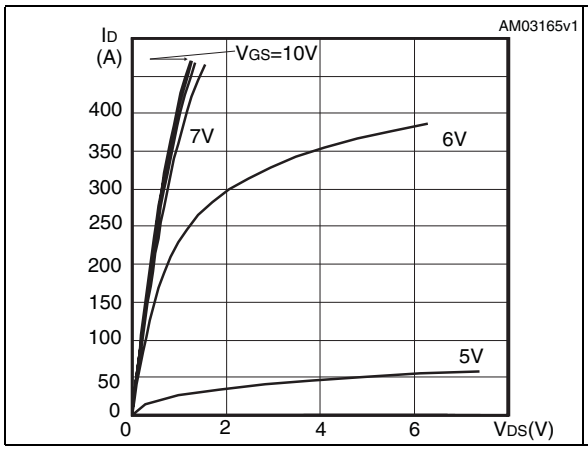


Figure 5. Transfer characteristics

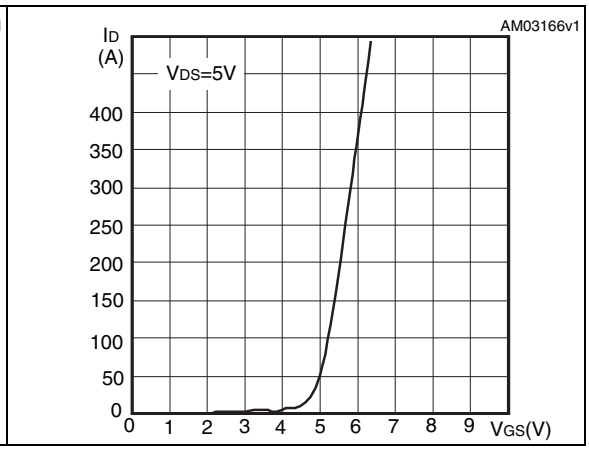


Figure 6. Normalized B_{VDSS} vs temperature

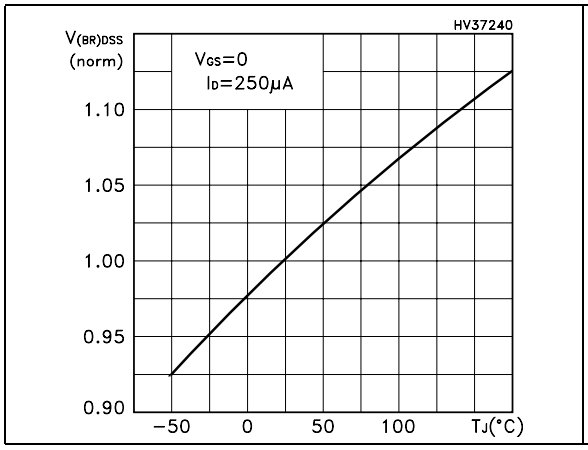


Figure 7. Static drain-source on resistance

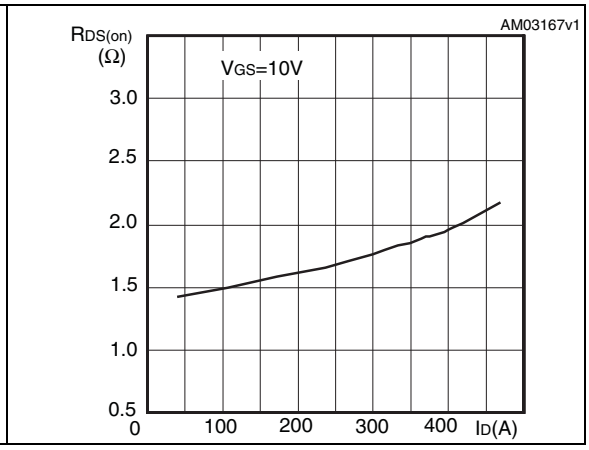


Figure 8. Gate charge vs gate-source voltage

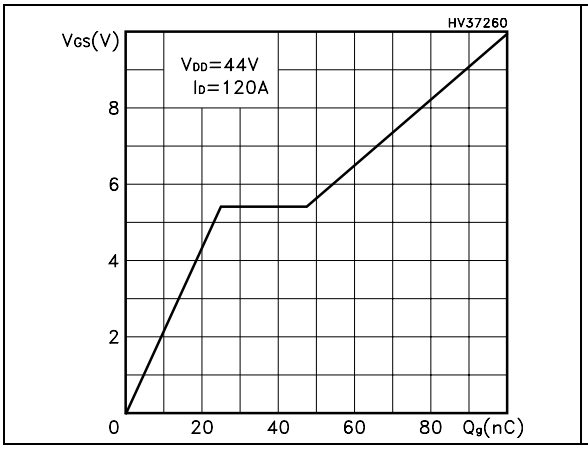


Figure 9. Capacitance variations

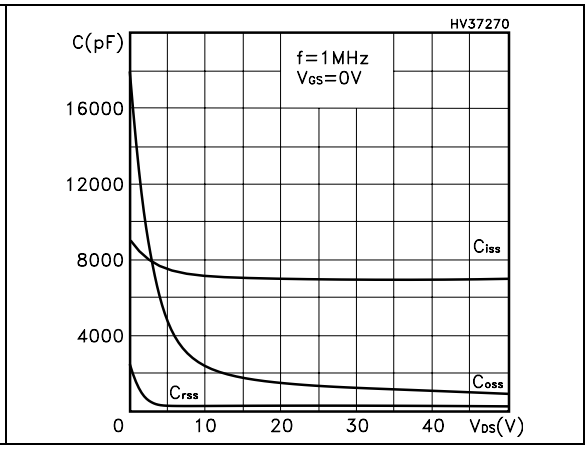


Figure 10. Normalized gate threshold voltage vs temperature

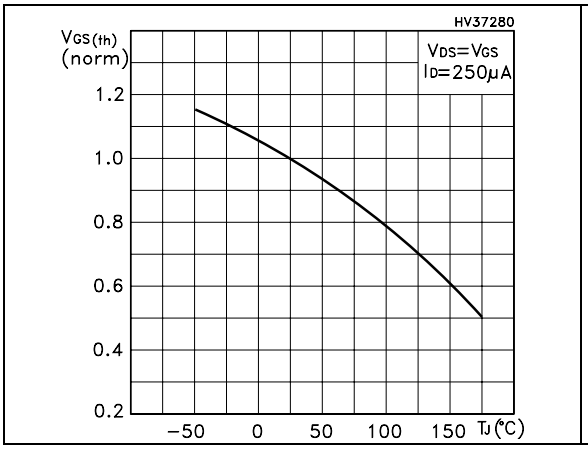


Figure 11. Normalized on resistance vs temperature

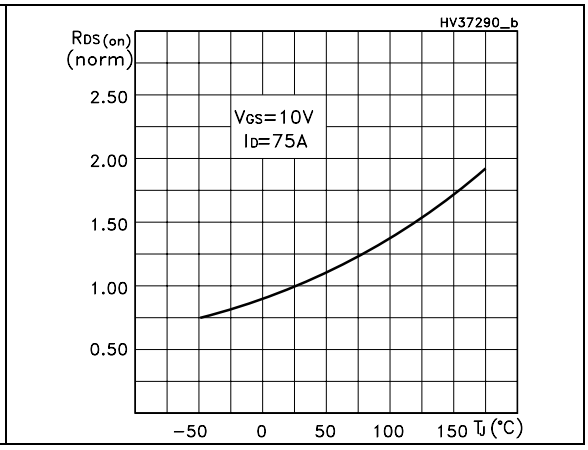
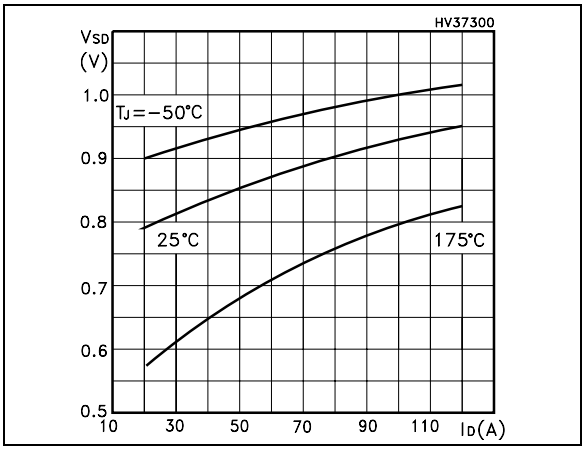


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

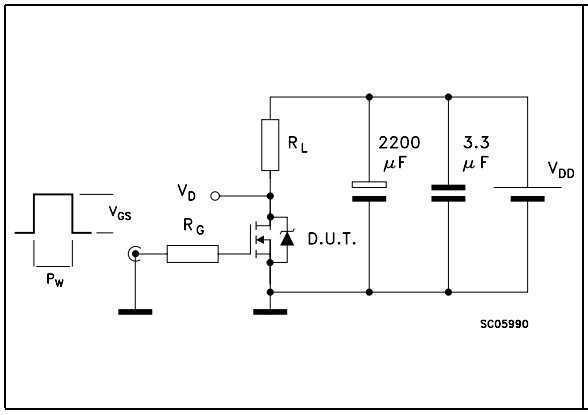


Figure 14. Gate charge test circuit

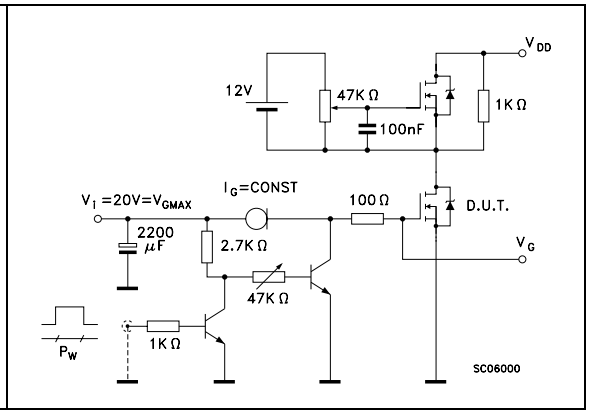


Figure 15. Test circuit for inductive load switching and diode recovery times

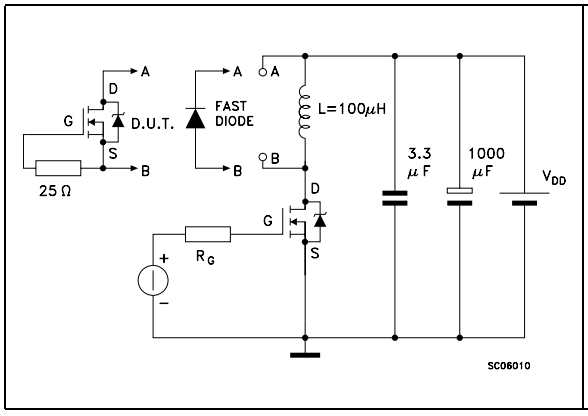


Figure 16. Unclamped inductive load test circuit

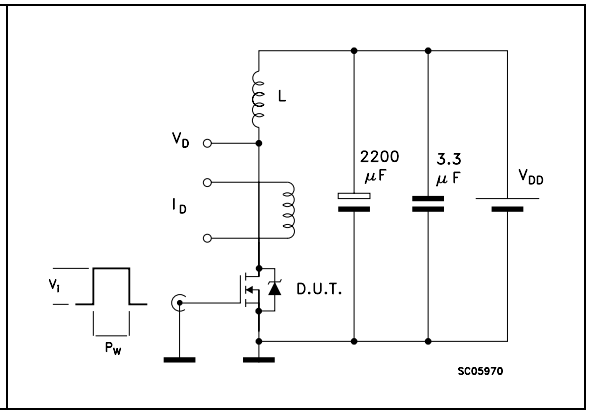


Figure 17. Unclamped inductive waveform

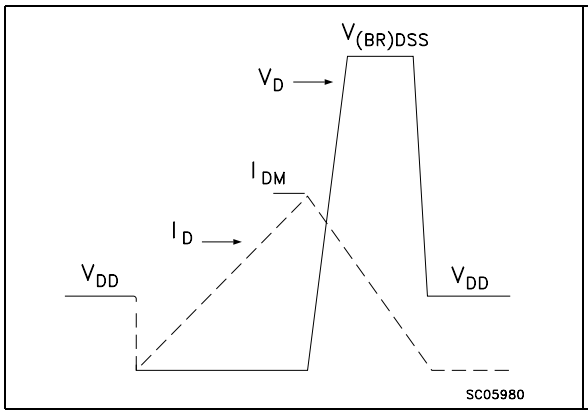
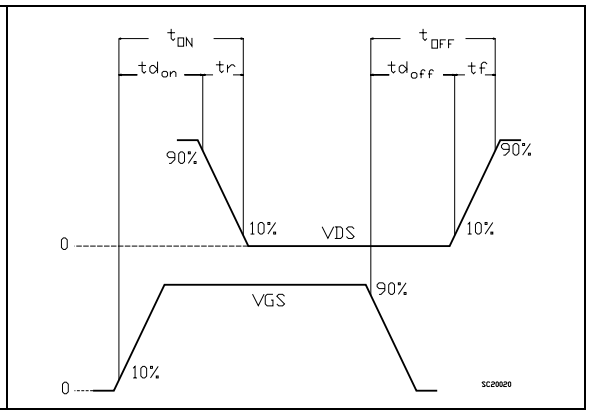


Figure 18. Switching time waveform

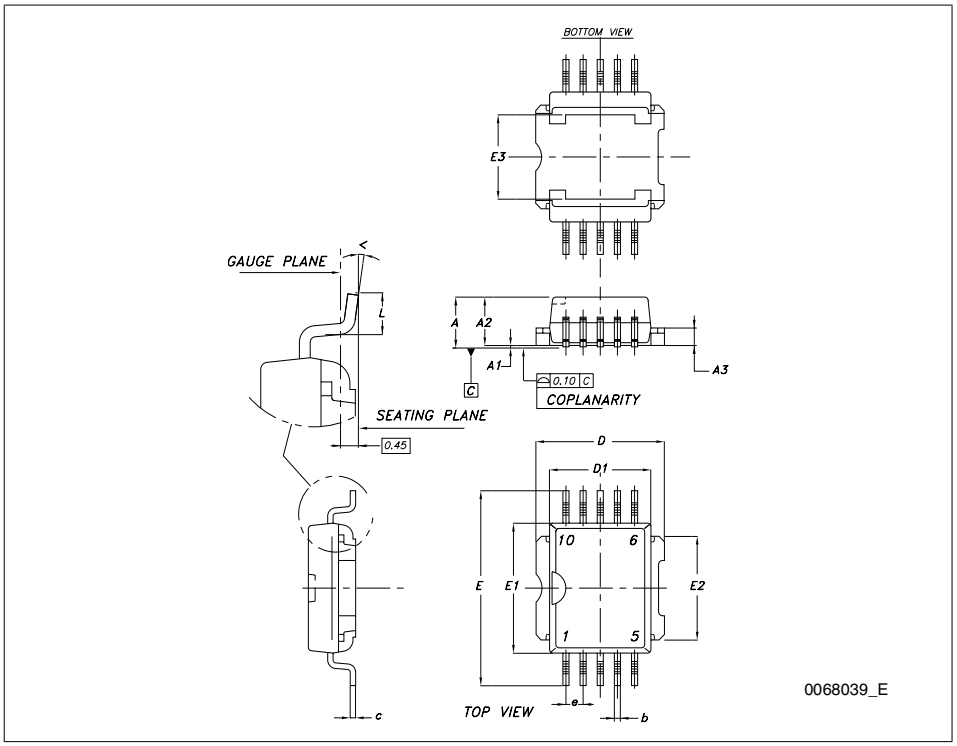


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

PowerSO-10 mechanical data

Dim	mm		
	Min	Typ	Max
A			3.70
A1	0.00		0.10
A2	3.40		3.60
A3	1.25		1.35
b	0.40		0.53
c	0.35		0.55
D	9.40		9.60
D1	7.40		7.60
E	13.80		14.40
E1	9.30		9.50
E2	7.20		7.60
E3	5.90		6.10
e		1.27	
L	0.95		1.65
<	0°		8°



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
25-Oct-2007	1	Initial release
20-Mar-2008	2	Content reworked to improve readability, no technical changes.
10-Nov-2008	3	Document status promoted from preliminary data to datasheet.
02-Mar-2009	4	*Figure 2* has been updated.

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