

# Trench Gate Power MOSFET

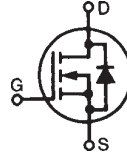
**IXTH200N075T**  
**IXTQ200N075T**

$$V_{DSS} = 75 \text{ V}$$

$$I_{D25} = 200 \text{ A}$$

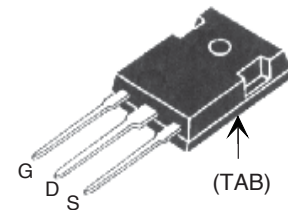
$$R_{DS(on)} \leq 5.0 \text{ m}\Omega$$

N-Channel Enhancement Mode  
Avalanche Rated

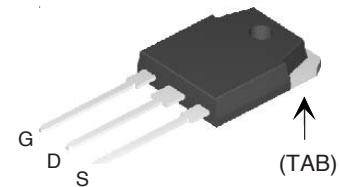


Symbol	Test Conditions	Maximum Ratings	
$V_{DSS}$	$T_J = 25^\circ\text{C}$ to $175^\circ\text{C}$	75	V
$V_{DGR}$	$T_J = 25^\circ\text{C}$ to $175^\circ\text{C}$ ; $R_{GS} = 1 \text{ M}\Omega$	75	V
$V_{GSM}$	Transient	$\pm 20$	V
$I_{D25}$	$T_C = 25^\circ\text{C}$	200	A
$I_{LRMS}$	Lead Current Limit, RMS	75	A
$I_{DM}$	$T_C = 25^\circ\text{C}$ , pulse width limited by $T_{JM}$	540	A
$I_{AR}$	$T_C = 25^\circ\text{C}$	25	A
$E_{AS}$	$T_C = 25^\circ\text{C}$	750	mJ
$dv/dt$	$I_S \leq I_{DM}$ , $di/dt \leq 100 \text{ A}/\mu\text{s}$ , $V_{DD} \leq V_{DSS}$ $T_J \leq 175^\circ\text{C}$ , $R_G = 5 \Omega$	3	V/ns
$P_D$	$T_C = 25^\circ\text{C}$	430	W
$T_J$		-55 ... +175	$^\circ\text{C}$
$T_{JM}$		175	$^\circ\text{C}$
$T_{stg}$		-55 ... +175	$^\circ\text{C}$
$T_L$	1.6 mm (0.062 in.) from case for 10 s	300	$^\circ\text{C}$
$T_{SOLD}$	Plastic body for 10 seconds	260	$^\circ\text{C}$
$M_d$	Mounting torque	1.13 / 10	Nm/lb.in.
Weight	TO-3P	5.5	g
	TO-247	6	g

TO-247 (IXTH)



TO-3P (IXTQ)



G = Gate      D = Drain  
S = Source      TAB = Drain

### Features

- International standard packages
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect

### Advantages

- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{DSS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$	75		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$	2.0		V
$I_{GSS}$	$V_{GS} = \pm 20 \text{ V}$ , $V_{DS} = 0 \text{ V}$			$\pm 200 \text{ nA}$
$I_{DSS}$	$V_{DS} = V_{DSS}$ $V_{GS} = 0 \text{ V}$ $T_J = 150^\circ\text{C}$			5 $\mu\text{A}$ 250 $\mu\text{A}$
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$ , $I_D = 25 \text{ A}$ , Notes 1, 2	4.0	5.0	m $\Omega$

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
<i>(T<sub>J</sub> = 25°C unless otherwise specified)</i>				
<b>g<sub>fs</sub></b>	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 60 A, Note 1	70	110	S
<b>C<sub>iss</sub></b>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz	6800		pF
<b>C<sub>oss</sub></b>		1040		pF
<b>C<sub>rss</sub></b>		190		pF
<b>t<sub>d(on)</sub></b>	<b>Resistive Switching Times</b>	31		ns
<b>t<sub>r</sub></b>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 0.5 V <sub>DSS</sub> , I <sub>D</sub> = 25 A	57		ns
<b>t<sub>d(off)</sub></b>	R <sub>G</sub> = 5 Ω (External)	54		ns
<b>t<sub>f</sub></b>		52		ns
<b>Q<sub>g(on)</sub></b>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 0.5 V <sub>DSS</sub> , I <sub>D</sub> = 25 A	160		nC
<b>Q<sub>gs</sub></b>		35		nC
<b>Q<sub>gd</sub></b>		43		nC
<b>R<sub>thJC</sub></b>				0.35 °C/W
<b>R<sub>thCH</sub></b>	TO-3P	0.25		°C/W
	TO-247	0.21		°C/W

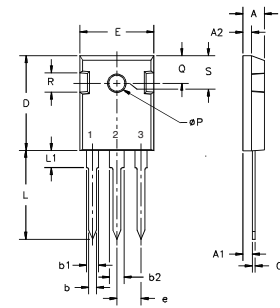
**Source-Drain Diode**

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
<i>T<sub>J</sub> = 25°C unless otherwise specified)</i>				
<b>I<sub>S</sub></b>	V <sub>GS</sub> = 0 V			200 A
<b>I<sub>SM</sub></b>	Pulse width limited by T <sub>JM</sub>			540 A
<b>V<sub>SD</sub></b>	I <sub>F</sub> = 25 A, V <sub>GS</sub> = 0 V, Note 1			1.0 V
<b>t<sub>rr</sub></b>	I <sub>F</sub> = 25 A, -di/dt = 100 A/μs	50		ns
	V <sub>R</sub> = 40 V, V <sub>GS</sub> = 0 V			

- Notes: 1. Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %;  
 2. On through-hole packages, R<sub>DS(on)</sub> Kelvin test contact location must be 5 mm or less from the package body.

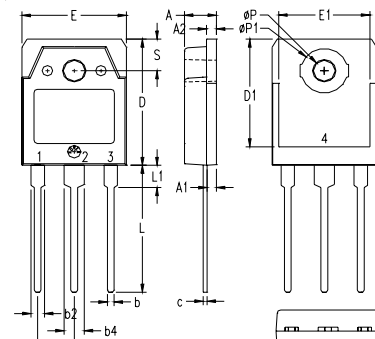
**PRELIMINARY TECHNICAL INFORMATION**

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

**TO-247 AD Outline**


Terminals: 1 - Gate 2 - Drain  
 3 - Source Tab - Drain

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.7	5.3	.185	.209
A <sub>1</sub>	2.2	2.54	.087	.102
A <sub>2</sub>	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b <sub>1</sub>	1.65	2.13	.065	.084
b <sub>2</sub>	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
ØP	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15 BSC		242 BSC	

**TO-3P (IXTQ) Outline**


Pins: 1 - Gate 2 - Drain  
 3 - Source 4, TAB - Drain

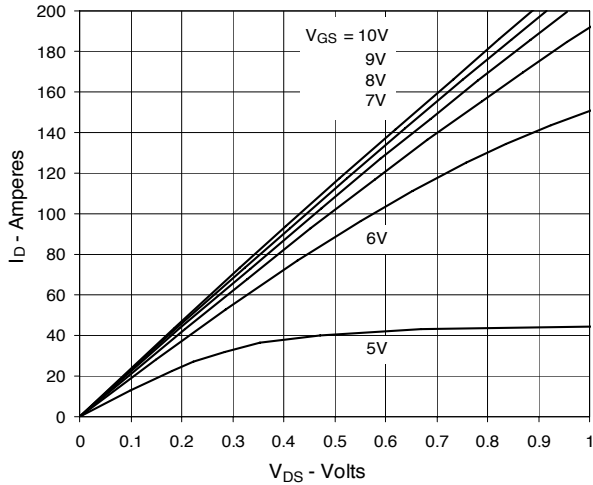
SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.193	4.70	4.90
A1	.051	.059	1.30	1.50
A2	.057	.065	1.45	1.65
b	.035	.045	0.90	1.15
b2	.075	.087	1.90	2.20
b4	.114	.126	2.90	3.20
c	.022	.031	0.55	0.80
D	.780	.791	19.80	20.10
D1	.665	.677	16.90	17.20
E	.610	.622	15.50	15.80
E1	.531	.539	13.50	13.70
e	.215 BSC		5.45 BSC	
L	.779	.795	19.80	20.20
L1	.134	.142	3.40	3.60
ØP	.126	.134	3.20	3.40
ØP1	.272	.280	6.90	7.10
S	.193	.201	4.90	5.10

All metal area are tin plated.

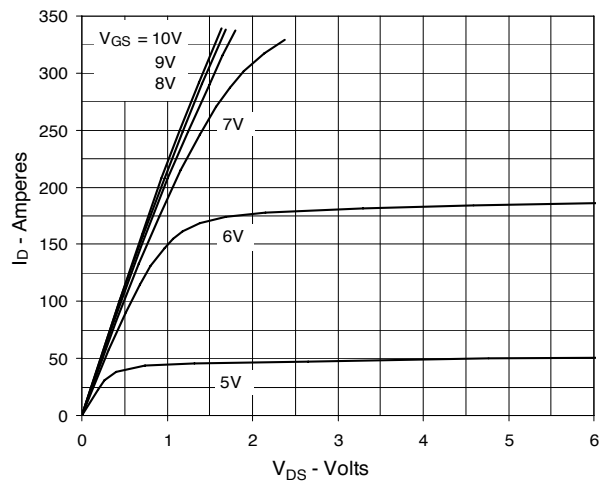
IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537

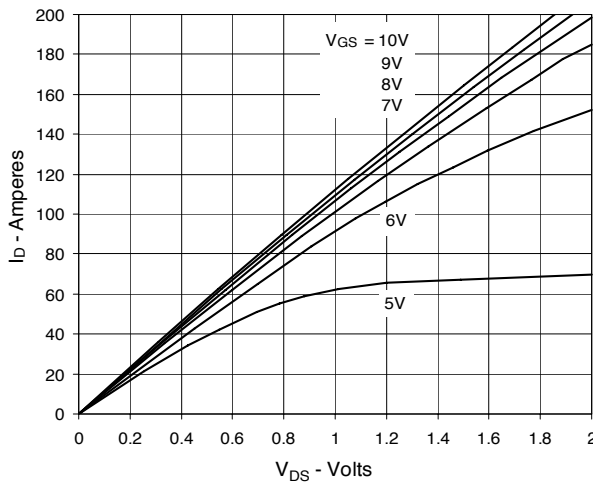
**Fig. 1. Output Characteristics @ 25°C**



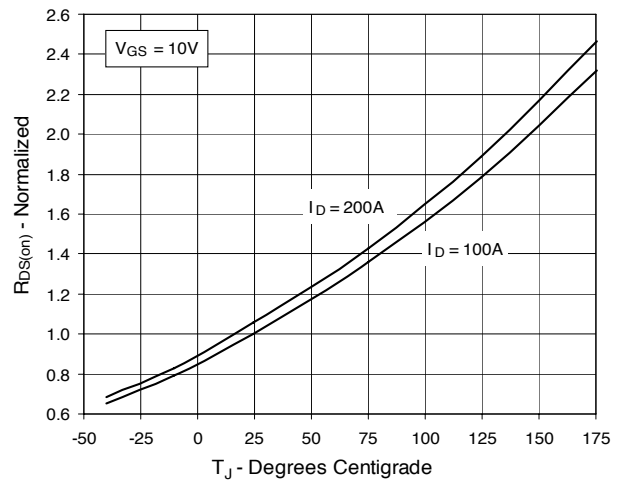
**Fig. 2. Extended Output Characteristics @ 25°C**



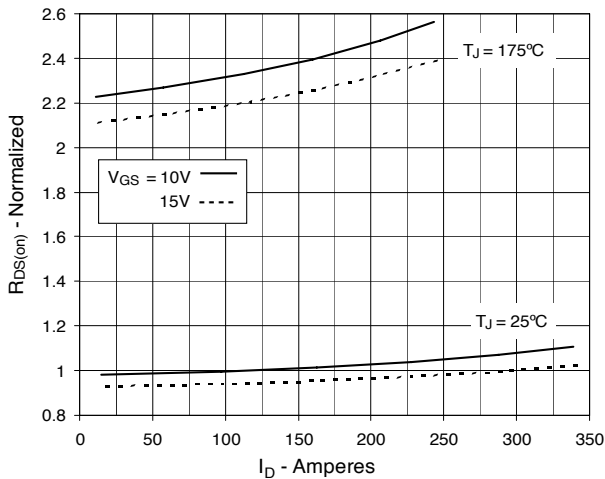
**Fig. 3. Output Characteristics @ 150°C**



**Fig. 4.  $R_{DS(on)}$  Normalized to  $I_D = 100A$  Value vs. Junction Temperature**



**Fig. 5.  $R_{DS(on)}$  Normalized to  $I_D = 100A$  Value vs. Drain Current**



**Fig. 6. Drain Current vs. Case Temperature**

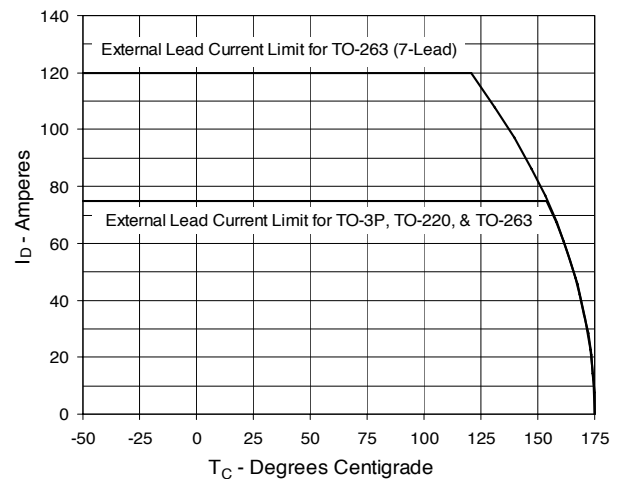


Fig. 7. Input Admittance

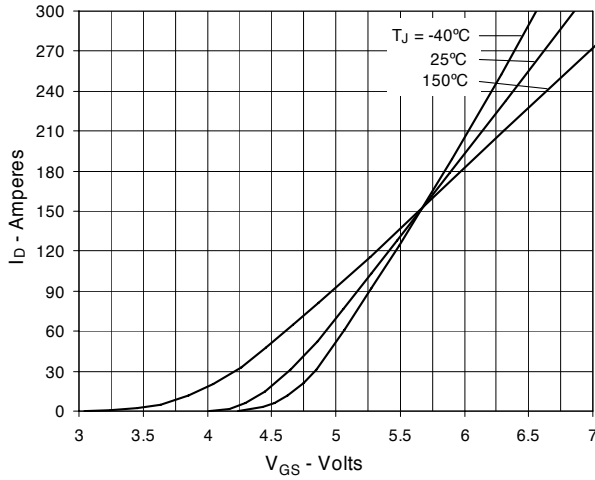


Fig. 8. Transconductance

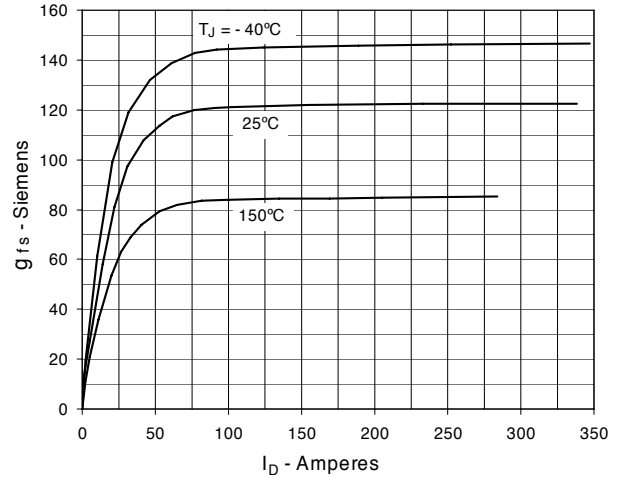


Fig. 9. Forward Voltage Drop of Intrinsic Diode

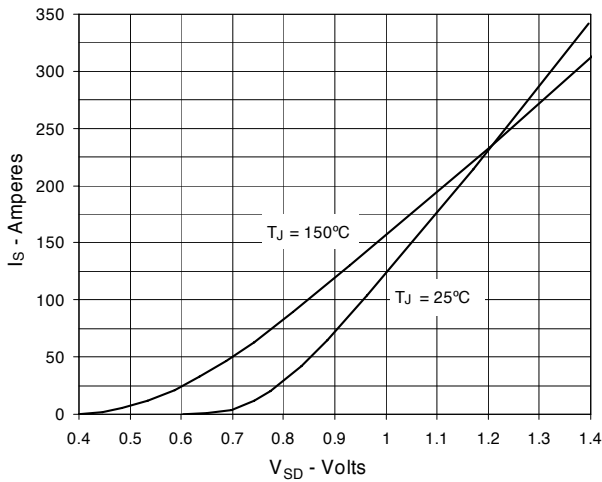


Fig. 10. Gate Charge

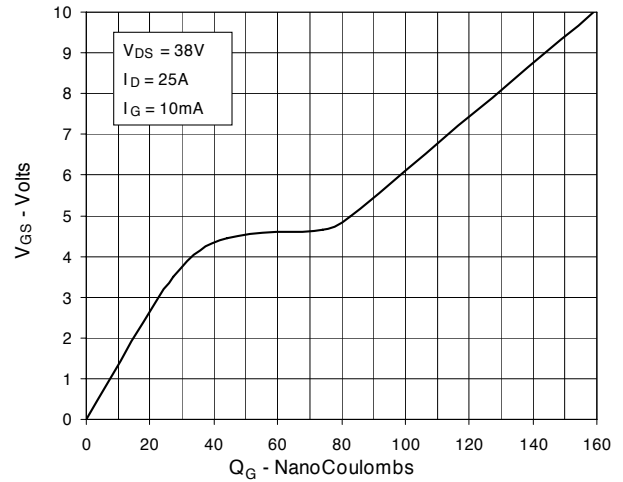


Fig. 11. Capacitance

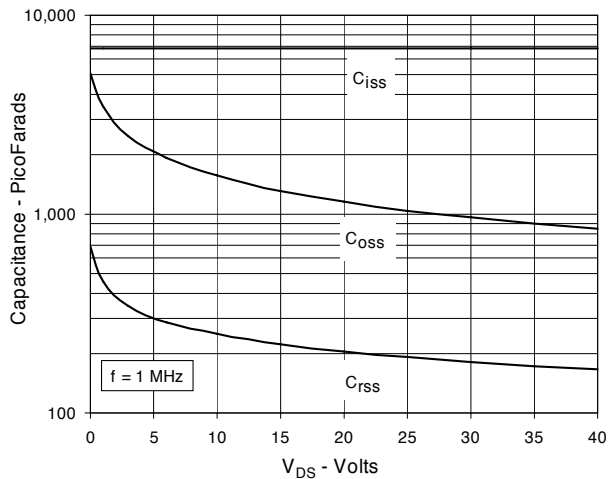
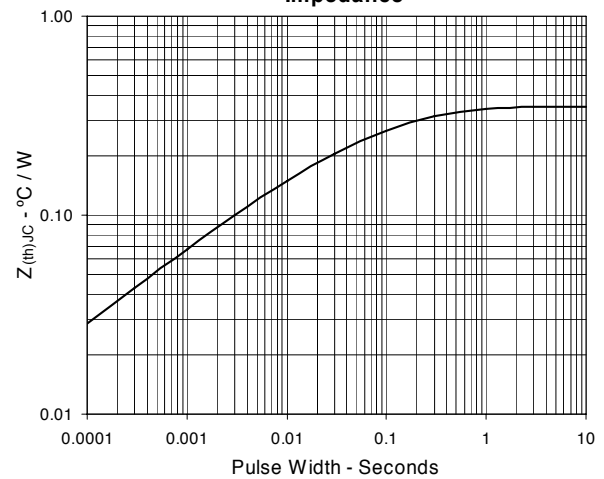
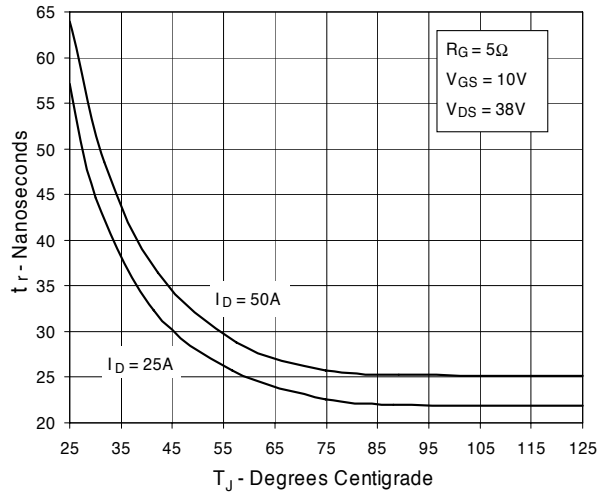


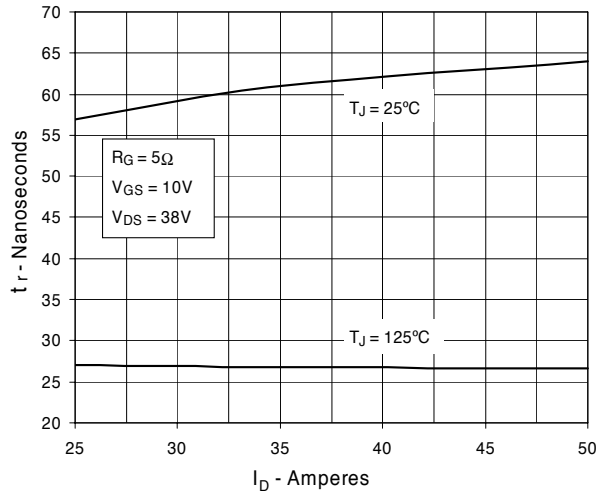
Fig. 12. Maximum Transient Thermal Impedance



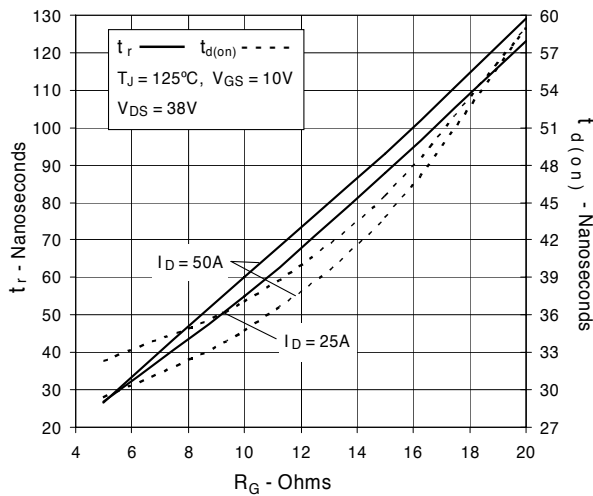
**Fig. 13. Resistive Turn-on  
Rise Time vs. Junction Temperature**



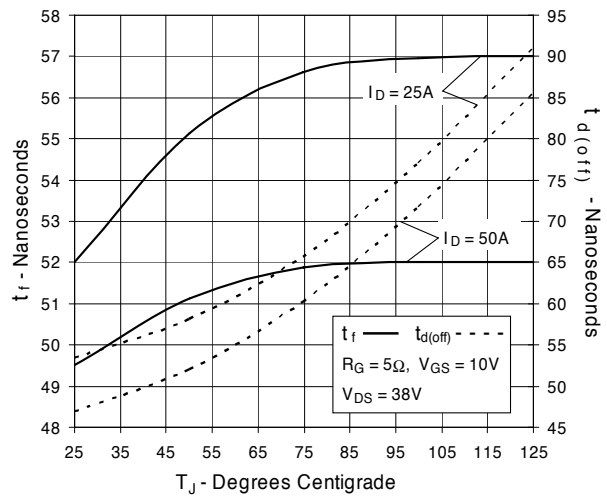
**Fig. 14. Resistive Turn-on  
Rise Time vs. Drain Current**



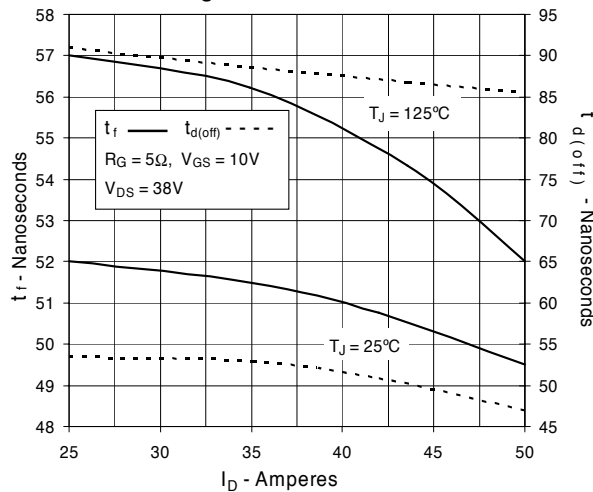
**Fig. 15. Resistive Turn-on  
Switching Times vs. Gate Resistance**



**Fig. 16. Resistive Turn-off  
Switching Times vs. Junction Temperature**



**Fig. 17. Resistive Turn-off  
Switching Times vs. Drain Current**



**Fig. 18. Resistive Turn-off  
Switching Times vs. Gate Resistance**

