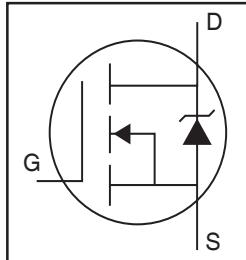


IRFB3306PbF
IRFS3306PbF
IRFSL3306PbF

HEXFET® Power MOSFET

Applications

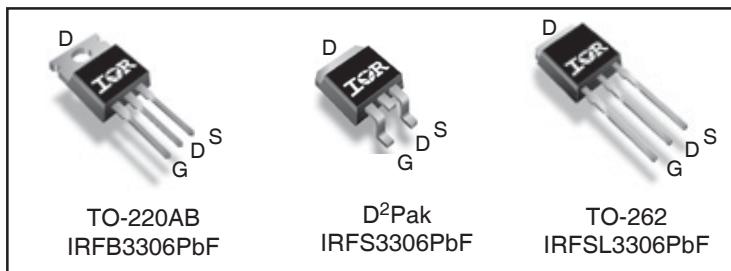
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



V_{DSS}	60V
R_{DS(on)}	typ. 3.3mΩ
	max. 4.2mΩ
I_D (Silicon Limited)	160A ①
I_D (Package Limited)	120A

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	160①	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	110①	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Wire Bond Limited)	120	
I _{DM}	Pulsed Drain Current ②	620	
P _D @ T _C = 25°C	Maximum Power Dissipation	230	W
	Linear Derating Factor	1.5	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	14	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

E _{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	184	mJ
I _{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b,	A
E _{AR}	Repetitive Avalanche Energy ⑤		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case ⑨	—	0.65	°C/W
R _{θCS}	Case-to-Sink, Flat Greased Surface , TO-220	0.50	—	
R _{θJA}	Junction-to-Ambient, TO-220 ⑩	—	62	
R _{θJA}	Junction-to-Ambient (PCB Mount) , D ² Pak ⑧⑨	—	40	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.07	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 5\text{mA}$ ②
$R_{DS(\text{on})}$	Static Drain-to-Source On-Resistance	—	3.3	4.2	m Ω	$V_{GS} = 10V, I_D = 75\text{A}$ ⑤
$V_{GS(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 150\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 60V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 48V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
R_G	Internal Gate Resistance	—	0.7	—	Ω	

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	230	—	—	S	$V_{DS} = 50V, I_D = 75\text{A}$
Q_g	Total Gate Charge	—	85	120	nC	$I_D = 75\text{A}$
Q_{gs}	Gate-to-Source Charge	—	20	—		$V_{DS} = 30V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	26	—		$V_{GS} = 10V$ ⑤
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	59	—		$I_D = 75\text{A}, V_{DS} = 0V, V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	$V_{DD} = 30V$
t_r	Rise Time	—	76	—		$I_D = 75\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	40	—		$R_G = 2.7\Omega$
t_f	Fall Time	—	77	—		$V_{GS} = 10V$ ⑤
C_{iss}	Input Capacitance	—	4520	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	500	—		$V_{DS} = 50V$
C_{rss}	Reverse Transfer Capacitance	—	250	—		$f = 1.0\text{MHz}$, See Fig. 5
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	720	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 48V$ ⑦, See Fig. 11
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)⑥	—	880	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 48V$ ⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_s	Continuous Source Current (Body Diode)	—	—	160①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	620	A	
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_s = 75\text{A}, V_{GS} = 0V$ ⑤
t_{rr}	Reverse Recovery Time	—	31	—	ns	$T_J = 25^\circ\text{C}$ $V_R = 51V$,
		—	35	—		$T_J = 125^\circ\text{C}$ $I_F = 75\text{A}$
Q_{rr}	Reverse Recovery Charge	—	34	—	nC	$T_J = 25^\circ\text{C}$ $\text{di}/\text{dt} = 100\text{A}/\mu\text{s}$ ⑤
		—	45	—		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	1.9	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by $T_{J\text{max}}$, starting $T_J = 25^\circ\text{C}$, $L = 0.04\text{mH}$ $R_G = 25\Omega$, $I_{AS} = 96\text{A}$, $V_{GS} = 10V$. Part not recommended for use above this value.

- ④ $I_{SD} \leq 75\text{A}$, $\text{di}/\text{dt} \leq 1400\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(\text{BR})\text{DSS}}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑥ $C_{oss \text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R_θ is measured at T_J approximately 90°C

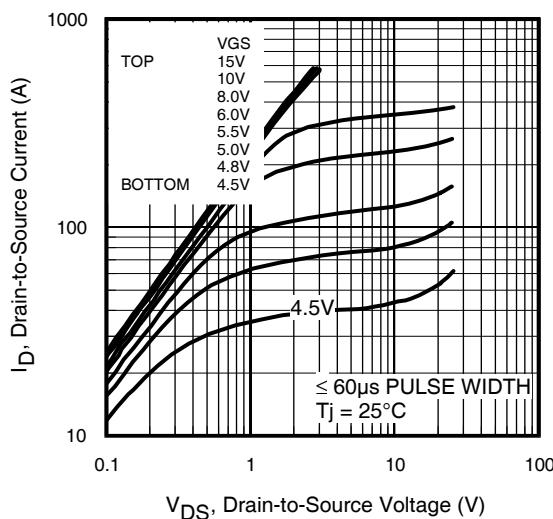


Fig 1. Typical Output Characteristics

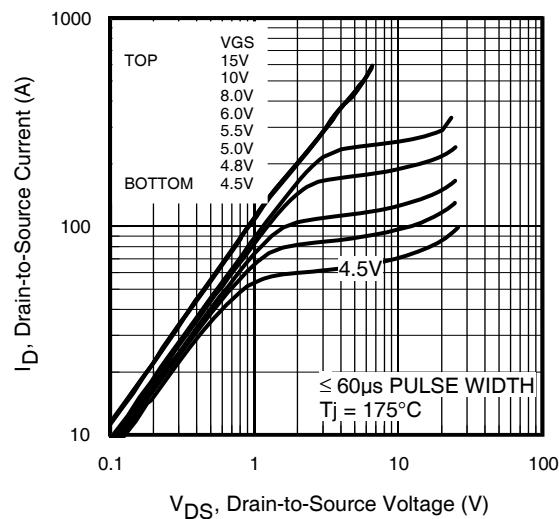


Fig 2. Typical Output Characteristics

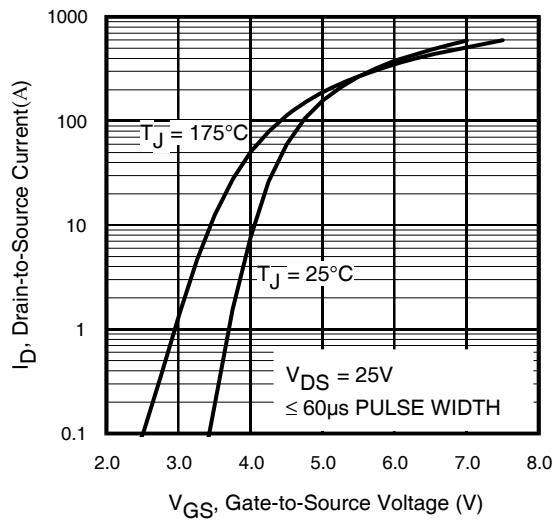


Fig 3. Typical Transfer Characteristics

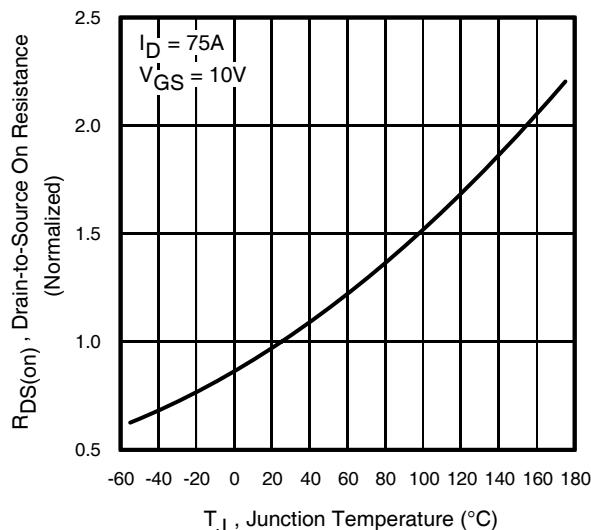


Fig 4. Normalized On-Resistance vs. Temperature

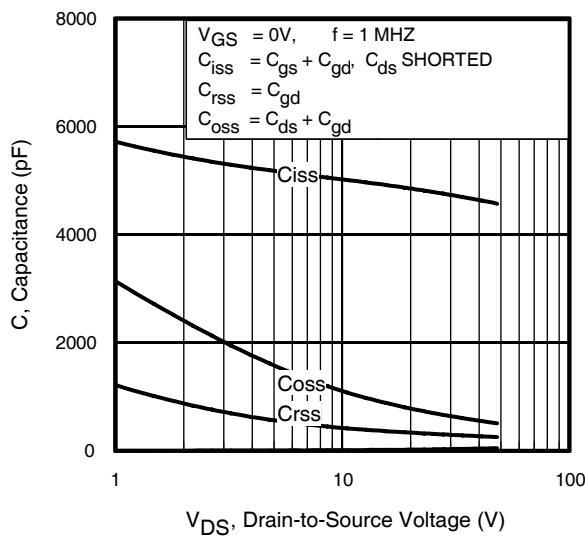


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

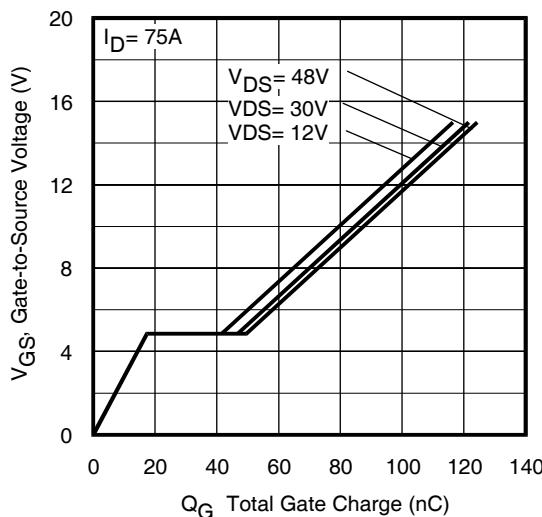


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

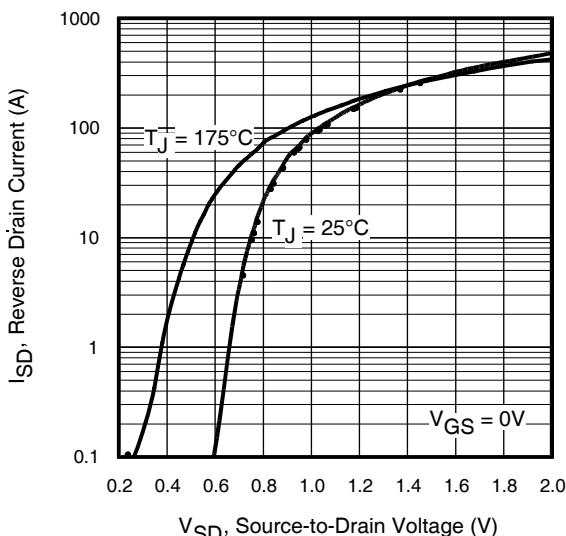


Fig 7. Typical Source-Drain Diode Forward Voltage

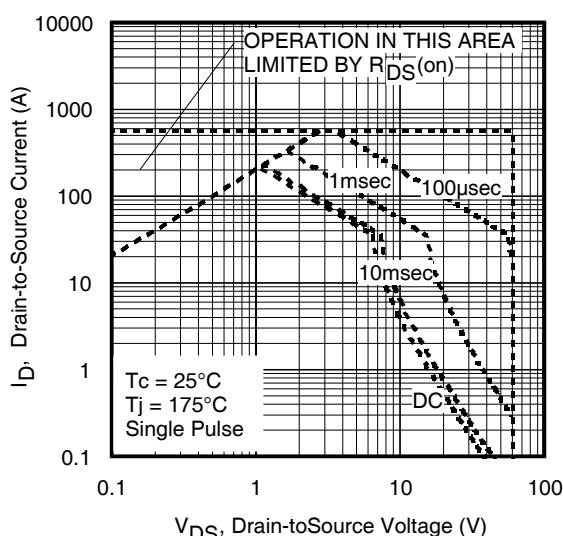


Fig 8. Maximum Safe Operating Area

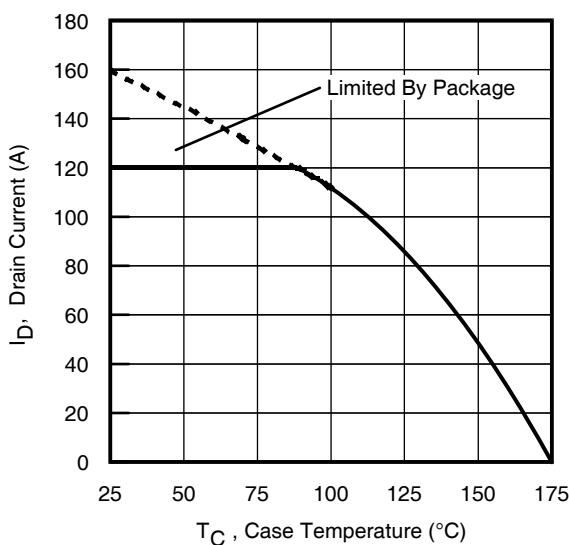


Fig 9. Maximum Drain Current vs. Case Temperature

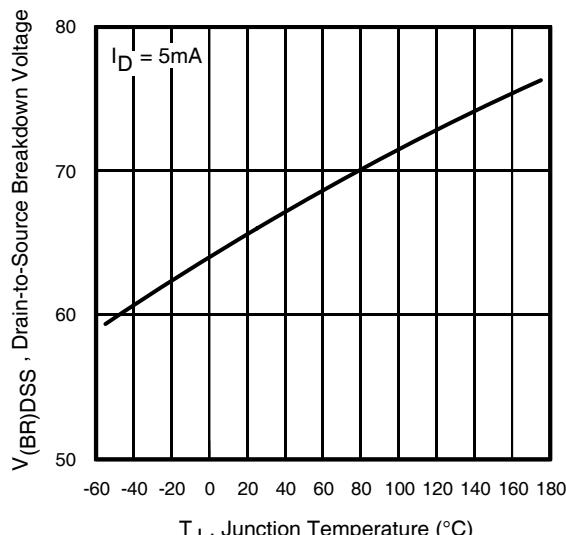


Fig 10. Drain-to-Source Breakdown Voltage

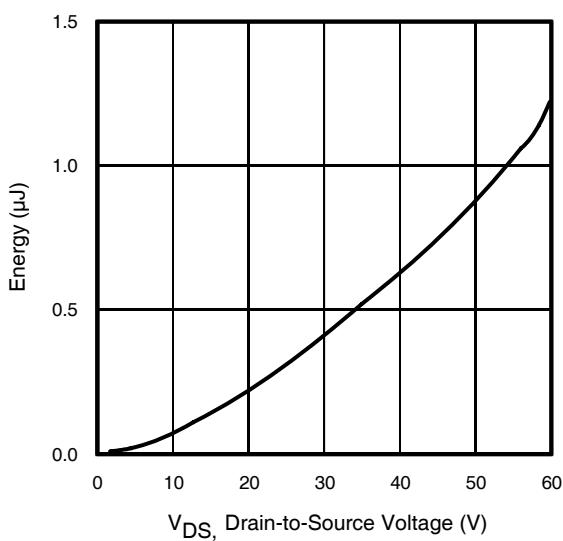


Fig 11. Typical C_{OSS} Stored Energy

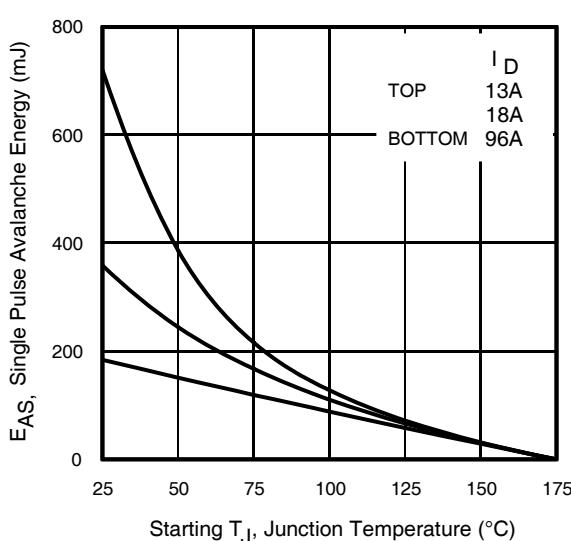


Fig 12. Maximum Avalanche Energy Vs. Drain Current

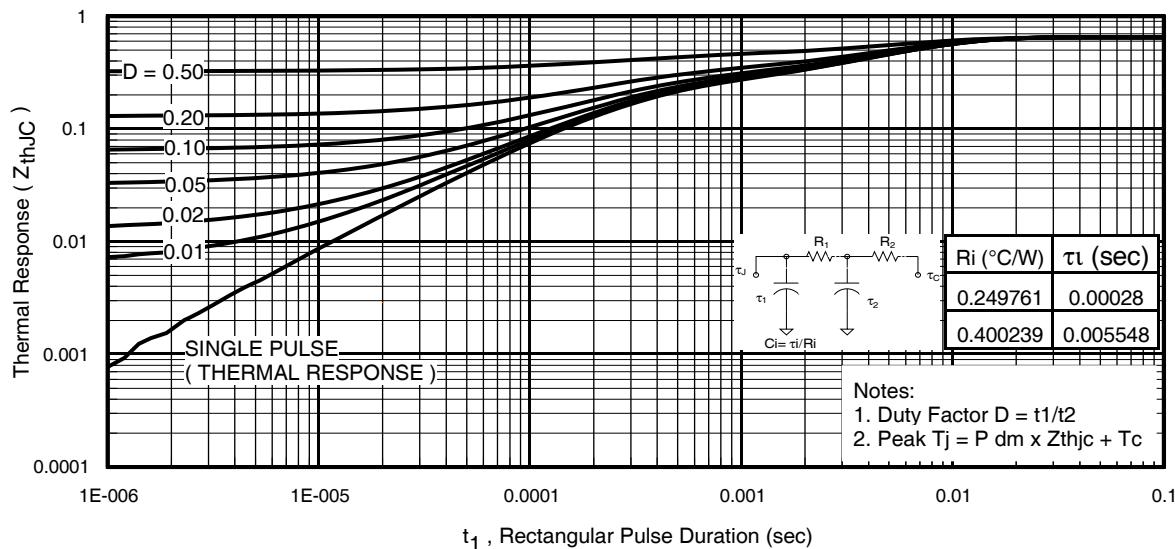


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

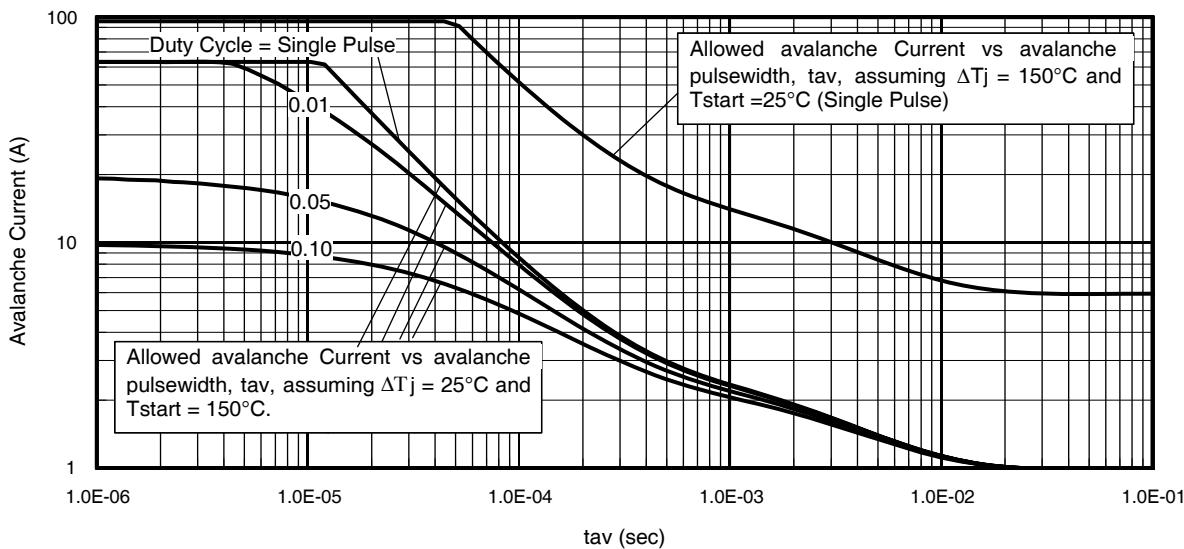


Fig 14. Typical Avalanche Current vs.Pulsewidth

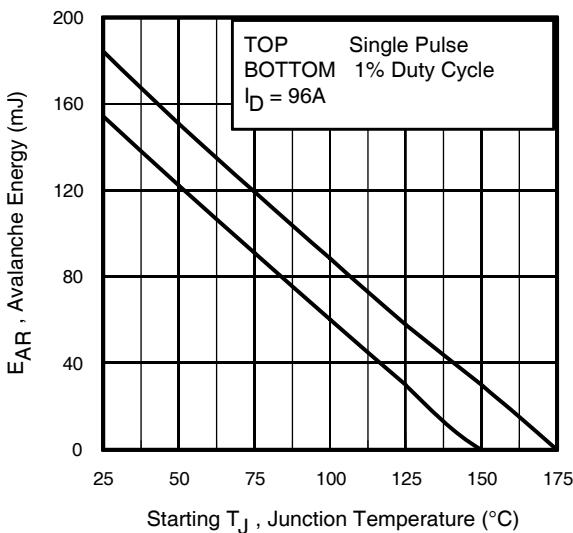


Fig 15. Maximum Avalanche Energy vs. Temperature

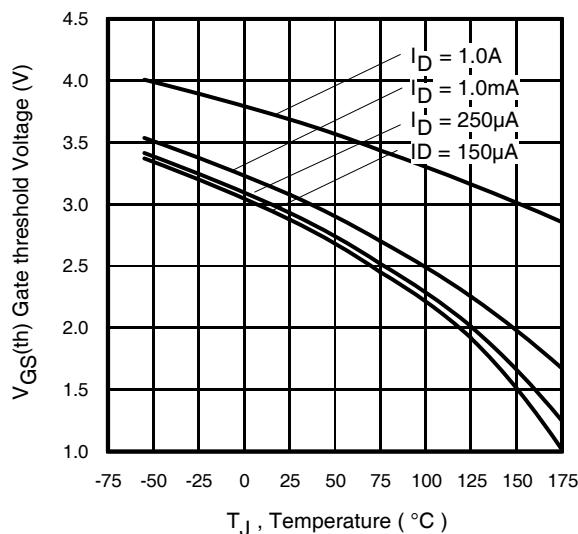
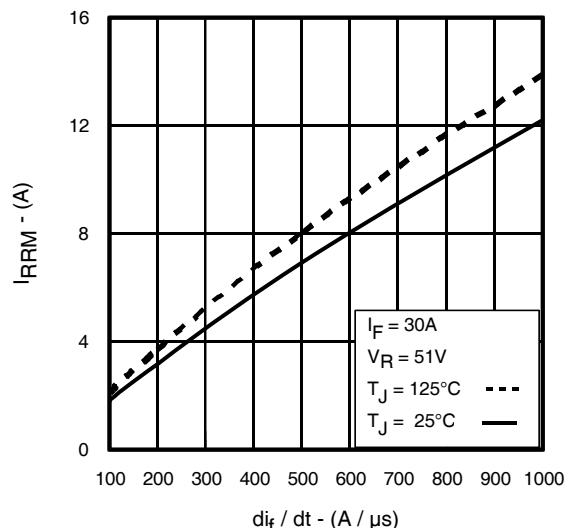
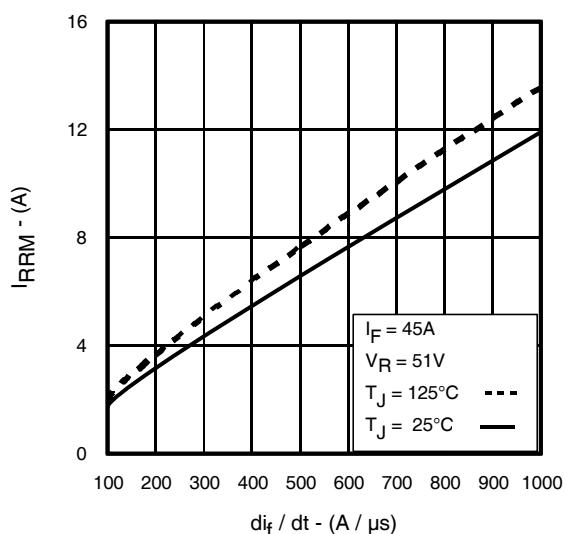
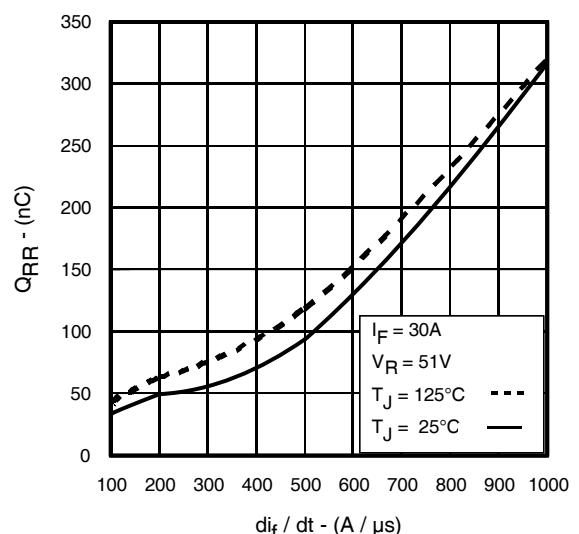
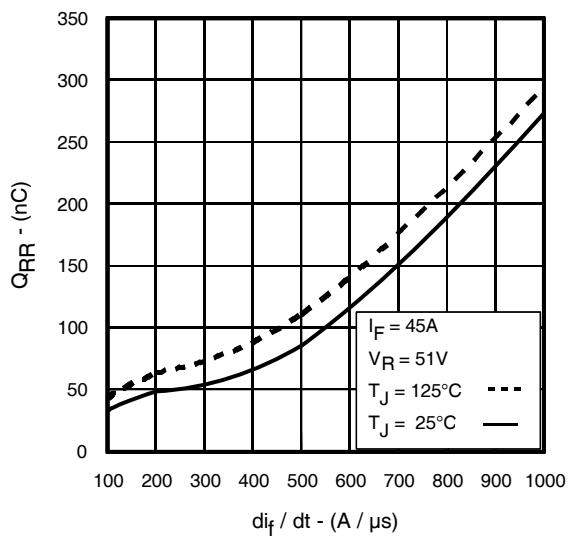
Notes on Repetitive Avalanche Curves , Figures 14, 15:
 (For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
 2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
 3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
 4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
 5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
 6. I_{av} = Allowable avalanche current.
 7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
- t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{th,JC}(D, t_{av})$ = Transient thermal resistance, see Figures 13

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{th,JC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

**Fig. 16.** Threshold Voltage Vs. Temperature**Fig. 17 -** Typical Recovery Current vs. di_f/dt **Fig. 18 -** Typical Recovery Current vs. di_f/dt **Fig. 19 -** Typical Stored Charge vs. di_f/dt **Fig. 20 -** Typical Stored Charge vs. di_f/dt

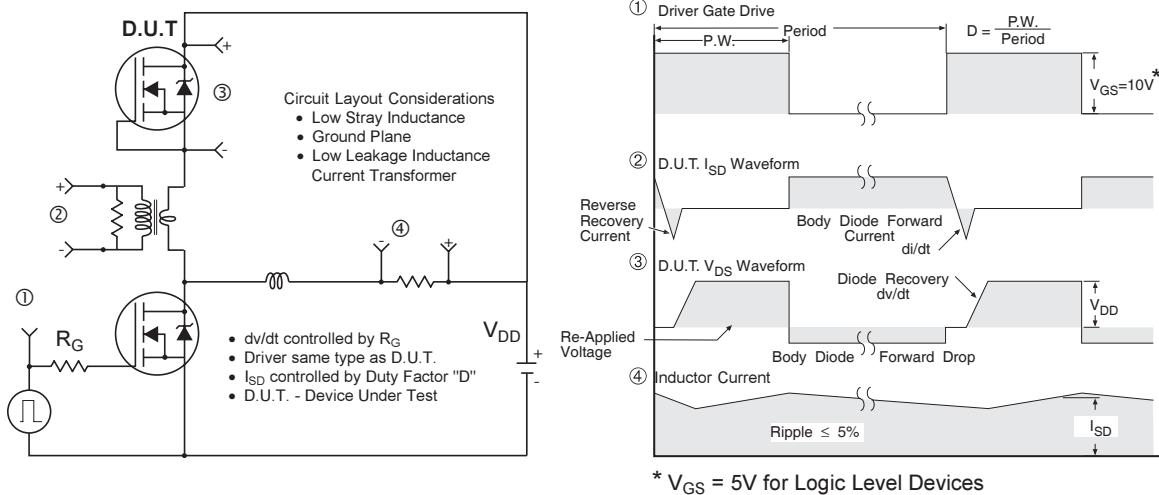


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

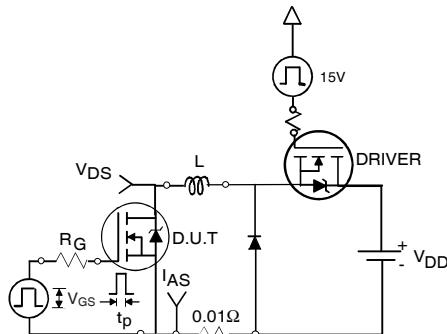


Fig 22a. Unclamped Inductive Test Circuit

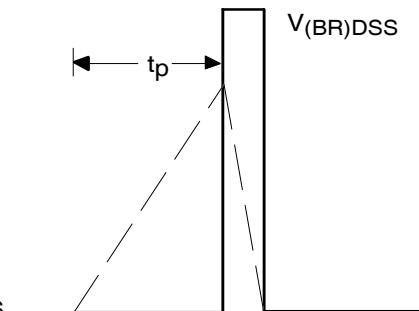


Fig 22b. Unclamped Inductive Waveforms

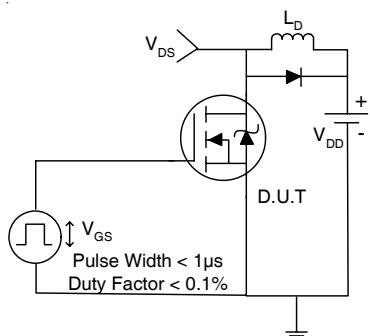


Fig 23a. Switching Time Test Circuit

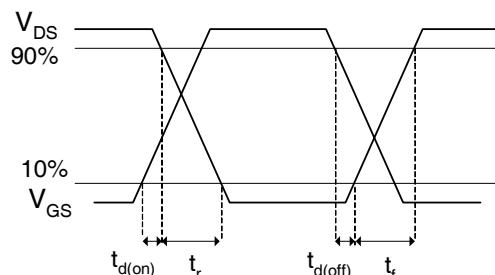


Fig 23b. Switching Time Waveforms

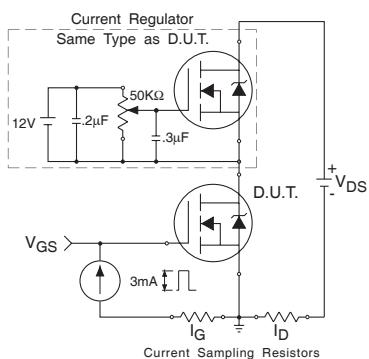


Fig 24a. Gate Charge Test Circuit
www.irf.com

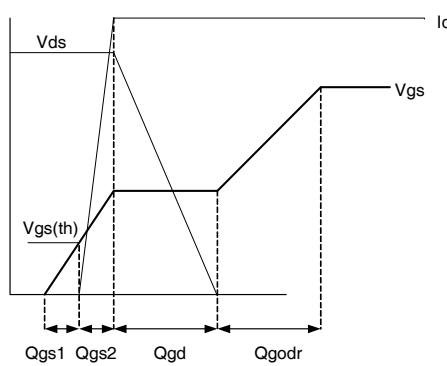
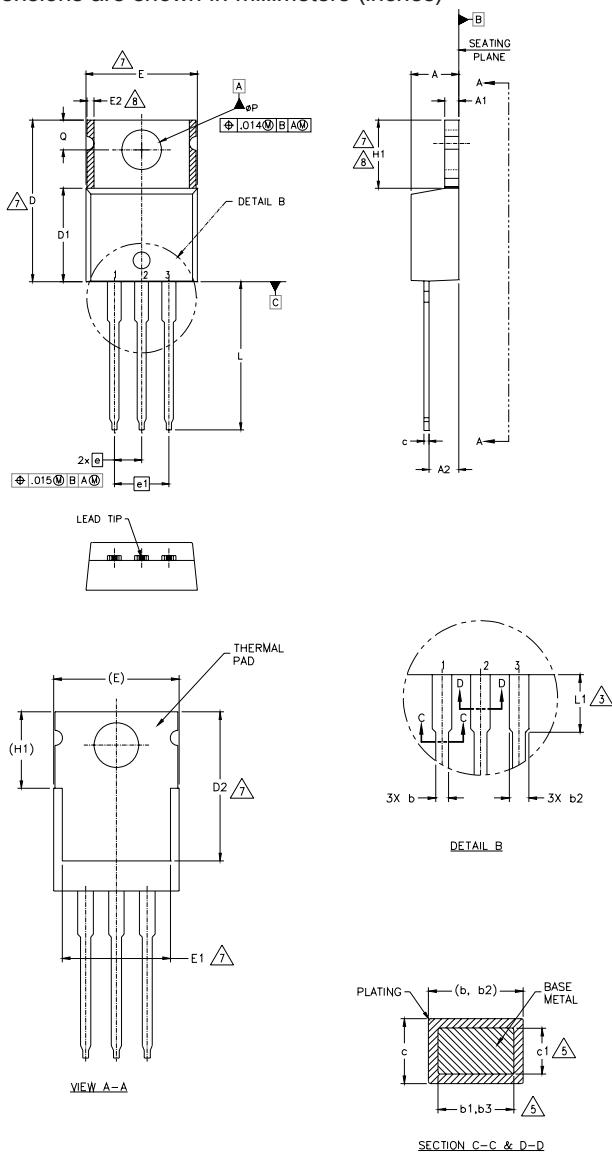


Fig 24b. Gate Charge Waveform

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- Dimensioning and tolerancing as per ASME Y14.5 M- 1994.
- Dimensions are shown in inches [millimeters].
- Lead dimension and finish uncontrolled in L1.
- Dimension D, D1 & E do not include mold flash. Mold flash shall not exceed .005" (0.127) per side. These dimensions are measured at the outermost extremes of the plastic body.
- Dimension b1, b3 & c1 apply to base metal only.
- Controlling dimension : INCHES.
- Thermal pad contour optional within dimensions E,H1,D2 & E1.
- Dimension E2 X H1 define a zone where stamping and singulation irregularities are allowed.
- Outline conforms to JEDEC TO-220, except A2 (max.) and D2 (min.) where dimensions are derived from the actual package outline.

SYMBOL	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	3.56	4.83	.140	.190
A1	0.51	1.40	.020	.055
A2	2.03	2.92	.080	.115
b	0.38	1.01	.015	.040
b1	0.38	0.97	.015	.038
b2	1.14	1.78	.045	.070
b3	1.14	1.73	.045	.068
c	0.36	0.61	.014	.024
c1	0.36	0.56	.014	.022
D	14.22	16.51	.560	.650
D1	8.38	9.02	.330	.355
D2	11.68	12.88	.460	.507
E	9.65	10.67	.380	.420
E1	6.86	8.89	.270	.350
E2	—	0.76	—	.030
e	2.54 BSC		.100 BSC	
e1	5.08 BSC		.200 BSC	
H1	5.84	6.86	.230	.270
L	12.70	14.73	.500	.580
L1	3.56	4.06	.140	.160
OP	3.54	4.08	.139	.161
Q	2.54	3.42	.100	.135

LEAD ASSIGNMENTS

HEXFET

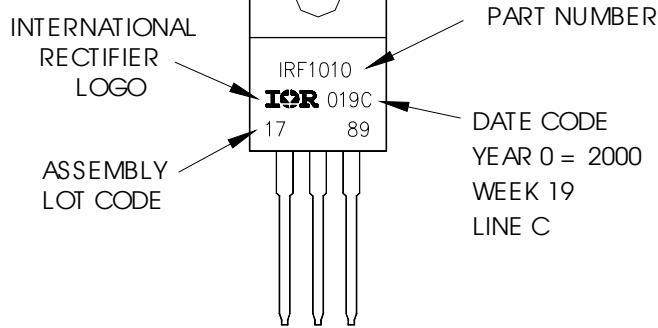
- GATE
- DRAIN
- SOURCE

IGBTs, GaP[®]

- GATE
- COLLECTOR
- Emitter

DIODES

- ANODE
- CATHODE
- ANODE



TO-220AB Part Marking Information

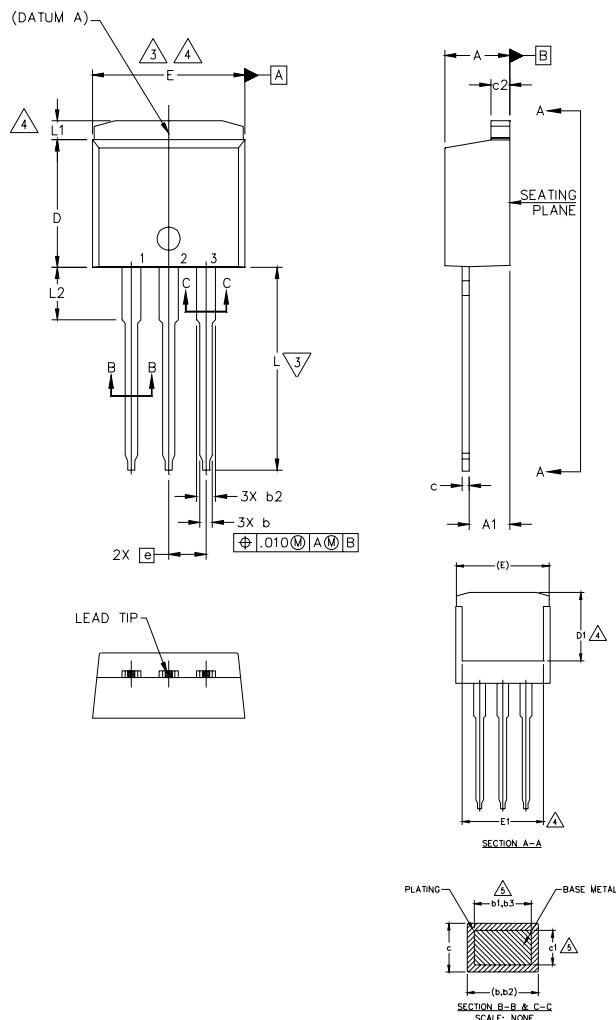
EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"

TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

TO-262 Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54	BSC	.100	BSC	
L	13.46	14.10	.530	.555	
L1	—	1.65	—	.065	4
L2	3.56	3.71	.140	.146	

LEAD ASSIGNMENTS

HEXFET

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

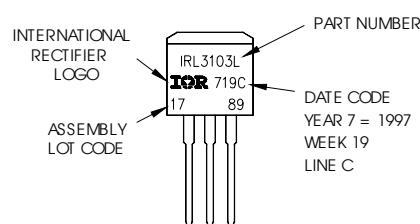
IGBTs, CoPACK

1. GATE
2. COLLECTOR
3. Emitter
4. COLLECTOR

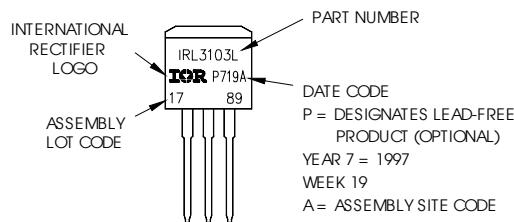
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW19, 1997
IN THE ASSEMBLY LINE "C"

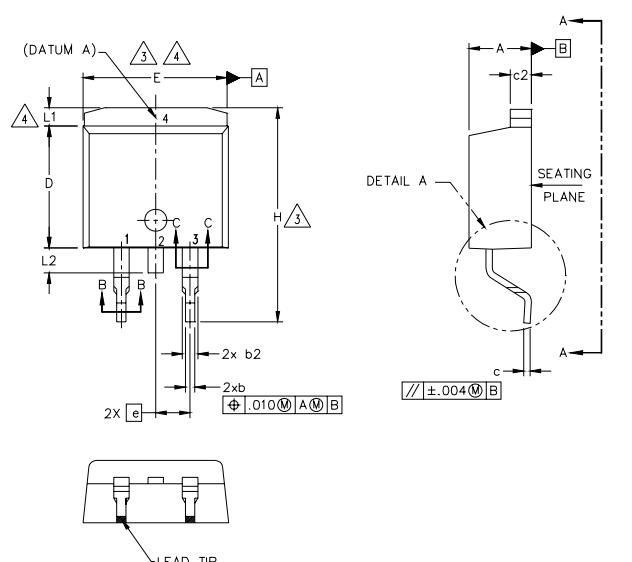
Note: "P" in assembly line position
indicates "Lead - Free"



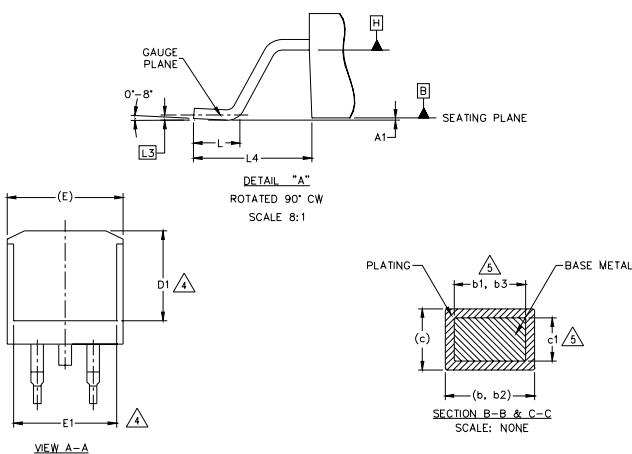
OR



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

D²Pak Package Outline (Dimensions are shown in millimeters (inches))

S Y M B O L	DIMENSIONS				N O T E S	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.06	4.83	.160	.190		
A1	0.00	0.254	.000	.010		
b	0.51	0.99	.020	.039	5	
b1	0.51	0.89	.020	.035	5	
b2	1.14	1.78	.045	.070		
b3	1.14	1.73	.045	.068		
c	0.38	0.74	.015	.029	5	
c1	0.38	0.58	.015	.023		
c2	1.14	1.65	.045	.065		
D	8.38	9.65	.330	.380	3	
D1	6.86	—	.270	—	4	
E	9.65	10.67	.380	.420	3,4	
E1	6.22	—	.245	—	4	
e	2.54	BSC	.100	BSC		
H	14.61	15.88	.575	.625		
L	1.78	2.79	.070	.110		
L1	—	1.65	—	.066		
L2	1.27	1.78	—	.070		
L3	0.25 BSC		.010	BSC		
L4	4.78	5.28	.188	.208		



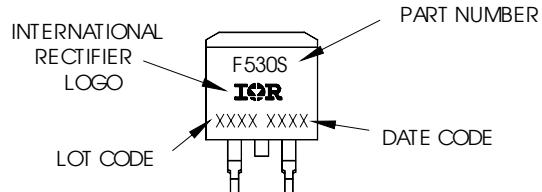
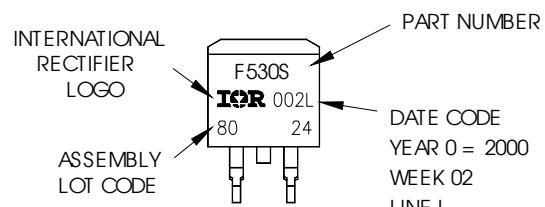
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

D²Pak Part Marking Information

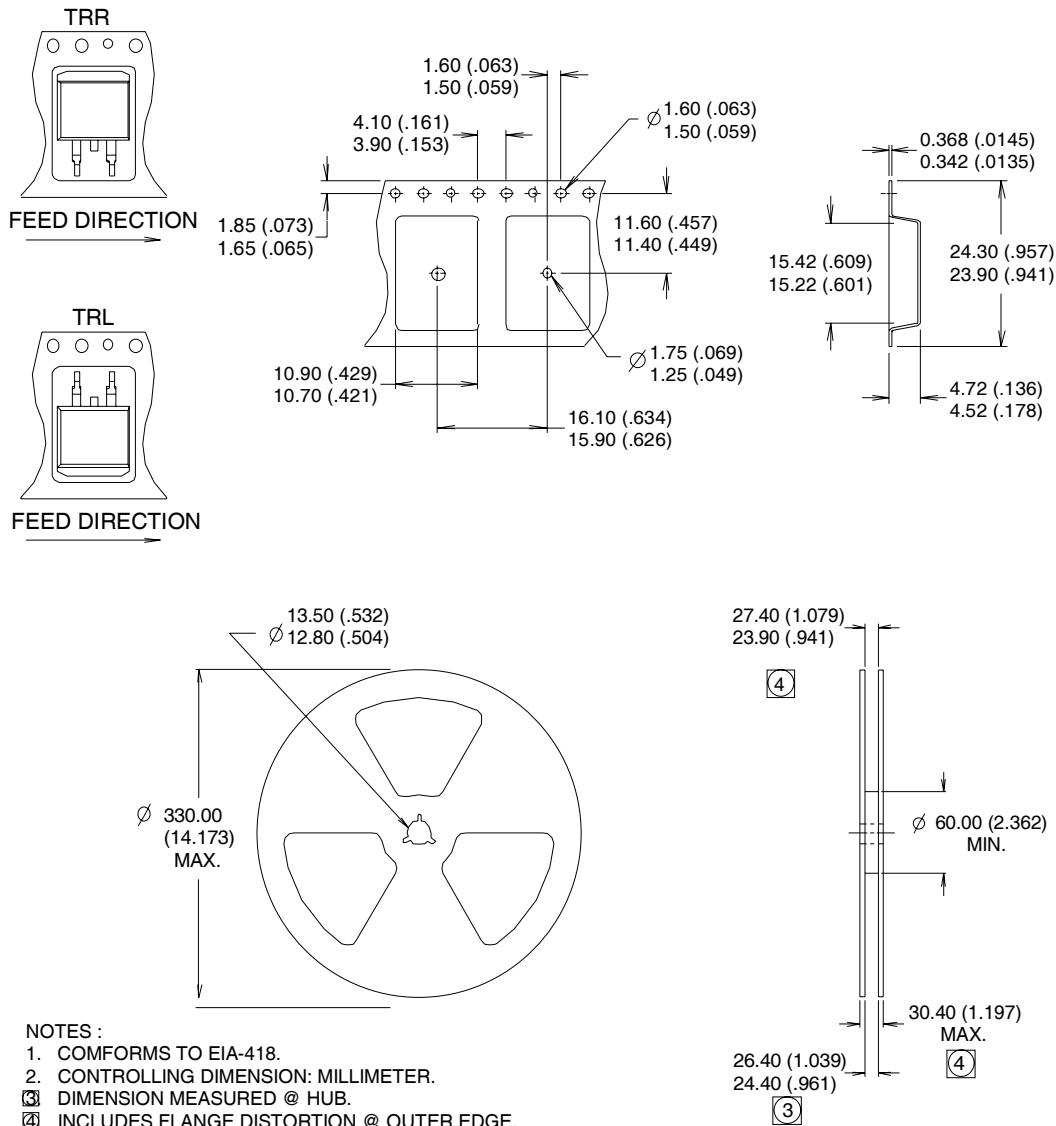
EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
For GB Production
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

D²Pak Tape & Reel Information



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

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