

International IOR Rectifier

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Optimized for SMPS Applications
- Lead-Free

Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRFZ34VL) is available for low-profile application.

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ⑤	30	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ⑤	21	
I_{DM}	Pulsed Drain Current ① ⑤	120	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	70	W
	Linear Derating Factor	0.46	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current ①	30	A
E_{AR}	Repetitive Avalanche Energy ①	7.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③ ⑤	4.5	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.15	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted)**	—	40	

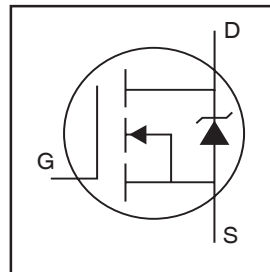
www.irf.com

PD - 95560A

IRFZ34VSPbF

IRFZ34VLPbF

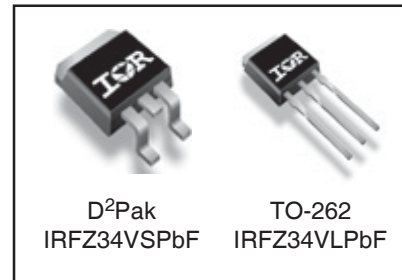
HEXFET® Power MOSFET



$$V_{DSS} = 60\text{V}$$

$$R_{DS(on)} = 28\text{m}\Omega$$

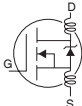
$$I_D = 30\text{A}$$



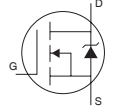
D²Pak
IRFZ34VSPbF

TO-262
IRFZ34VLPbF

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.062	—	V/°C	Reference to 25°C, I _D = 1mA ^⑤
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	28	mΩ	V _{GS} = 10V, I _D = 18A ^④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	15	—	—	S	V _{DS} = 25V, I _D = 18A ^{④⑤}
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 60V, V _{GS} = 0V
		—	—	250		V _{DS} = 48V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	49	nC	I _D = 30A
Q _{gs}	Gate-to-Source Charge	—	—	12		V _{DS} = 48V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	18		V _{GS} = 10V, See Fig. 6 and 13 ^⑤
t _{d(on)}	Turn-On Delay Time	—	10	—	ns	V _{DD} = 30V
t _r	Rise Time	—	65	—		I _D = 30A
t _{d(off)}	Turn-Off Delay Time	—	31	—		R _G = 12Ω
t _f	Fall Time	—	40	—		V _{GS} = 10V, See Fig. 10 ^{④⑤}
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	1120	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	250	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	59	—		f = 1.0MHz, See Fig. 5 ^⑤
E _{AS}	Single Pulse Avalanche Energy ^{②⑤}	—	260	81		mJ

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	30	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ^①	—	—	120		
V _{SD}	Diode Forward Voltage	—	—	1.6	V	T _J = 25°C, I _S = 30A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	—	70	110	ns	T _J = 25°C, I _F = 30A
Q _{rr}	Reverse Recovery Charge	—	99	150	nC	di/dt = 100A/μs ^{④⑤}
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T_J = 25°C, L = 180μH
R_G = 25Ω, I_{AS} = 30A. (See Figure 12)
- ③ I_{SD} ≤ 30A, di/dt ≤ 250A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 175°C

- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ Uses IRFZ34V data and test conditions.

** When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to
application note #AN-994.

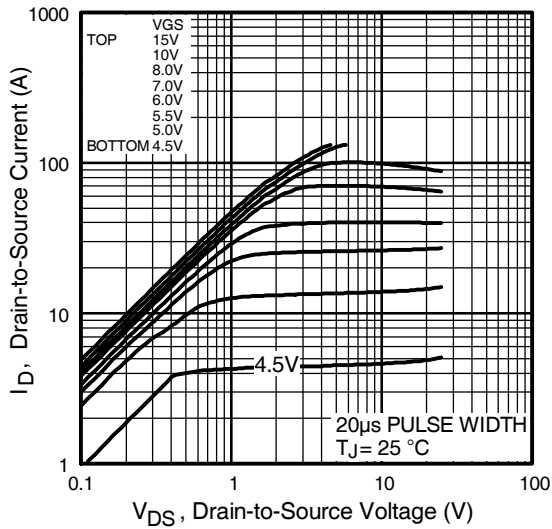


Fig 1. Typical Output Characteristics

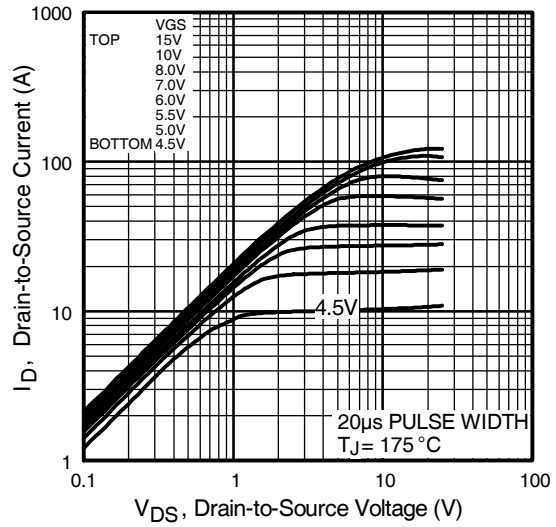


Fig 2. Typical Output Characteristics

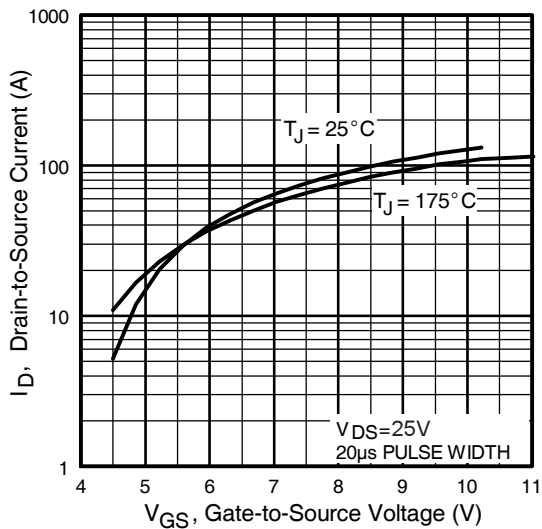


Fig 3. Typical Transfer Characteristics

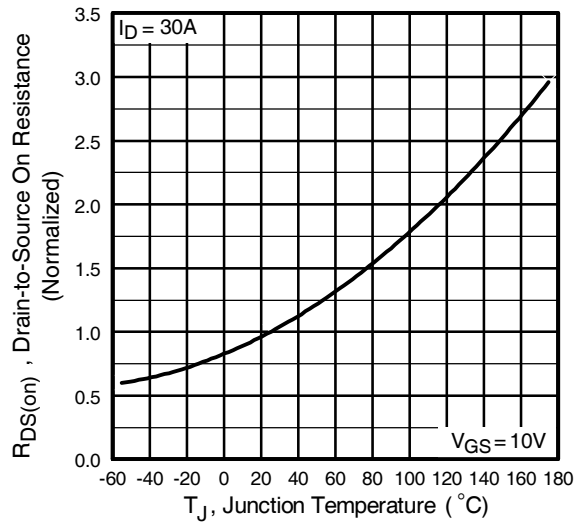


Fig 4. Normalized On-Resistance Vs. Temperature

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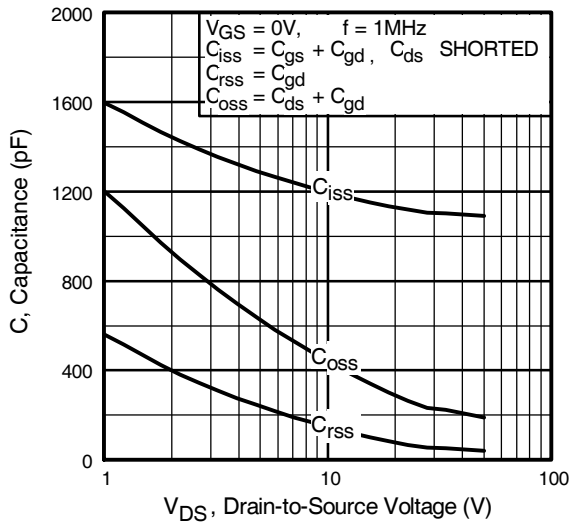


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

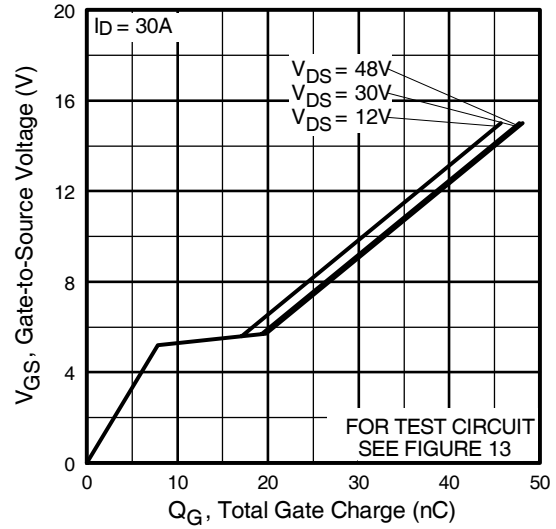


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

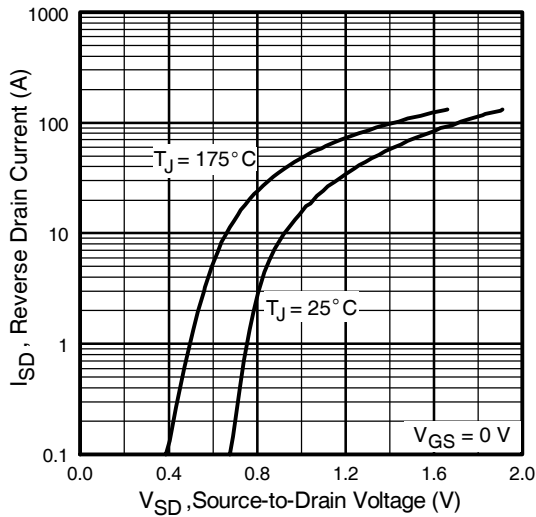


Fig 7. Typical Source-Drain Diode Forward Voltage

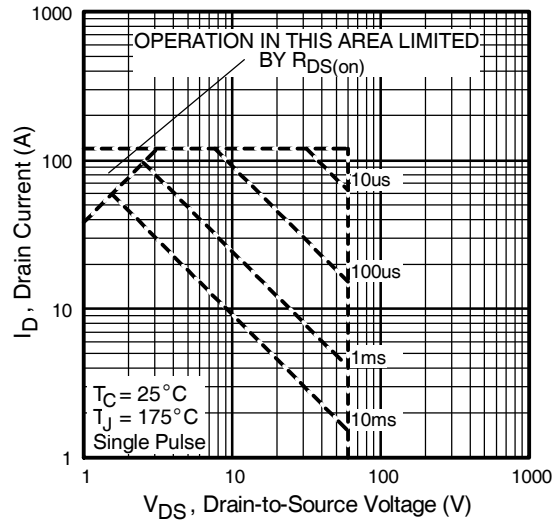


Fig 8. Maximum Safe Operating Area

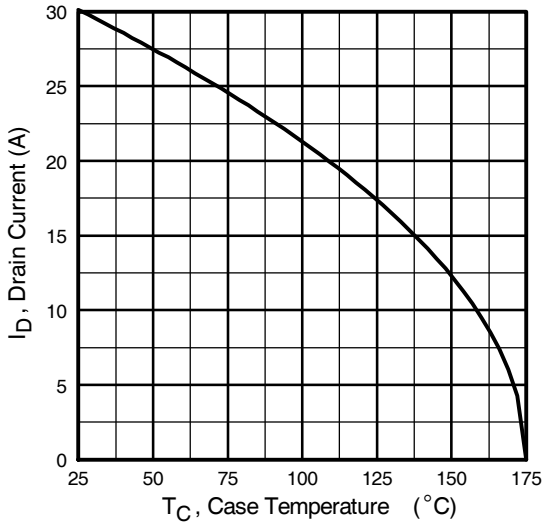


Fig 9. Maximum Drain Current Vs. Case Temperature

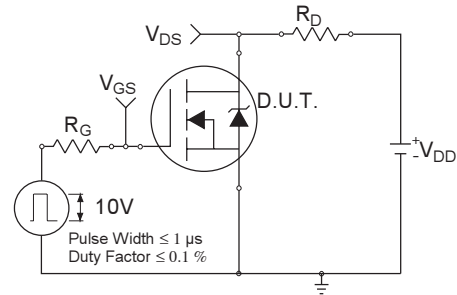


Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

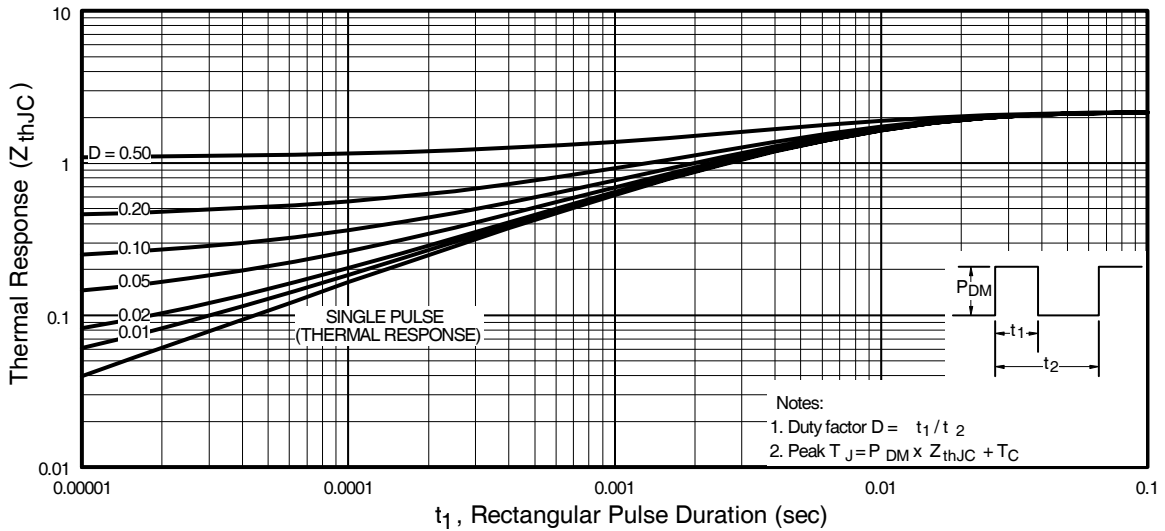


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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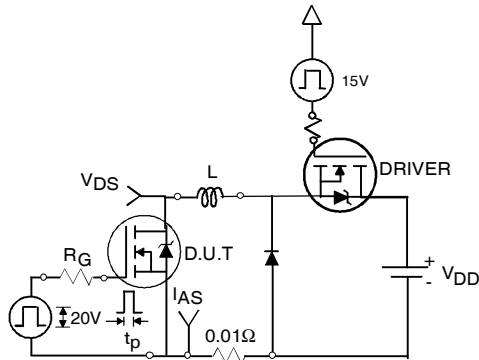


Fig 12a. Unclamped Inductive Test Circuit

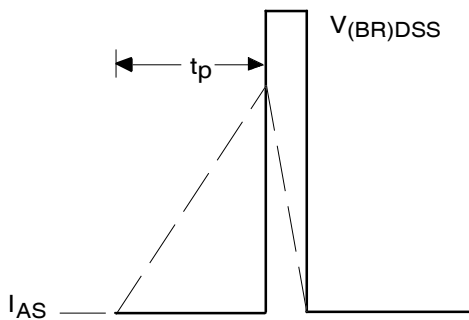


Fig 12b. Unclamped Inductive Waveforms

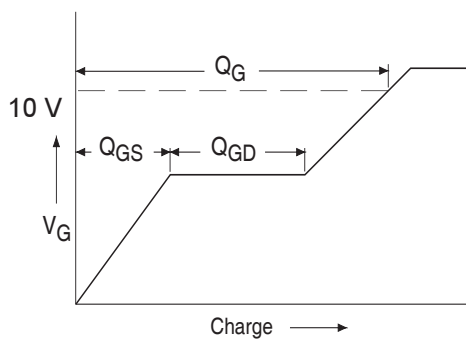


Fig 13a. Basic Gate Charge Waveform

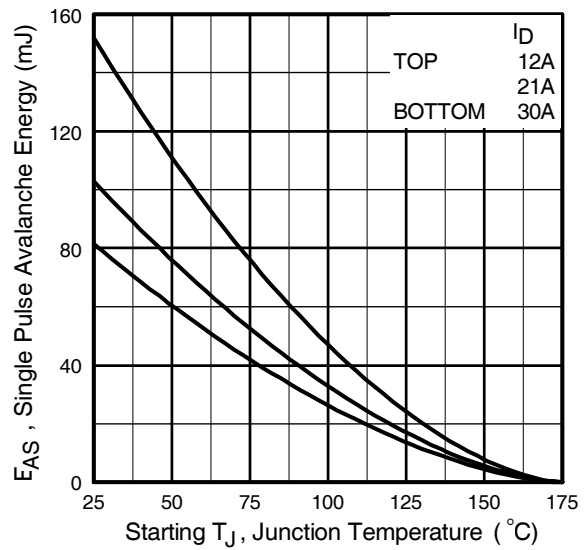


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

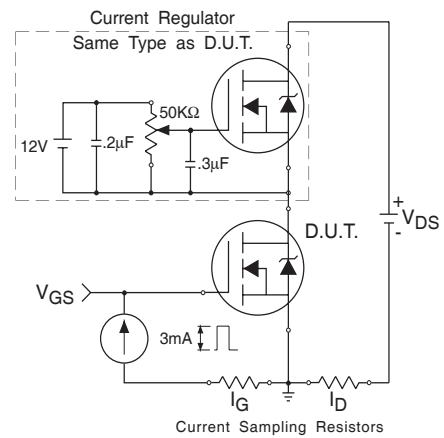
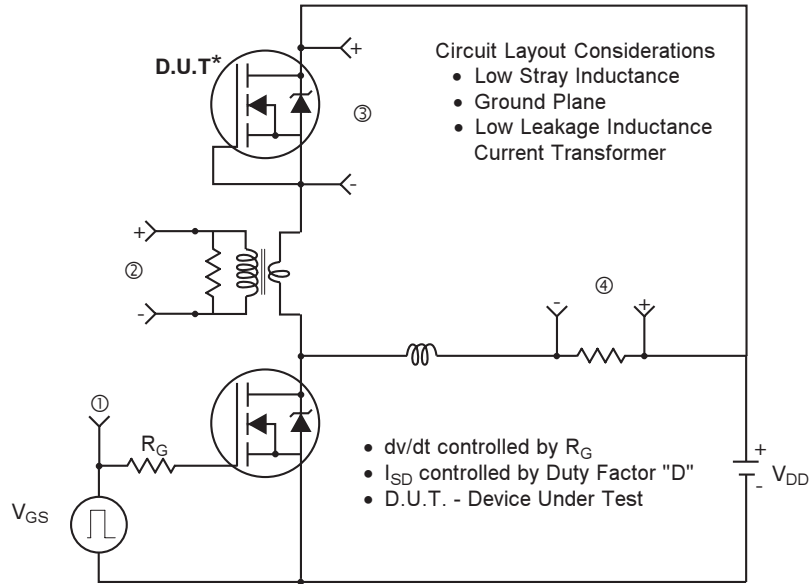


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel

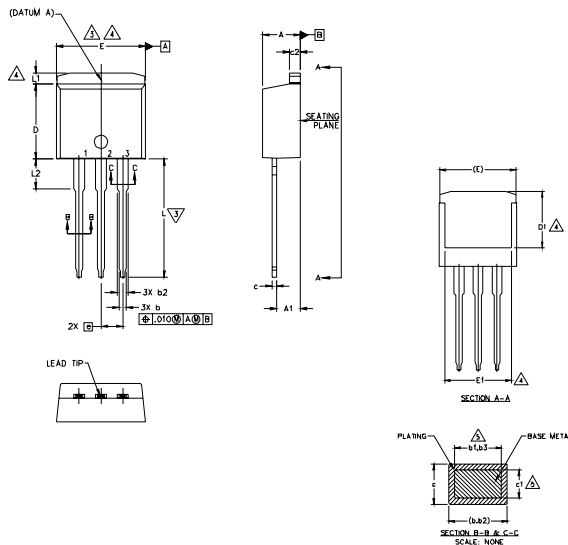


*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs

TO-262 Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
 5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 6. CONTROLLING DIMENSION: INCH.
 - 7.- OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.), AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.565	
L1	-	1.65	-	.065	4
L2	3.56	3.71	.140	.146	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

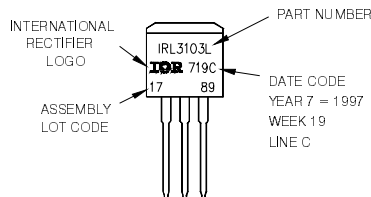
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

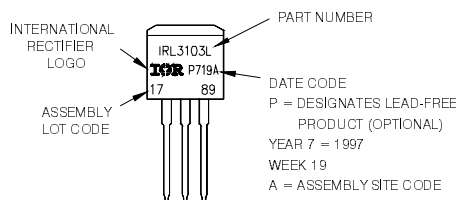
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE 'C'

Note: "P" in assembly line position indicates "Lead - Free"



OR



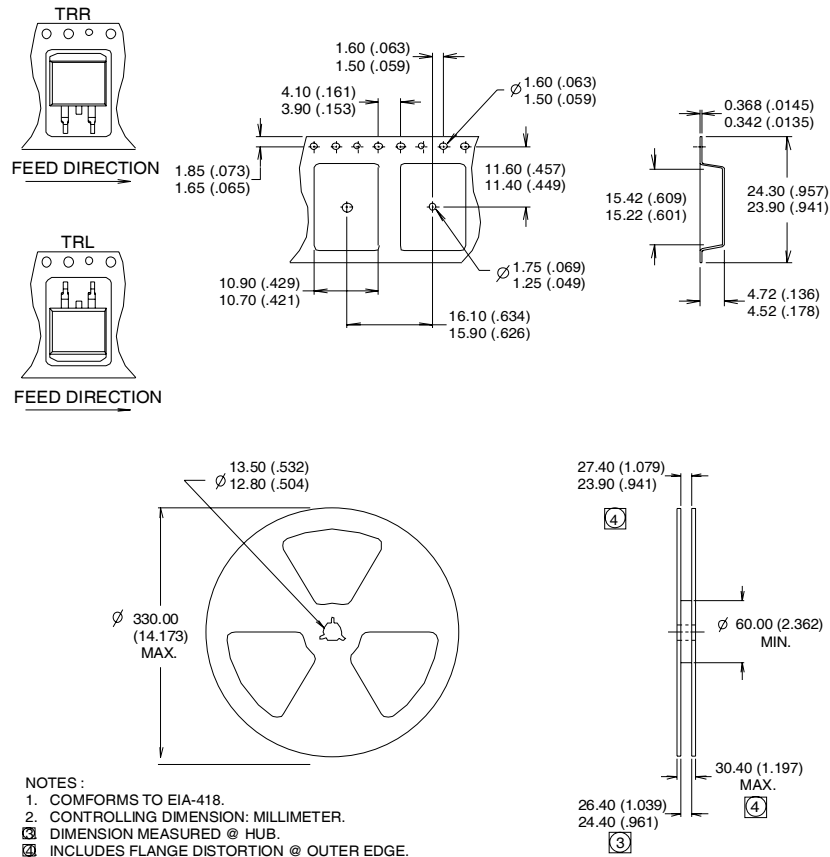
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>
www.irf.com

IRFZ34VS/LPbF

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D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.

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