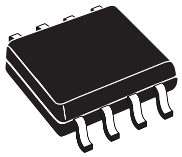
STS12NH3LL

N-channel 30 V - 0.008 Ω - 12 A - SO-8 ultra low gate charge STripFET™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STS12NH3LL	30 V	<0.0105 Ω	12 A

- Optimal $R_{DS(on)}$ x Qg trade-off @ 4.5 V
- Switching losses reduced
- Low input capacitance
- Low threshold device



SO-8

Application

- Switching applications

Description

This series is based on the latest generation of ST's proprietary "STripFET™" technology. An innovative layout enables the device to also exhibit extremely low gate charge for the most demanding requirements as high-side switch in high-frequency DC-DC converters. It's therefore ideal for high-density converters in telecom and computer applications.

Figure 1. Internal schematic diagram

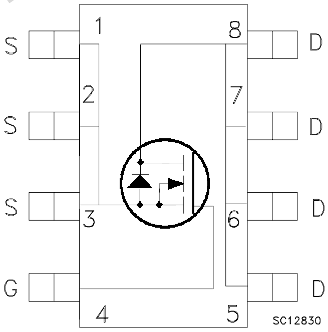


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Table 1. Device summary

Order code	Marking	Packag	Packaging
STS12NH3LL	12H3LL	SO-8	Tape & reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}[1]	Gate-source voltage	± 16	V
V_{GS}[2]	Gate-source voltage	± 18	V
I_D	Drain current (continuous) at T_C = 25 °C	12	A
I_D	Drain current (continuous) at T_C=100 °C	7.5	A
I_{DM}[3]	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at T_C = 25 °C	2.7	W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Continuous mode
2. Guaranteed for test time ≤ 15 ms
3. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$[1]	Thermal resistance junction-ambient	47	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

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2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±16 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 6 A V_{GS}= 4.5 V, I_D= 6 A		0.008 0.010	0.0105 0.013	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	V_{DS} =10 V, I_D = 12 A		38		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0		965 285 38		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=15 V, I_D = 12 A V_{GS} =4.5 V *(see Figure 20)*		9 3.7 3	12	nC nC nC
Q_{gs1} Q_{gs2}	Pre V_{th} gate-to-source charge Post V_{th} gate-to-source charge	V_{DD}=15 V, I_D = 12 A V_{GS} =4.5 V *(see Figure 20)*		2.5 1.2		nC nC
R_G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test signal level = 20 mV open drain	0.5	1.5	2.5	Ω

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Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=15 V, I_D= 6 A, R_G=4.7 Ω, V_{GS}=4.5 V *(see Figure 14)*		15		ns
t_r	Rise time			32		ns
$t_{d(off)}$	Turn-off delay time			18		ns
t_f	Fall time			8.5		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				12	A
I_{SDM}(1)	Source-drain current (pulsed)				48	A
V_{SD}(2)	Forward on Voltage	I_{SD}=12 A, V_{GS}=0			1.3	V
t_{rr}	Reverse recovery time	I_{SD}=12 A, di/dt = 100 A/µs, V_{DD}=20 V, Tj=150 °C *(see Figure 16)*		24		ns
Q_{rr}	Reverse recovery charge			17.4		nC
I_{RRM}	Reverse recovery current			1.45		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 µs, duty cycle 1.5%

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2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

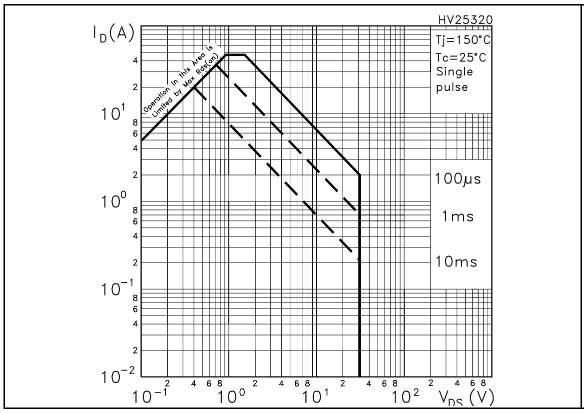

Figure 3. Thermal impedance

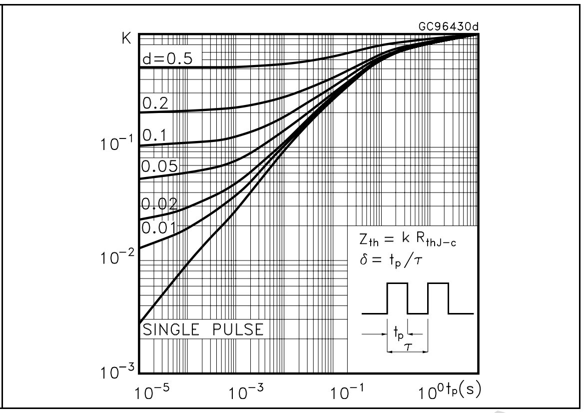

Figure 4. Output characteristics

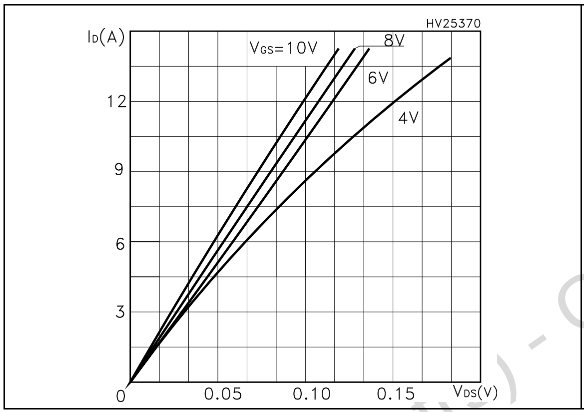

Figure 5. Transfer characteristics

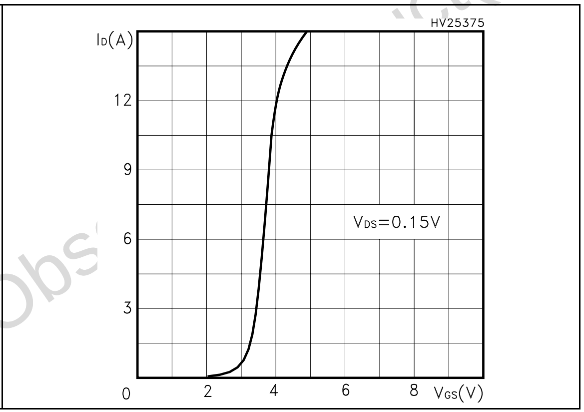

Figure 6. Transconductance

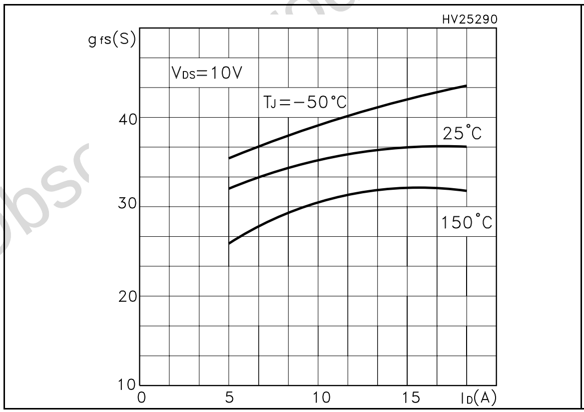

Figure 7. Static drain-source on resistance

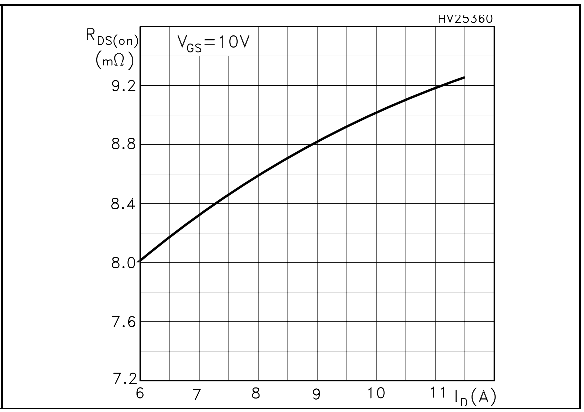

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Figure 8. Gate charge vs gate-source voltage

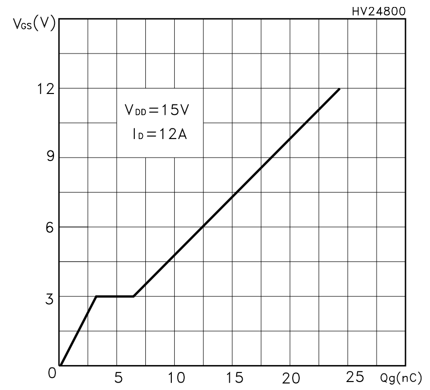


Figure 9. Capacitance variations

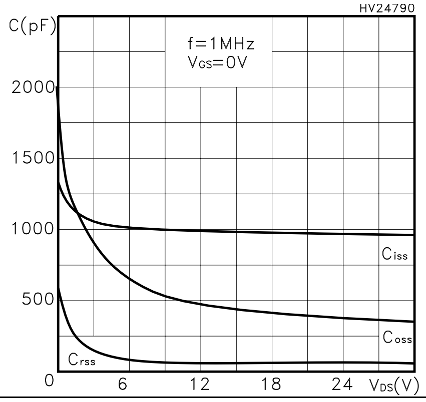


Figure 10. Normalized gate threshold voltage vs temperature

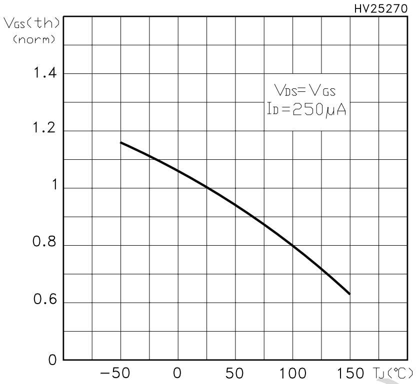


Figure 11. Normalized on resistance vs temperature

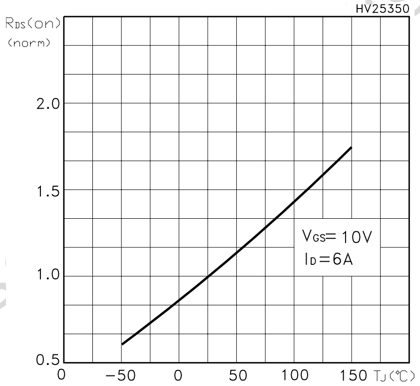


Figure 12. Source-drain diode forward characteristics

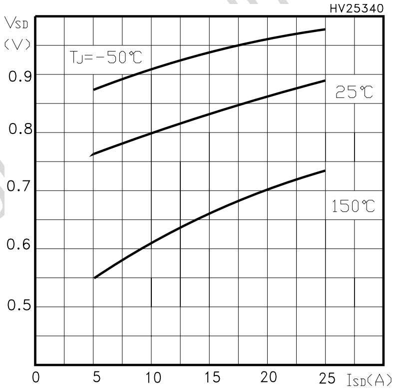
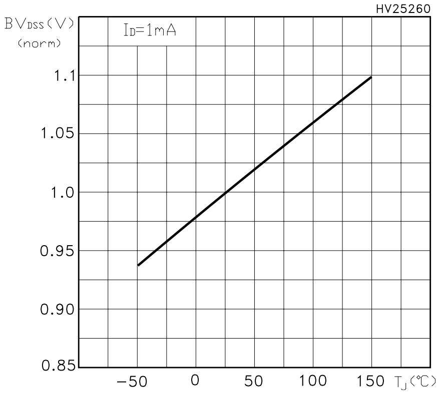


Figure 13. Normalized B_{VDSS} vs temperature



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3 Test circuit

Figure 14. Switching times test circuit for resistive load

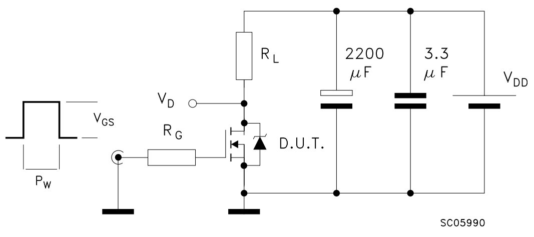

Figure 15. Gate charge test circuit

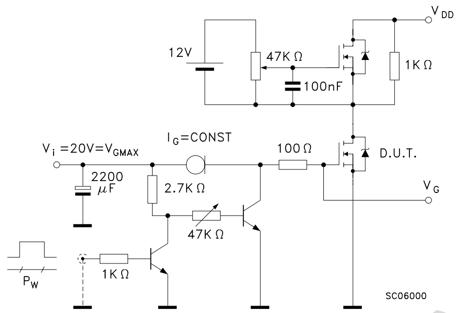

Figure 16. Test circuit for inductive load switching and diode recovery times

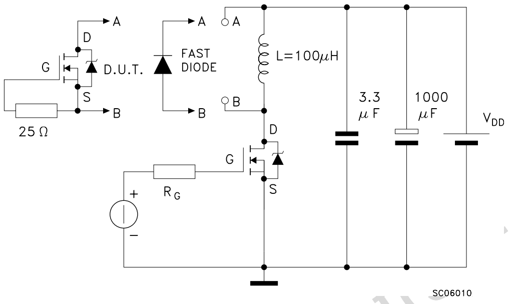

Figure 17. Unclamped inductive load test circuit

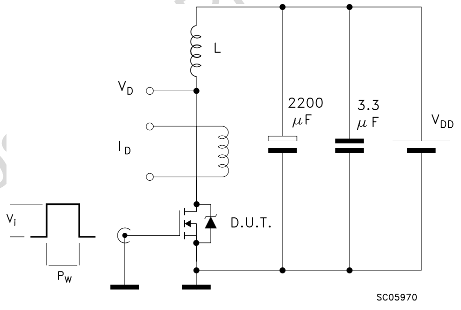

Figure 18. Unclamped inductive waveform

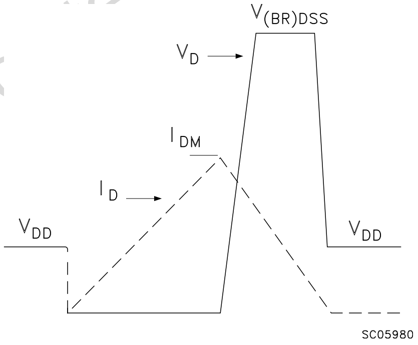

Figure 19. Switching time waveform

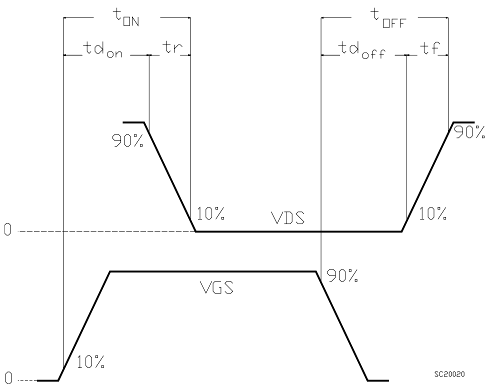

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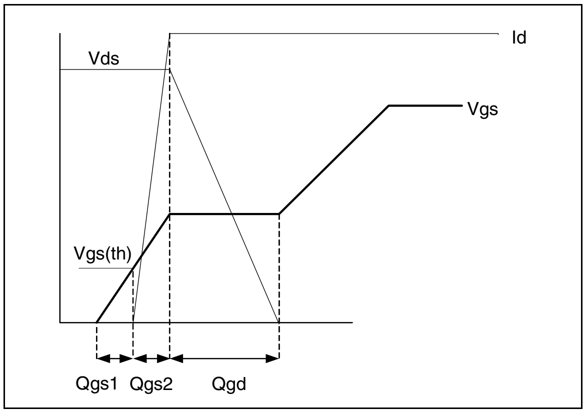
Figure 20. Gate charge waveform



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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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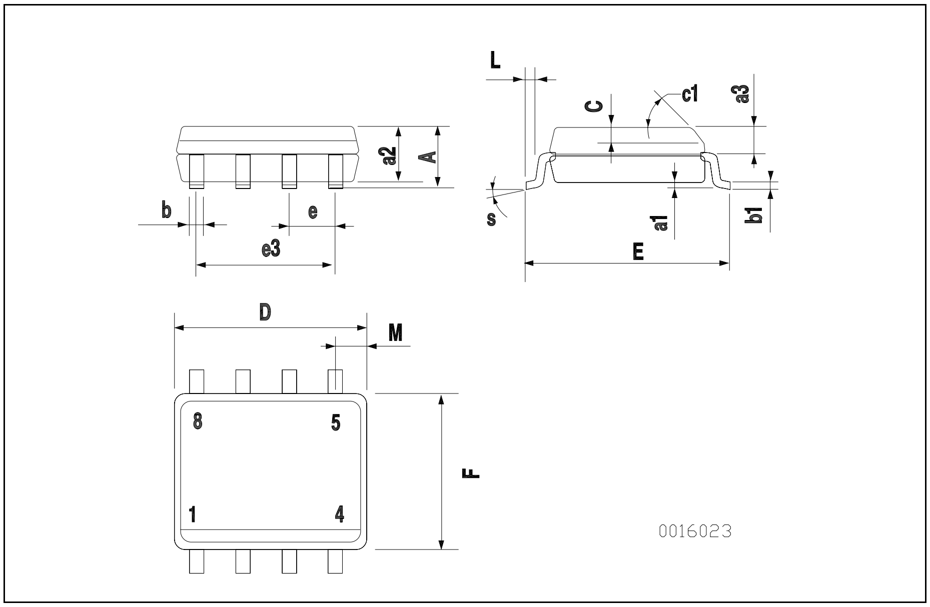
SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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5 Revision history

Table 8. Document revision history

Date	Revision	Changes
22-Jun2004	1	First release
03-Aug-2004	2	Some value change in *Table 2*
08-Mar-2005	3	Complete version
17-Mar-2005	4	Ron value change (see *Table 4*)
23-Jun-2005	5	New Rg value on *Table 5*
30-Mar-2006	6	The document has been reformatted
17-Apr-2007	7	New parameters on *Table 5* and new *Figure 20*
23-Apr-2007	8	Modified value on *Table 2*
26-Nov-2007	9	Modified marking on *Table 1*

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