STN1N20

N-channel 200 V, 1.2 Ω, 1 A, SOT-223 MESH OVERLAY™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STN1N20	200 V	< 1.5 Ω	1 A

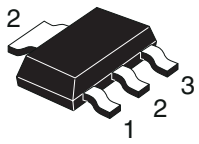
- 100% avalanche tested

Application

- Switching applications

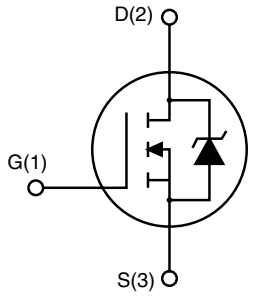
Description

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performance. The new patented STrip layout coupled with the company's proprietary edge termination structure, makes it suitable in converters for lighting applications.



SOT-223

Figure 1. Internal schematic diagram



AM01475v1

Table 1. Device summary

Order codes	Marking	Package	Packaging
STN1N20	N1N20	SOT-223	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} =0)	200	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25 °C	1	A
I_D	Drain current (continuous) at T_C = 100 °C	0.6	A
I_{DM} (1)	Drain current (pulsed)	4	A
P_{TOT}	Total dissipation at T_C = 25 °C	2.9	W
	Derating factor	0.023	W/°C
dv/dt	Peak diode recovery voltage slope	6	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max	43	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	60	°C/W
T_l	Maximum lead temperature for soldering purpose	260	°C

Table 4. Thermal data

Symbol	Parameter	Value	Unit
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	1	A
E_{AS}	Single pulse avalanche energy (1)	10	mJ

1. Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V

2 Electrical characteristics

(Tcase = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0) V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C				1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 0.5 A		1.2	1.5	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 0.5 A		2.7		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		206 40 15		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 160 V, I_D = 4 A, V_{GS} = 10 V (see *Figure 14*)		11 2.8 4	15.7	nC nC nC

1. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 160 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13*)		9 10 25 6		ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				1 4	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 1 A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 4 A, di/dt = 100 A/µs V_{DD} = 30 V, T_j = 150 °C (see *Figure 18*)		124 446 7.2		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

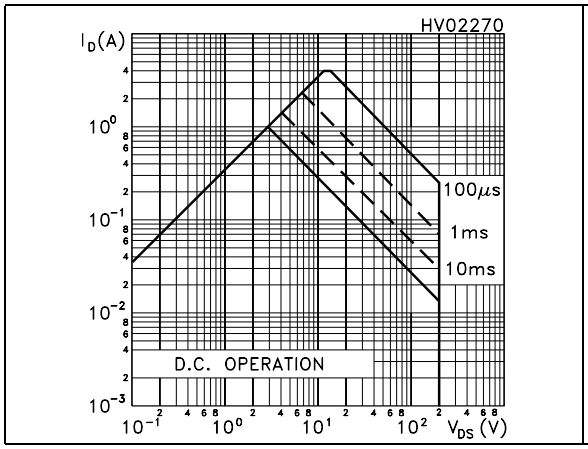


Figure 3. Thermal impedance

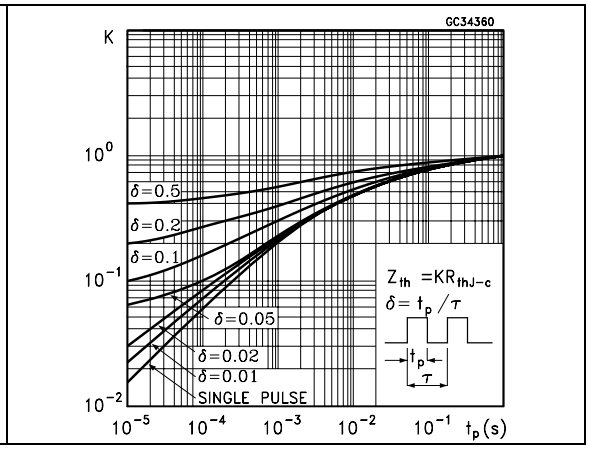


Figure 4. Output characteristics

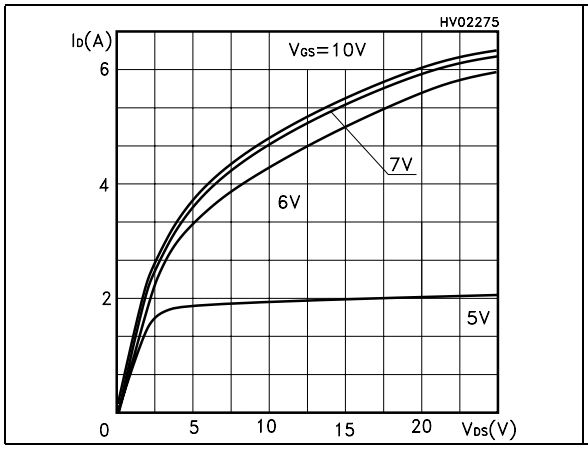


Figure 5. Transfer characteristics

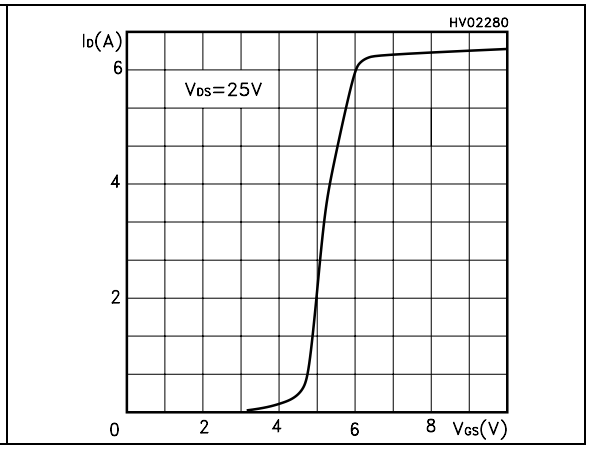


Figure 6. Transconductance

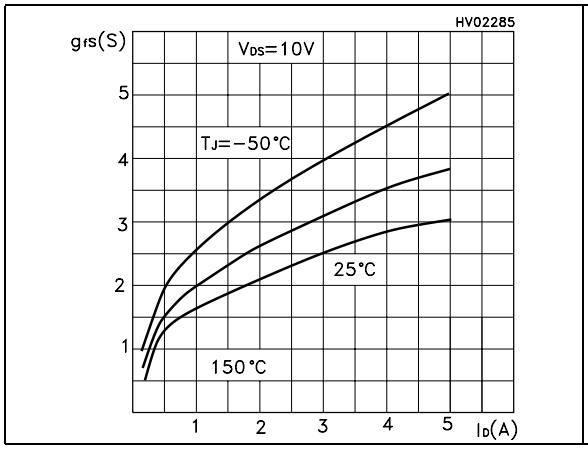


Figure 7. Static drain-source on resistance

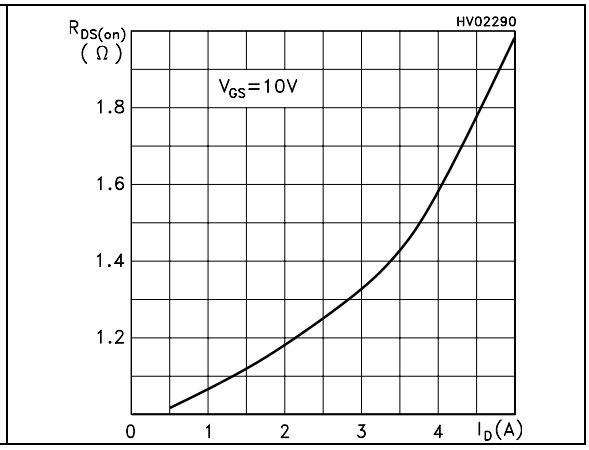


Figure 8. Gate charge vs gate-source voltage

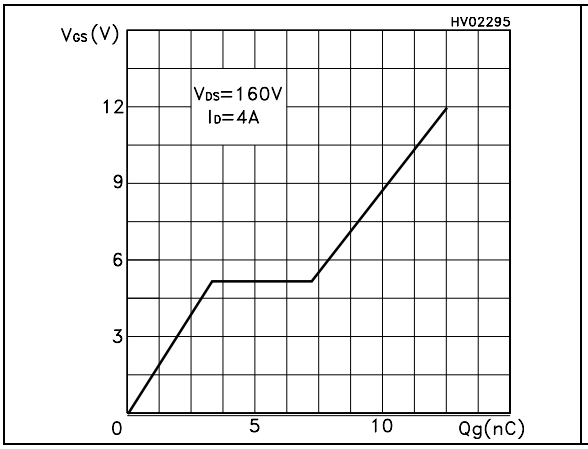


Figure 9. Capacitance variations

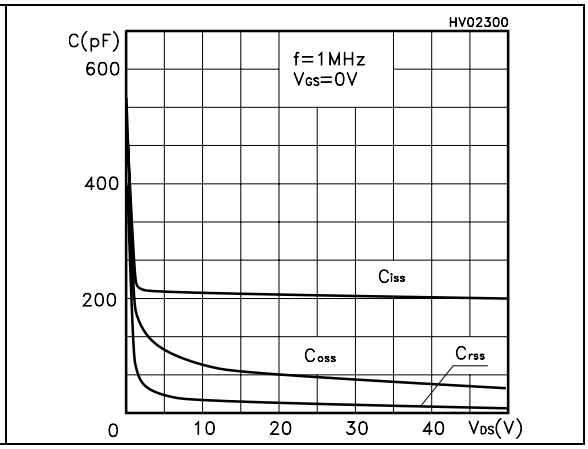


Figure 10. Normalized gate threshold voltage vs temperature

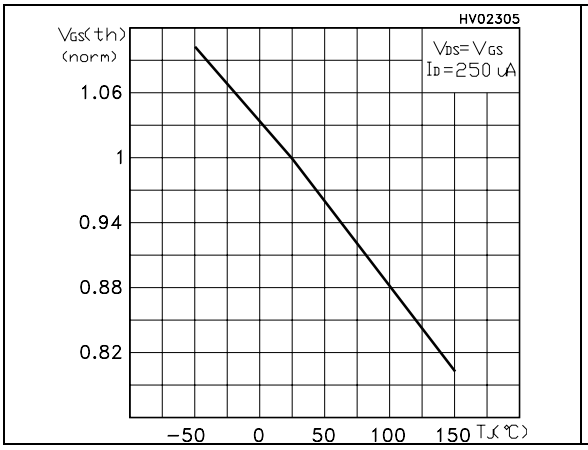


Figure 11. Normalized on resistance vs temperature

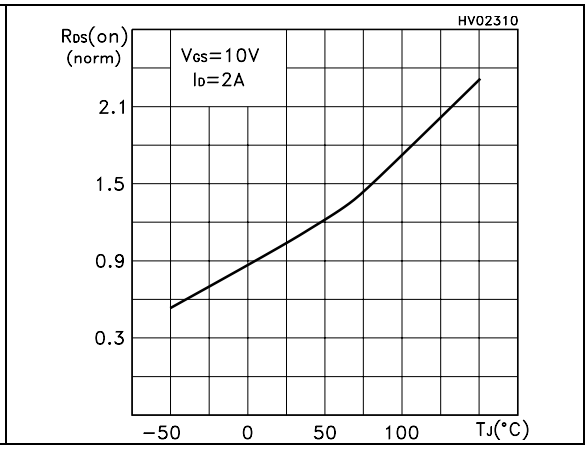
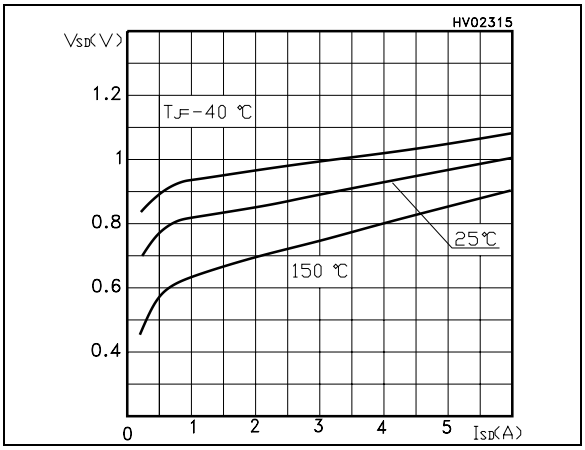


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

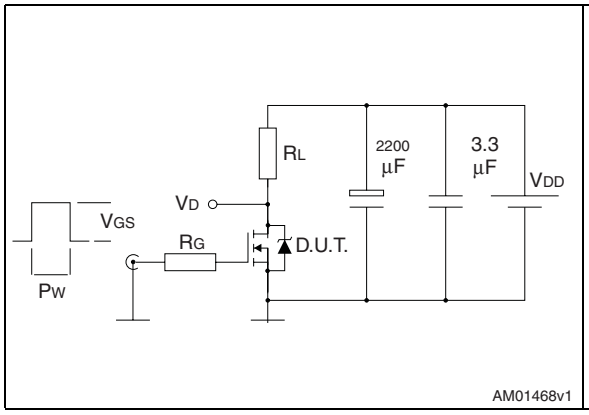


Figure 14. Gate charge test circuit

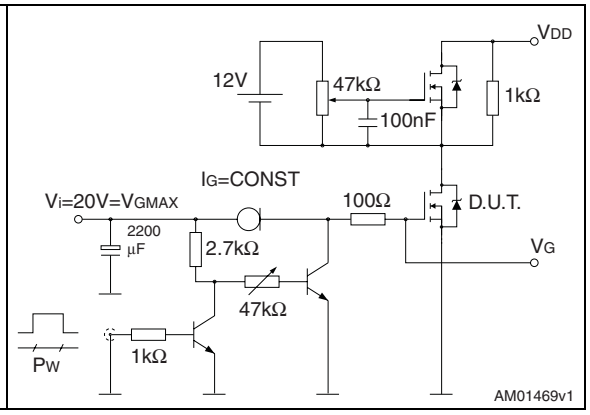


Figure 15. Test circuit for inductive load switching and diode recovery times

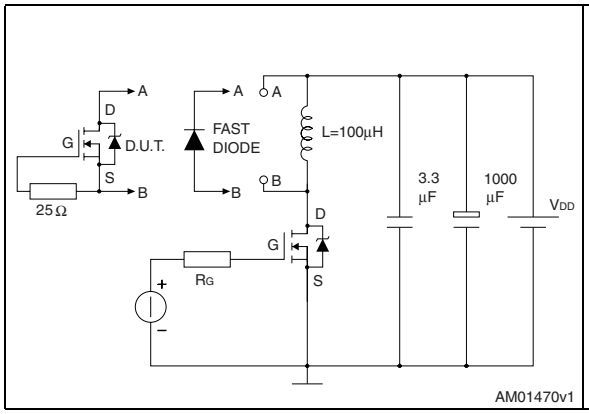


Figure 16. Unclamped inductive load test circuit

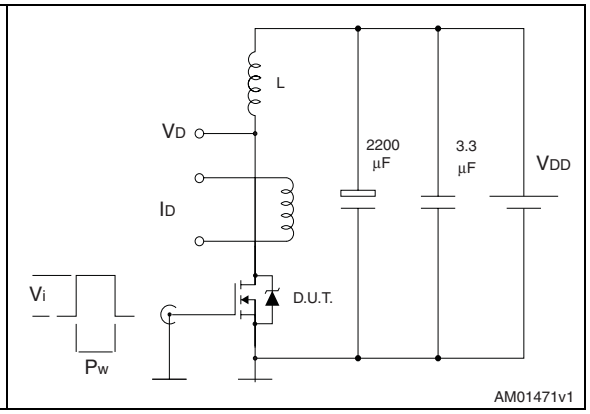


Figure 17. Unclamped inductive waveform

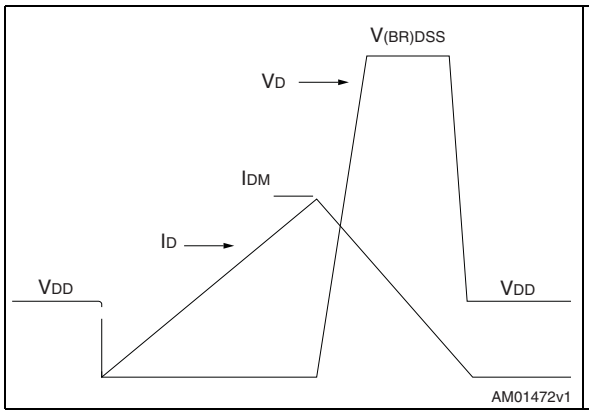
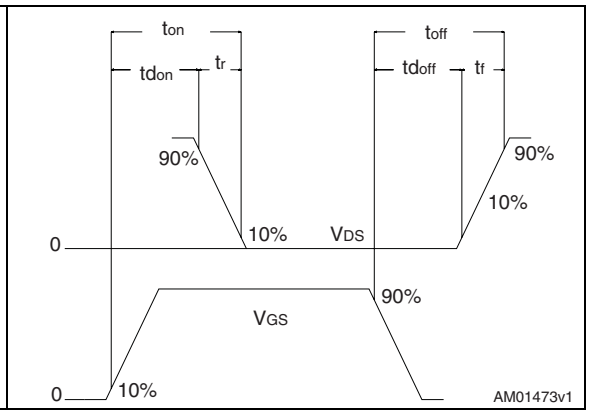


Figure 18. Switching time waveform

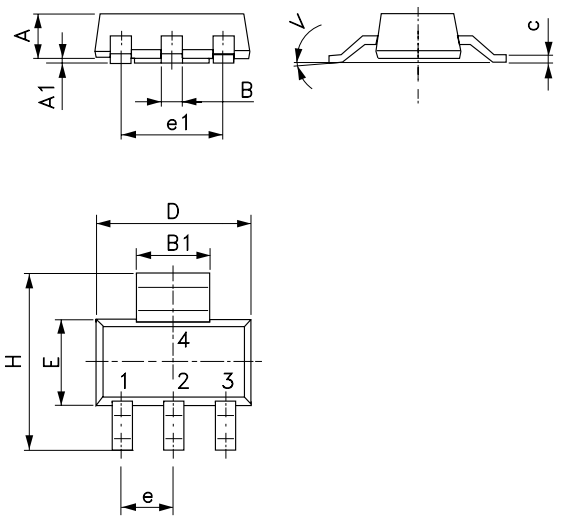


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

SOT-223 mechanical data

DIM.	mm.		
	min.	typ	max.
A			1.80
A1	0.02		0.1
B	0.60	0.70	0.85
B1	2.90	3.00	3.15
c	0.24	0.26	0.35
D	6.30	6.50	6.70
e		2.30	
e1		4.60	
E	3.30	3.50	3.70
H	6.70	7.00	7.30
V			10 °



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
21-Jun-2004	1	First release.
31-Mar-2009	2	Document status promoted from preliminary data to datasheet.

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