

## IRLR8259PbF IRLU8259PbF

HEXFET® Power MOSFET

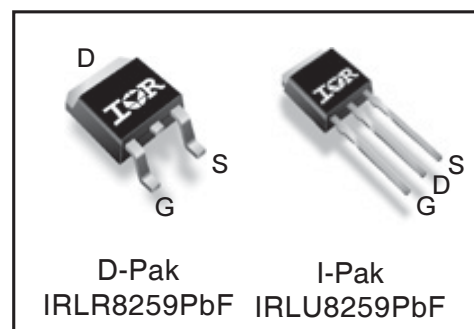
### Applications

- High Frequency Synchronous Buck Converters for Computer Processor Power
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use

$V_{DSS}$	$R_{DS(on) \max}$	$Q_g$
25V	8.7m $\Omega$	6.8nC

### Benefits

- Very Low  $R_{DS(on)}$  at 4.5V  $V_{GS}$
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current
- Lead-Free
- RoHS compliant



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

### Absolute Maximum Ratings

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	25	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	57 <sup>④</sup>	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	40 <sup>④</sup>	
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	230	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation <sup>⑤</sup>	48	W
$P_D @ T_C = 100^\circ\text{C}$	Maximum Power Dissipation <sup>⑤</sup>	24	
	Linear Derating Factor	0.32	W/ $^\circ\text{C}$
$T_J$	Operating Junction and	-55 to + 175	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

### Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	3.15	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) <sup>⑤</sup>	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

#### ORDERING INFORMATION:

See detailed ordering and shipping information on the last page of this data sheet.

Notes <sup>①</sup> through <sup>⑤</sup> are on page 11

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## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

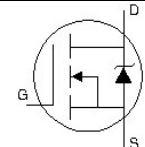
	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	25	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	18	—	mV/°C	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	6.3	8.7	m $\Omega$	$V_{GS} = 10V, I_D = 21A$ ③
		—	10.6	12.9		$V_{GS} = 4.5V, I_D = 17A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.90	2.35	V	$V_{DS} = V_{GS}, I_D = 25\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-7.1	—	mV/°C	
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	$\mu A$	$V_{DS} = 20V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$g_{fs}$	Forward Transconductance	55	—	—	S	$V_{DS} = 13V, I_D = 17A$
$Q_g$	Total Gate Charge	—	6.8	10	nC	$V_{DS} = 13V$ $V_{GS} = 4.5V$ $I_D = 17A$ See Fig. 16
$Q_{gs1}$	Pre-Vth Gate-to-Source Charge	—	1.5	—		
$Q_{gs2}$	Post-Vth Gate-to-Source Charge	—	1.1	—		
$Q_{gd}$	Gate-to-Drain Charge	—	2.4	—		
$Q_{godr}$	Gate Charge Overdrive	—	1.8	—		
$Q_{sw}$	Switch Charge ( $Q_{gs2} + Q_{gd}$ )	—	3.5	—		
$Q_{oss}$	Output Charge	—	5.9	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
$R_G$	Gate Resistance	—	2.2	3.6	$\Omega$	
$t_{d(on)}$	Turn-On Delay Time	—	8.4	—	ns	$V_{DD} = 13V, V_{GS} = 4.5V$ ③ $I_D = 17A$ $R_G = 1.8\Omega$ See Fig. 14
$t_r$	Rise Time	—	38	—		
$t_{d(off)}$	Turn-Off Delay Time	—	9.1	—		
$t_f$	Fall Time	—	8.9	—		
$C_{iss}$	Input Capacitance	—	900	—	pF	$V_{GS} = 0V$ $V_{DS} = 13V$ $f = 1.0MHz$
$C_{oss}$	Output Capacitance	—	300	—		
$C_{rss}$	Reverse Transfer Capacitance	—	110	—		

## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy ②	—	67	mJ
$I_{AR}$	Avalanche Current ①	—	17	A
$E_{AR}$	Repetitive Avalanche Energy ①	—	4.8	mJ

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	56 ④	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	230		
$V_{SD}$	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 17A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	17	26	ns	$T_J = 25^\circ\text{C}, I_F = 17A, V_{DD} = 13V$
$Q_{rr}$	Reverse Recovery Charge	—	15	23	nC	$di/dt = 200A/\mu s$ ③
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				



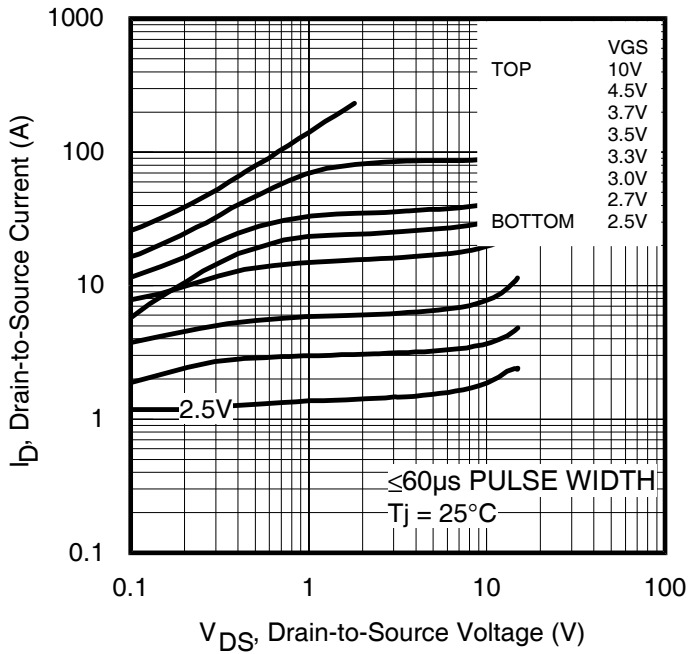


Fig 1. Typical Output Characteristics

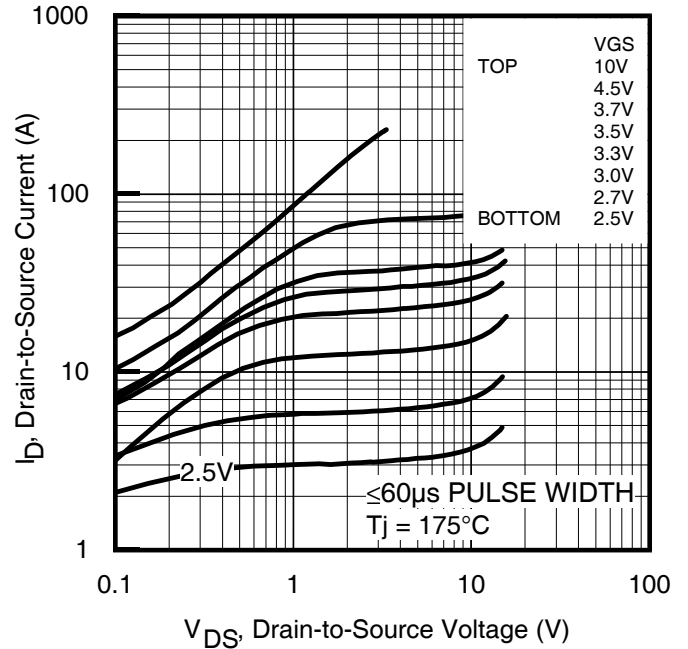


Fig 2. Typical Output Characteristics

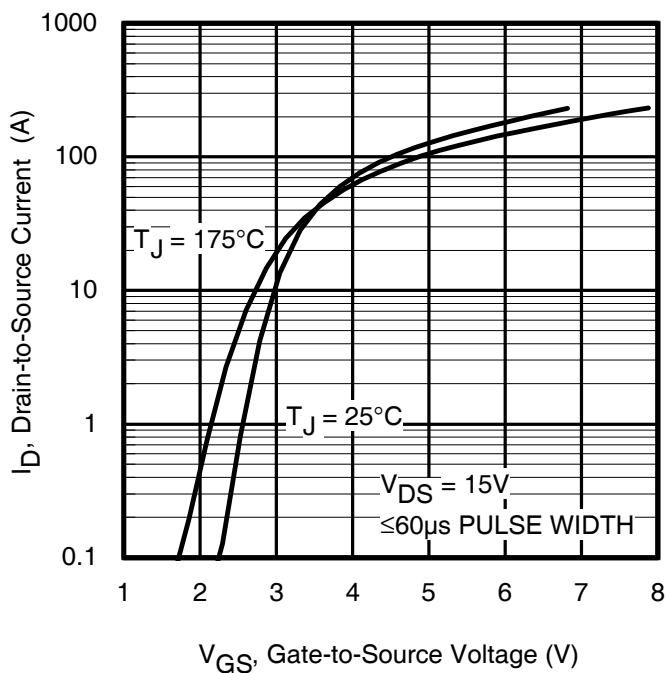


Fig 3. Typical Transfer Characteristics

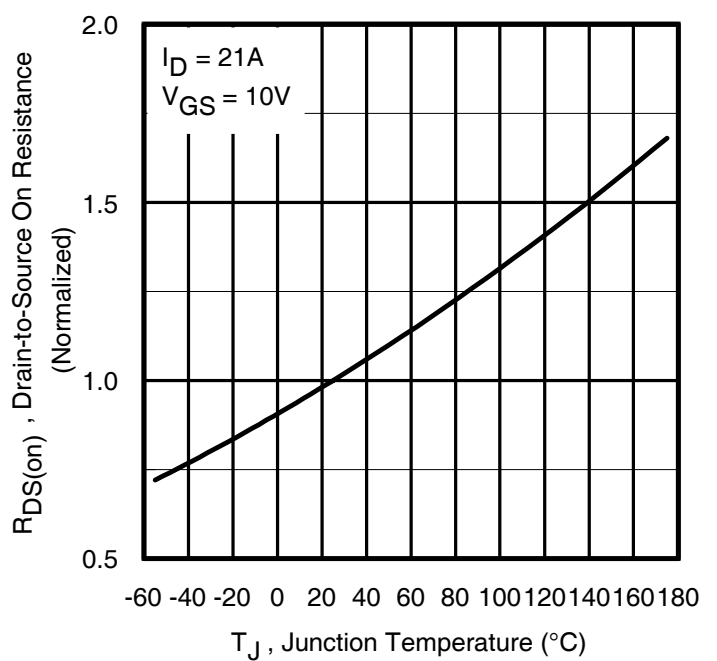
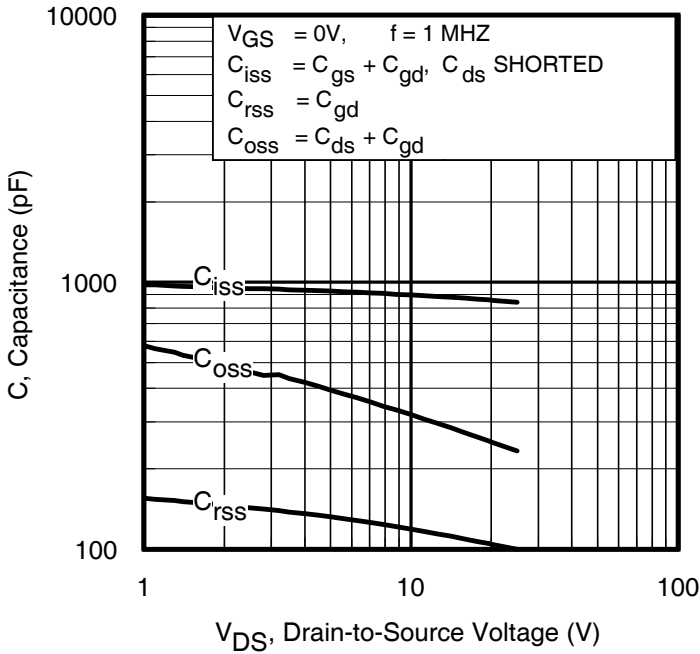
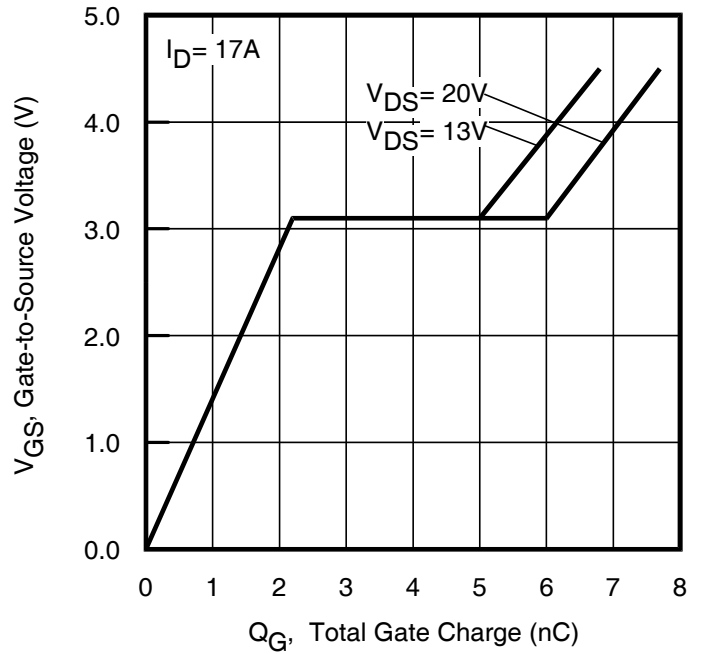


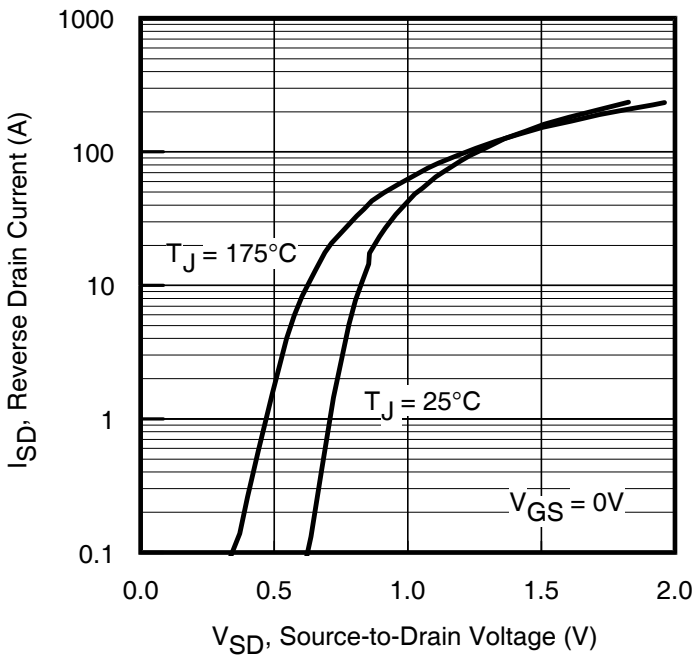
Fig 4. Normalized On-Resistance vs. Temperature



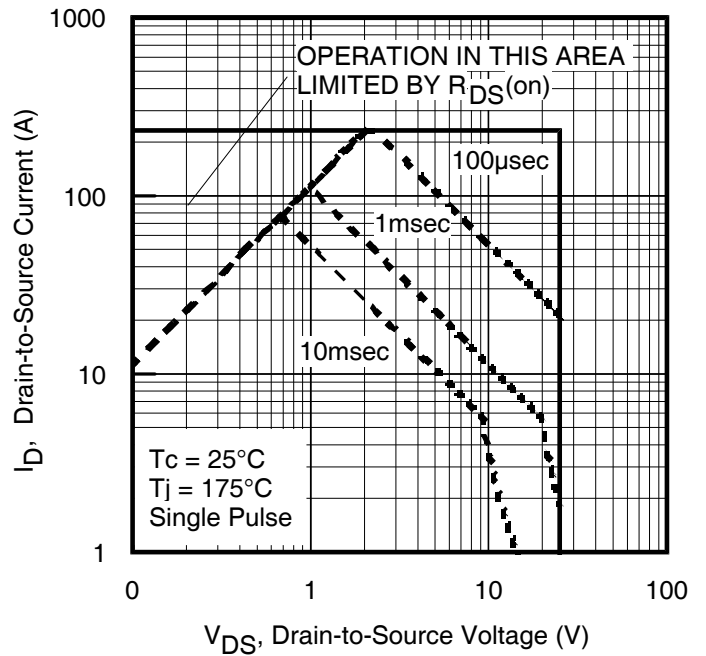
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



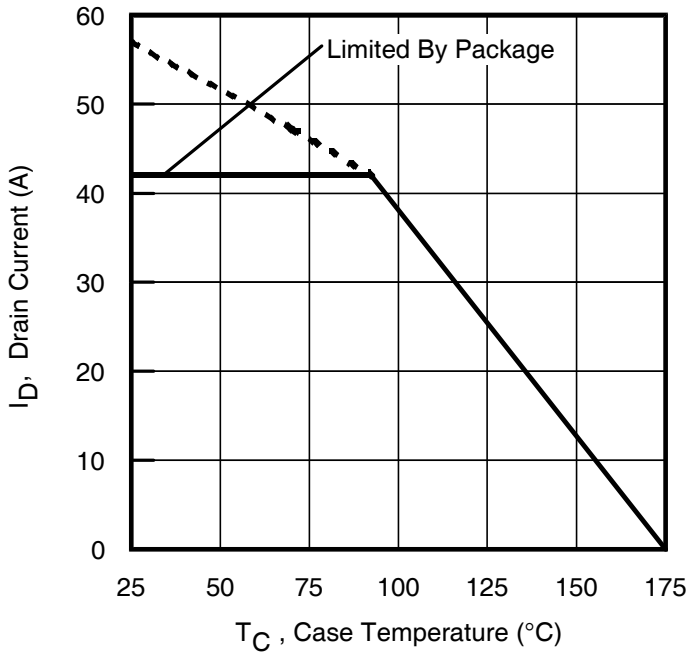
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



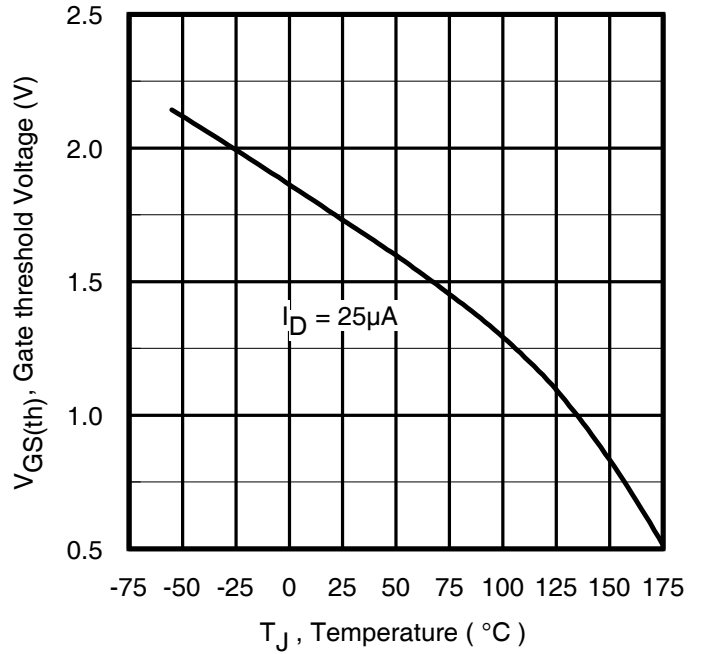
**Fig 7.** Typical Source-Drain Diode Forward Voltage



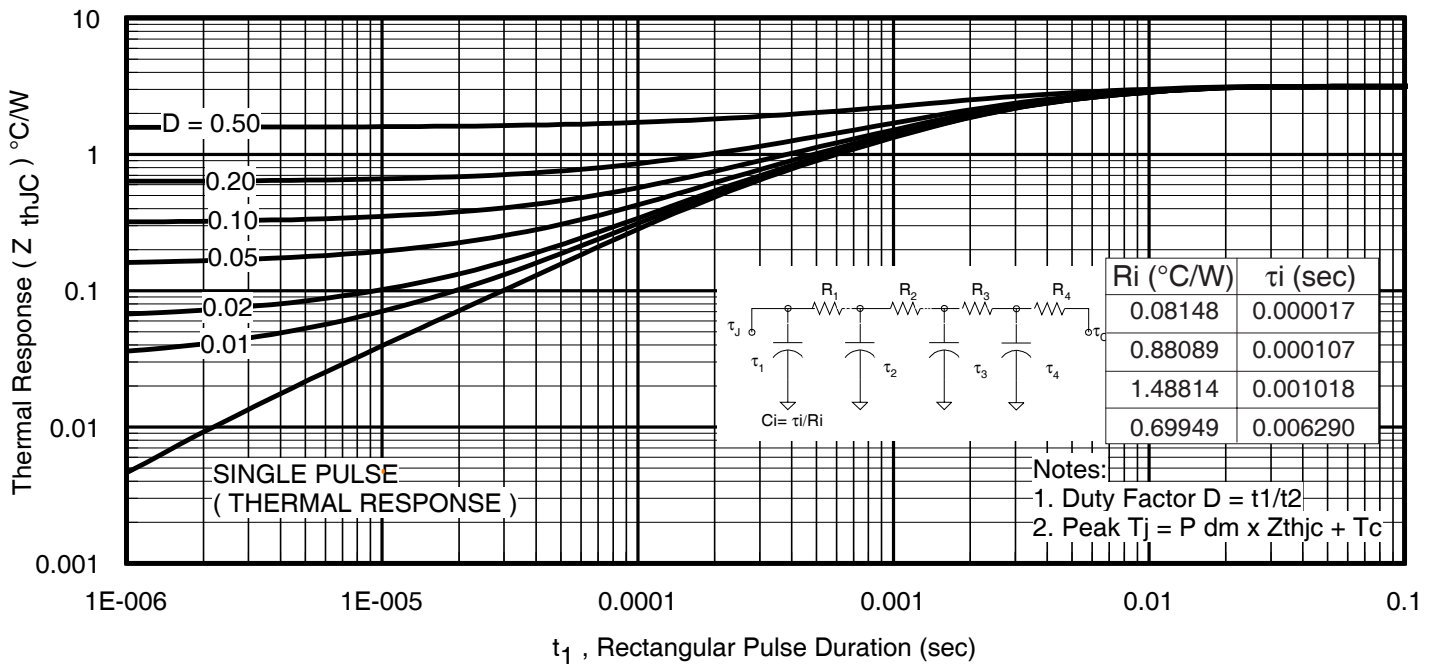
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current vs. Case Temperature

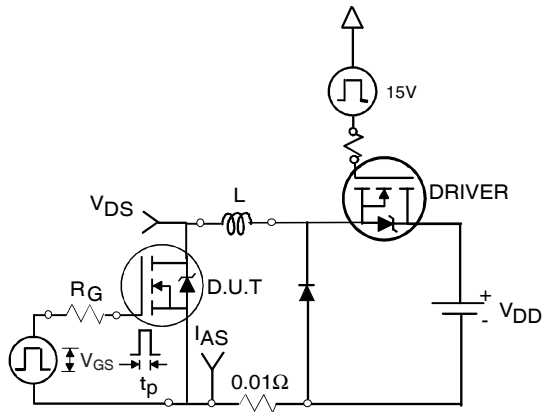


**Fig 10.** Threshold Voltage vs. Temperature

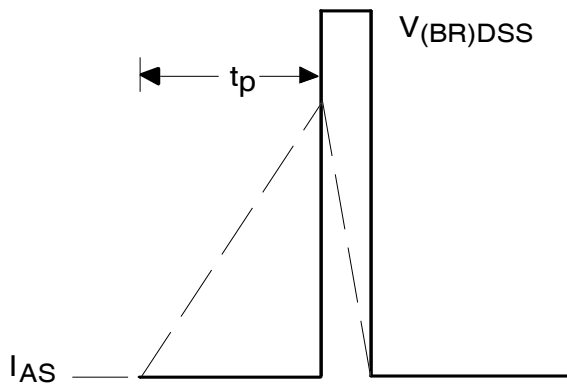


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

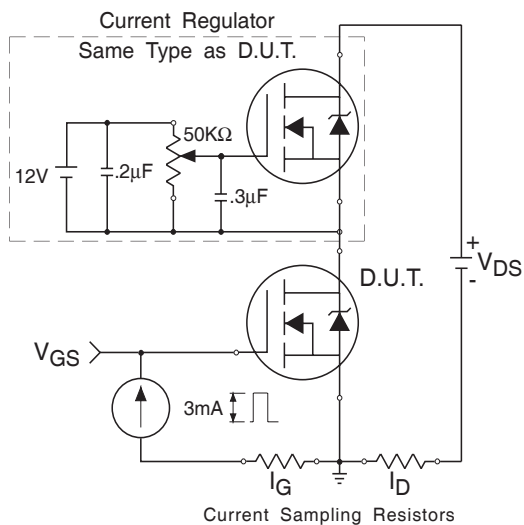
# IRLR/U8259PbF



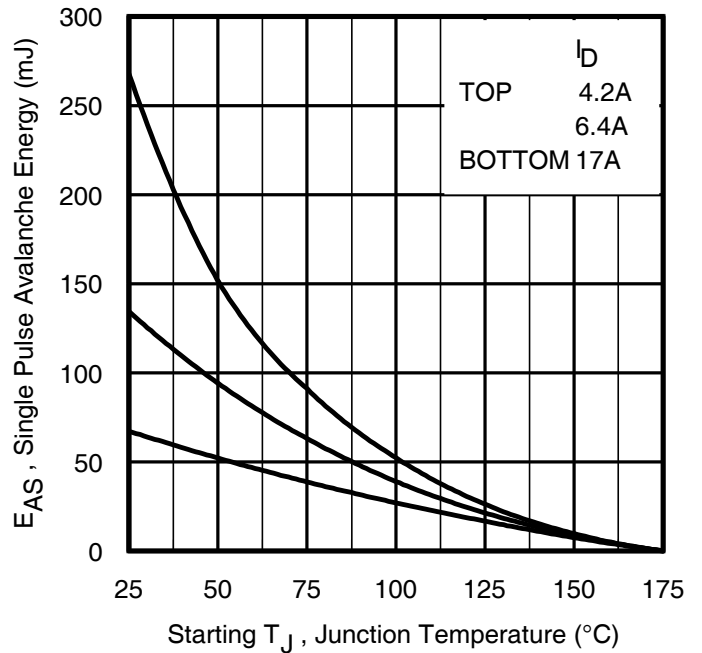
**Fig 12a.** Unclamped Inductive Test Circuit



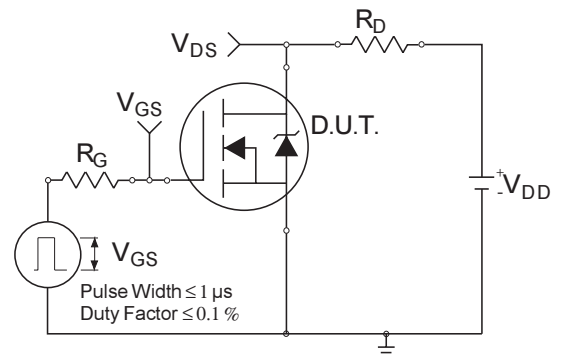
**Fig 12b.** Unclamped Inductive Waveforms



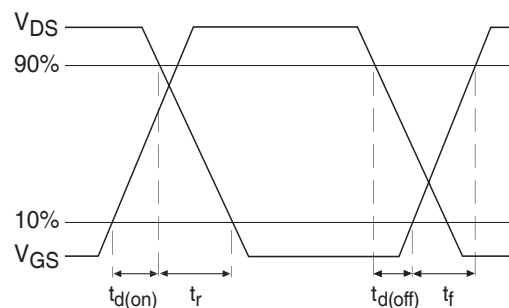
**Fig 13.** Gate Charge Test Circuit



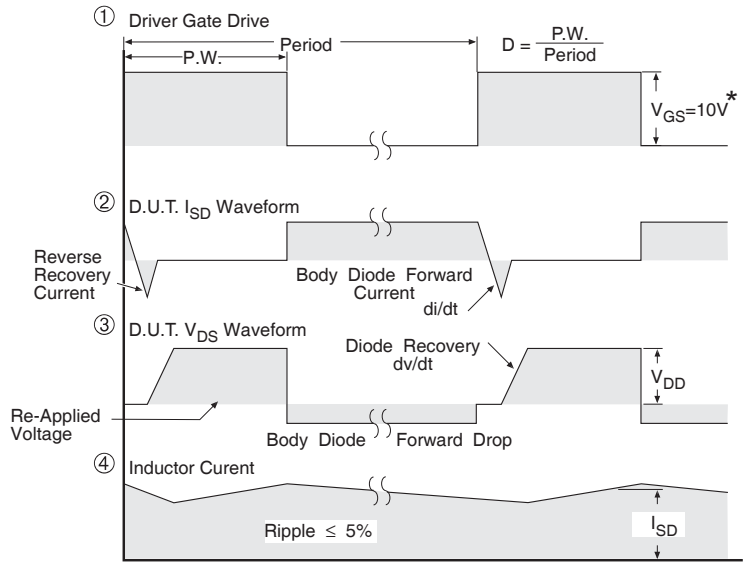
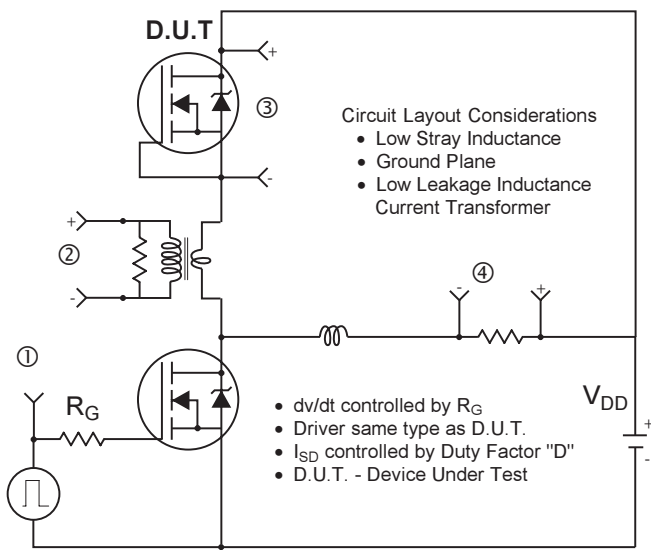
**Fig 12c.** Maximum Avalanche Energy vs. Drain Current



**Fig 14a.** Switching Time Test Circuit

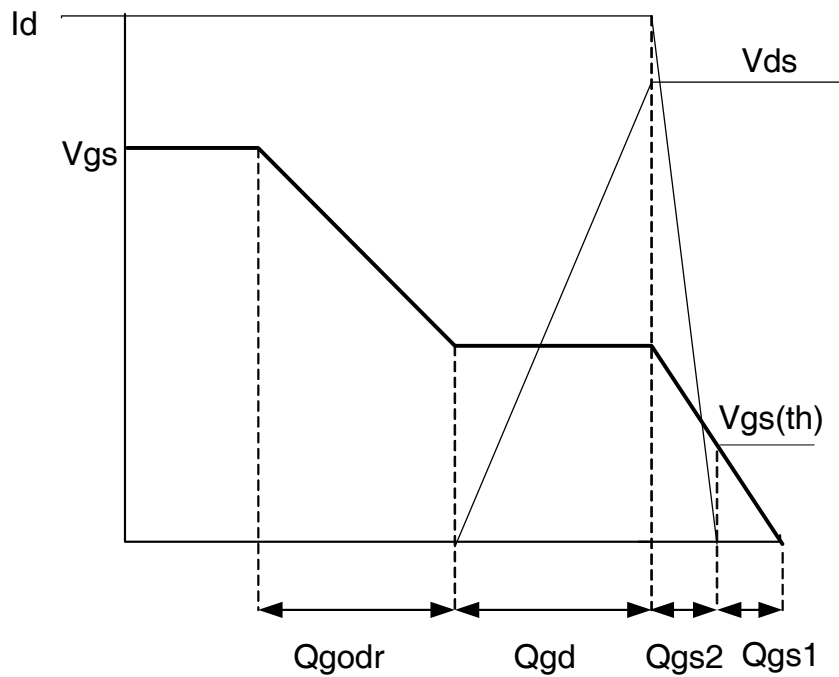


**Fig 14b.** Switching Time Waveforms



\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 15. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET<sup>®</sup> Power MOSFETs**

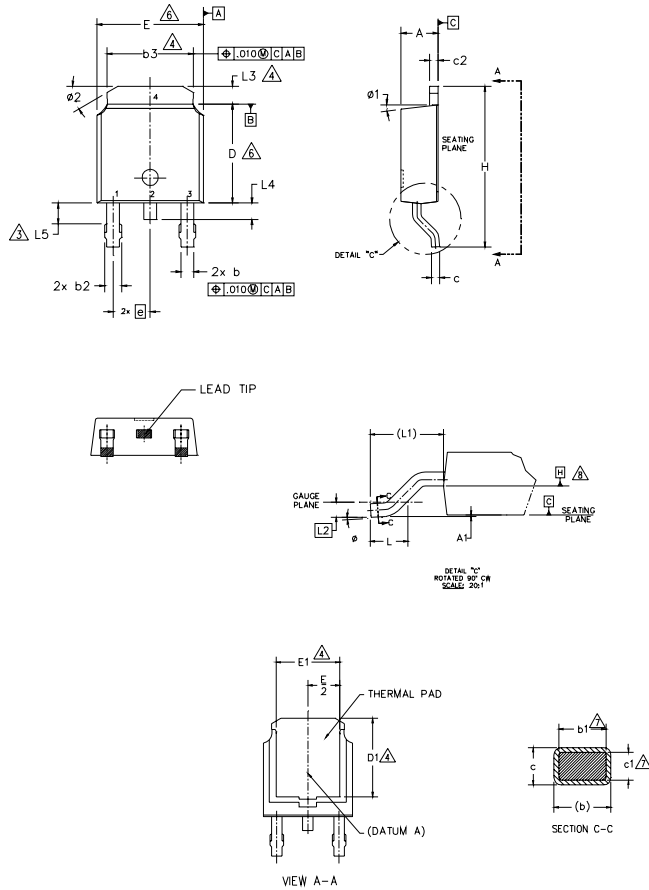


**Fig 16. Gate Charge Waveform**

# IRLR/U8259PbF

## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- △ LEAD DIMENSION UNCONTROLLED IN L5.
- △- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- △- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- △- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- △- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
∅	0"	10"	0"	10"	
∅1	0"	15"	0"	15"	
∅2	25"	35"	25"	35"	

**LEAD ASSIGNMENTS**

**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBT & CoPAK**

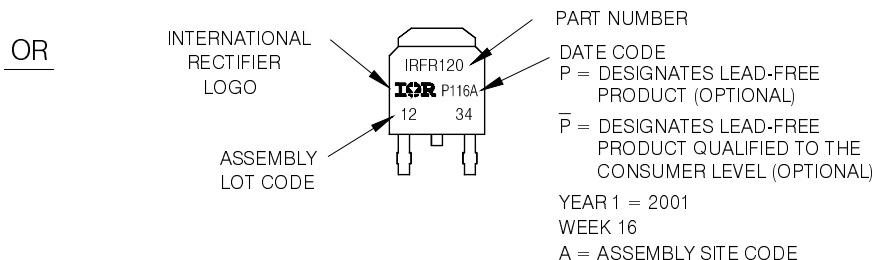
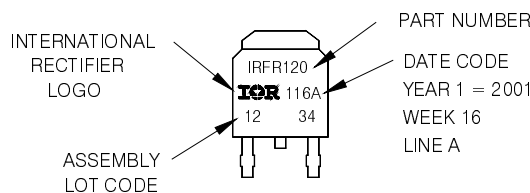
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 2001  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates "Lead-Free"

"P̄" in assembly line position indicates  
"Lead-Free" qualification to the consumer-level

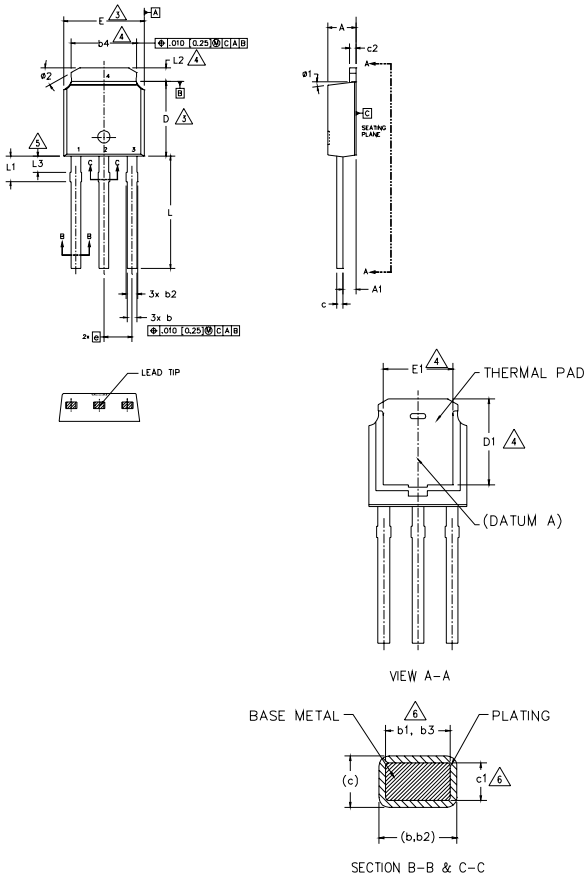


**Note:** For the most current drawing please refer to IR website at <http://www.irf.com/package/>



## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  - 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  4. THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
  5. LEAD DIMENSION UNCONTROLLED IN L3.
  6. DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
  - 7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).
  - 8.- CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.89	1.14	.035	.045	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	6
b2	0.76	1.14	.030	.045	
b3	0.76	1.04	.030	.041	6
b4	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	6
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	3
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
L	8.89	9.65	.350	.380	
L1	1.91	2.29	.045	.090	
L2	0.89	1.27	.035	.050	4
L3	1.14	1.52	.045	.060	5
Ø1	0"	15"	0"	15"	
Ø2	25"	35"	25"	35"	

LEAD ASSIGNMENTS

HEXFET

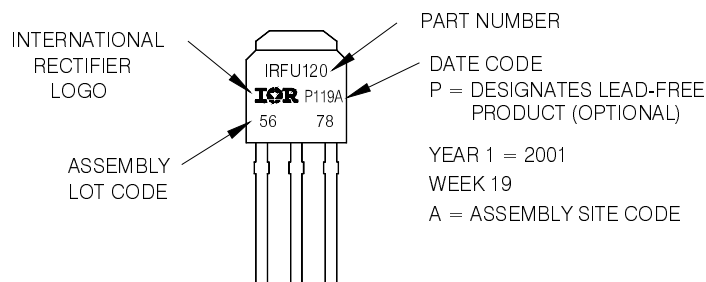
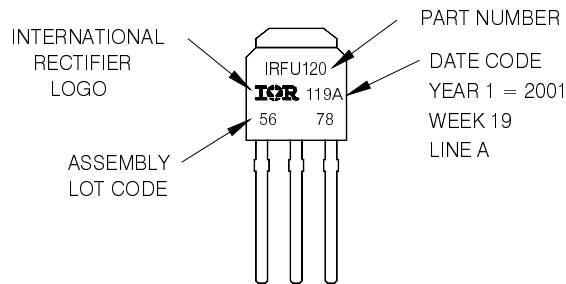
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
WITH ASSEMBLY  
LOT CODE 5678  
ASSEMBLED ON WW 19, 2001  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates Lead-Free"

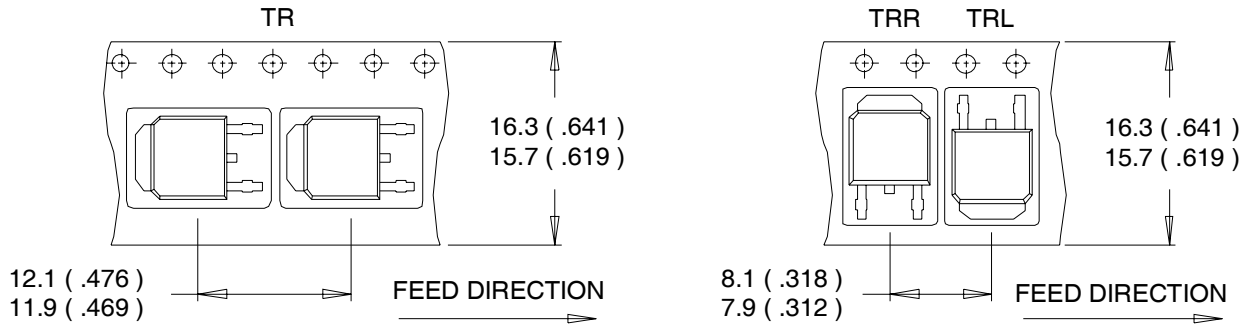
OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>  
[www.irf.com](http://www.irf.com)

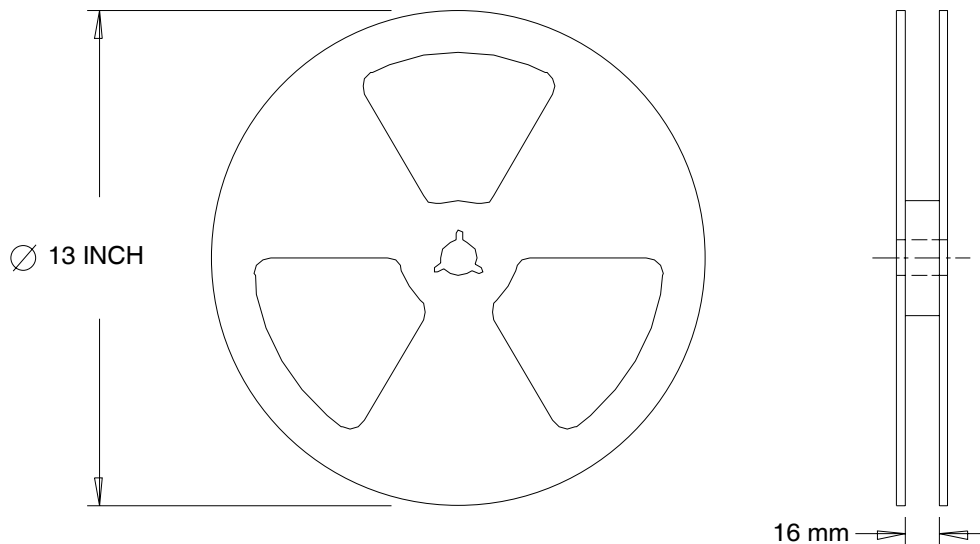
## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

**Note:** For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRLR8259PBF	D-PAK	Tube/Bulk	75	
IRLR8259TRPBF	D-PAK	Tape and Reel	2000	
IRLU8259PBF	I-PAK	Tube/Bulk	75	

Qualification information†		
Qualification level	Industrial†† (per JEDEC JESD47F††† guidelines)	
	Comments: This family of products has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level	D-PAK	MSL1 (per JEDEC J-ST D-020D†††)
	I-PAK	Not applicable
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/product-info/reliability>  
 †† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: <http://www.irf.com/whoto-call/salesrep/>  
 ††† Applicable version of JEDEC standard at the time of product release.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.48\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 17\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④ Calculated continuous current based on maximum allowable junction temperature.  
 Package limitation current is 42A.
- ⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.



**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
 TAC Fax: (310) 252-790

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