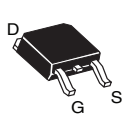


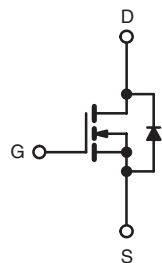
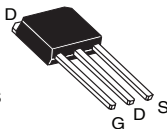
## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	60
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 5.0$ V   0.10
$Q_g$ (Max.) (nC)	18
$Q_{gs}$ (nC)	4.5
$Q_{gd}$ (nC)	12
Configuration	Single

DPAK (TO-252)



IPAK (TO-251)



N-Channel MOSFET

### FEATURES

- Dynamic dV/dt Rating
- Surface Mount (IRLR024/SiHLR024)
- Straight Lead (IRLU024/SiHLU024)
- Available in Tape and Reel
- Logic-Level Gate Drive
- $R_{DS(on)}$  Specified at  $V_{GS} = 4$  V and 5 V
- Fast Switching
- Lead (Pb)-free Available



Available  
**RoHS\***  
COMPLIANT

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRLU/SiHLU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION			
Package	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free	IRLR024PbF	IRLR024TRPbF <sup>a</sup>	IRLU024PbF
	SiHLR024-E3	SiHLR024T-E3 <sup>a</sup>	SiHLU024-E3
SnPb	IRLR024	IRLR024TR <sup>a</sup>	IRLU024
	SiHLR024	SiHLR024T <sup>a</sup>	SiHLU024

#### Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 10$	
Continuous Drain Current	$V_{GS}$ at 5.0 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	56	W/°C
Linear Derating Factor		0.33	
Linear Derating Factor (PCB Mount) <sup>e</sup>		0.020	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	91	mJ
Maximum Power Dissipation	$P_D$	$T_C = 25$ °C	W
		$T_A = 25$ °C	
Maximum Power Dissipation (PCB Mount) <sup>e</sup>		2.5	
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	260 <sup>d</sup>	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$  V, starting  $T_J = 25$  °C,  $L = 541$   $\mu$ H,  $R_G = 25$   $\Omega$ ,  $I_{AS} = 14$  A (see fig. 12).
- $I_{SD} \leq 17$  A,  $di/dt \leq 140$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	-	110	°C/W
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	-	50	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	-	3.0	

### Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$		60	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.068	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$		1.0	-	2.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 10\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{ V}$ , $V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 48\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 5.0\text{ V}$	$I_D = 8.4\text{ A}^b$	-	-	0.10	$\Omega$
		$V_{GS} = 4.0\text{ V}$	$I_D = 7.0\text{ A}^b$	-	-	0.14	
Forward Transconductance	$g_{fs}$	$V_{DS} = 25\text{ V}$ , $I_D = 8.4\text{ A}^b$		7.3	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5		-	870	-	pF
Output Capacitance	$C_{oss}$			-	360	-	
Reverse Transfer Capacitance	$C_{rss}$			-	53	-	
Total Gate Charge	$Q_g$	$V_{GS} = 5.0\text{ V}$	$I_D = 17\text{ A}$ , $V_{DS} = 48\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	18	nC
Gate-Source Charge	$Q_{gs}$			-	-	4.5	
Gate-Drain Charge	$Q_{gd}$			-	-	12	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}$ , $I_D = 17\text{ A}$ , $R_G = 9.0\text{ }\Omega$ , $R_D = 1.7\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	11	-	ns
Rise Time	$t_r$			-	110	-	
Turn-Off Delay Time	$t_{d(off)}$			-	23	-	
Fall Time	$t_f$			-	41	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact <sup>c</sup>		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	14	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	56	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_S = 14\text{ A}$ , $V_{GS} = 0\text{ V}^b$		-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_F = 17\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	130	260	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.75	1.5	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

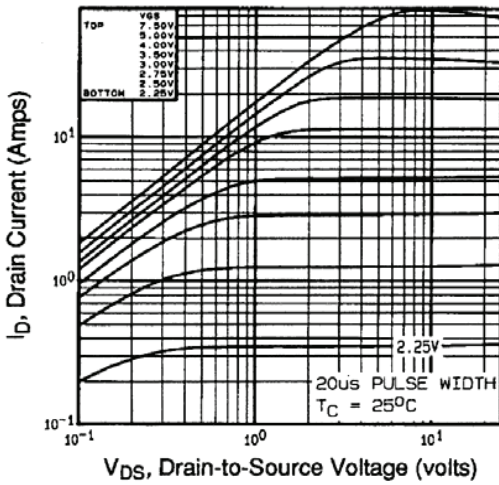


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$

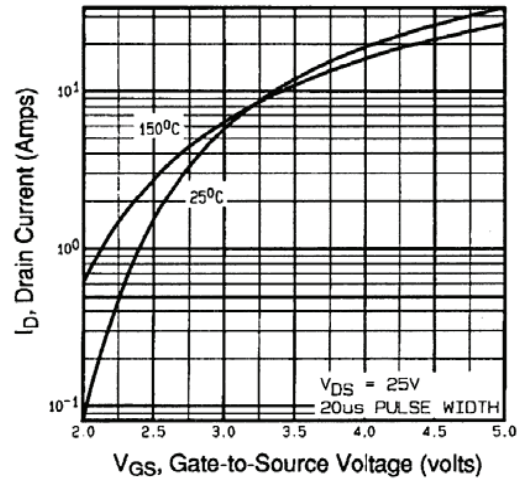


Fig. 3 - Typical Transfer Characteristics

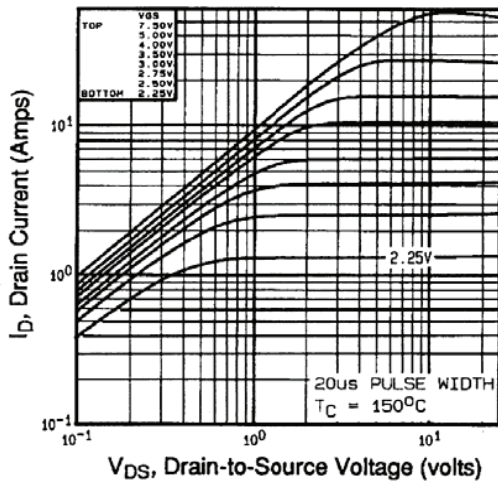


Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$

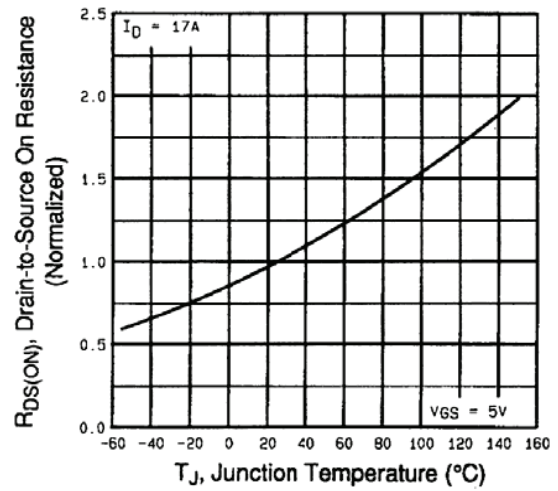


Fig. 4 - Normalized On-Resistance vs. Temperature

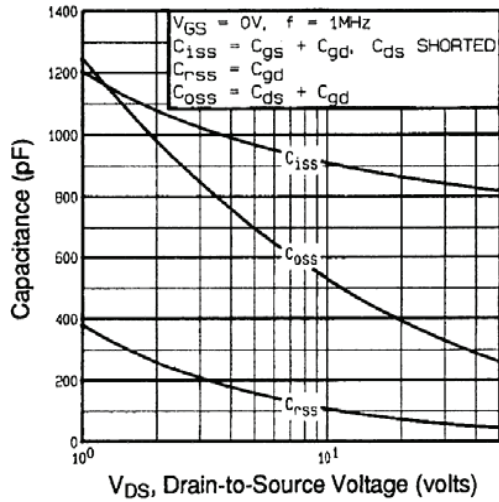


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

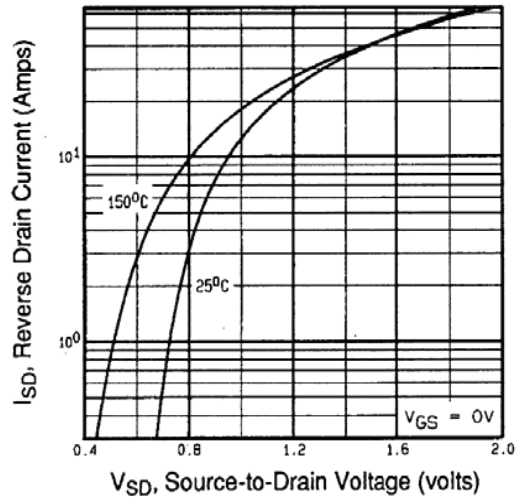


Fig. 7 - Typical Source-Drain Diode Forward Voltage

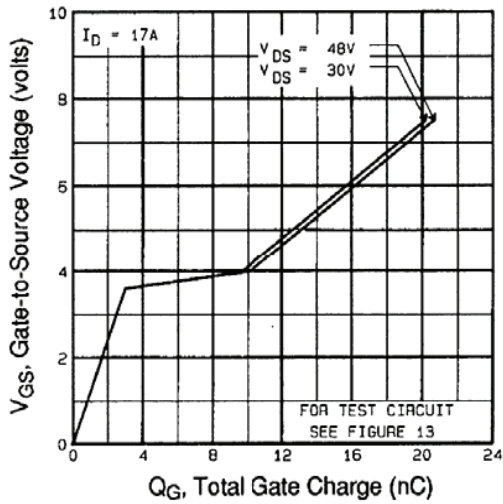


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

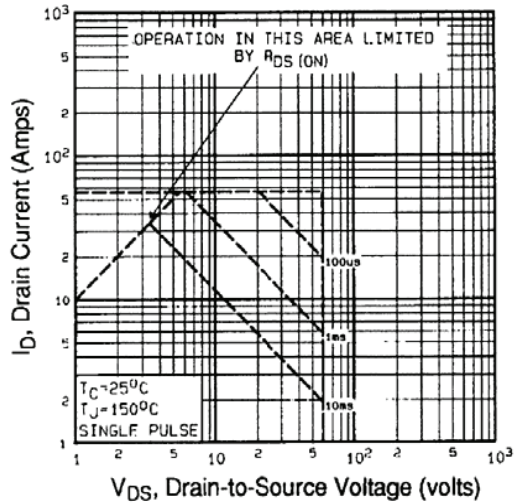


Fig. 8 - Maximum Safe Operating Area

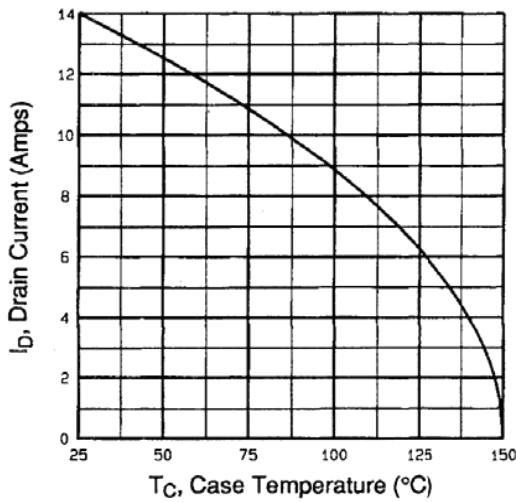


Fig. 9 - Maximum Drain Current vs. Case Temperature

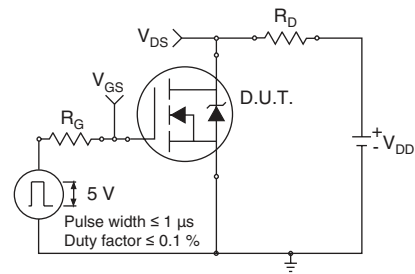


Fig. 10a - Switching Time Test Circuit

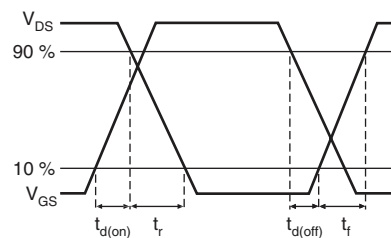


Fig. 10b - Switching Time Waveforms

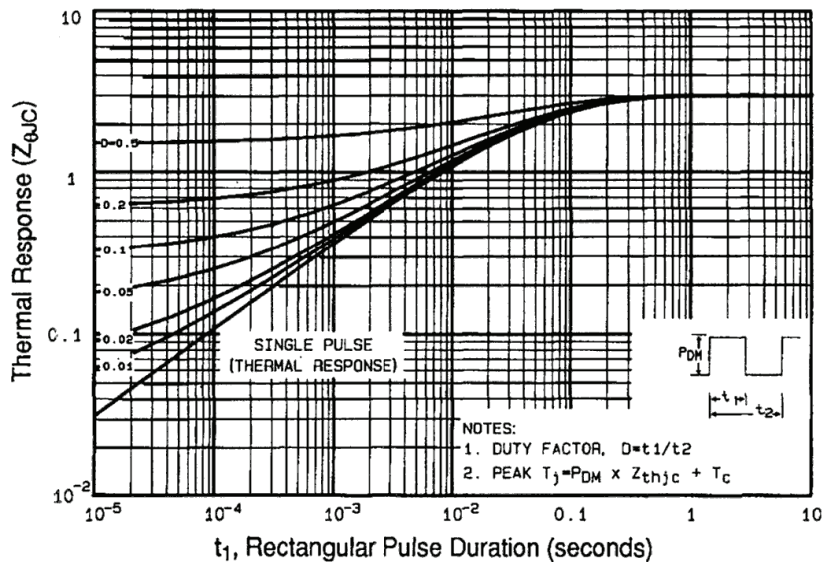


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

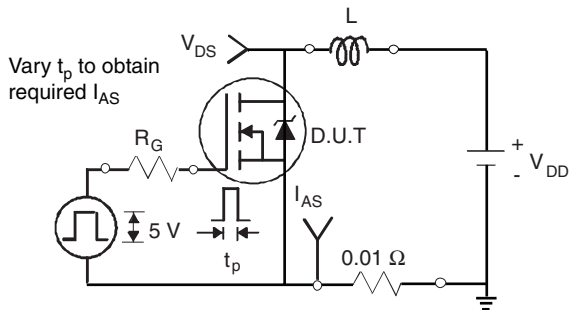


Fig. 12a - Unclamped Inductive Test Circuit

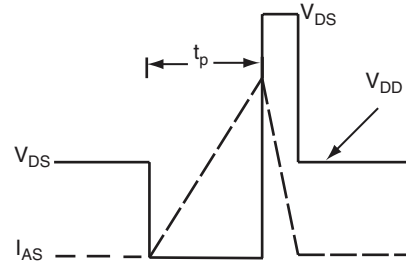


Fig. 12b - Unclamped Inductive Waveforms

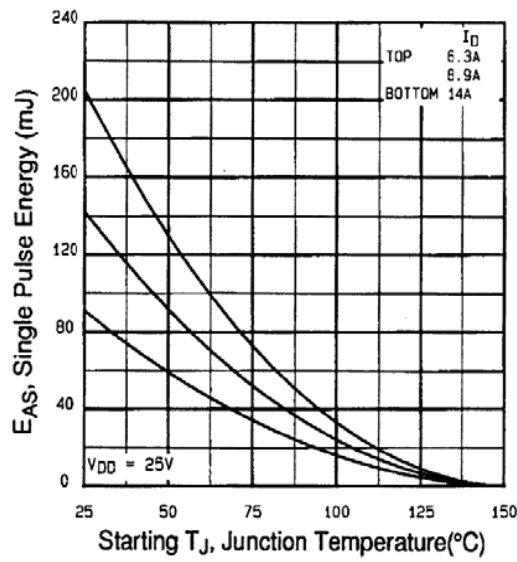


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

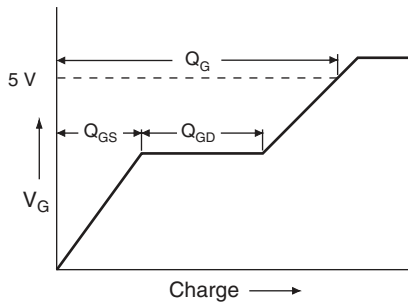


Fig. 13a - Basic Gate Charge Waveform

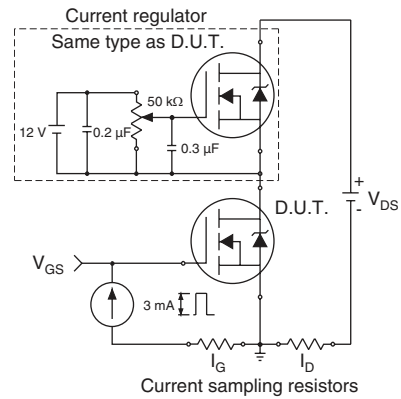
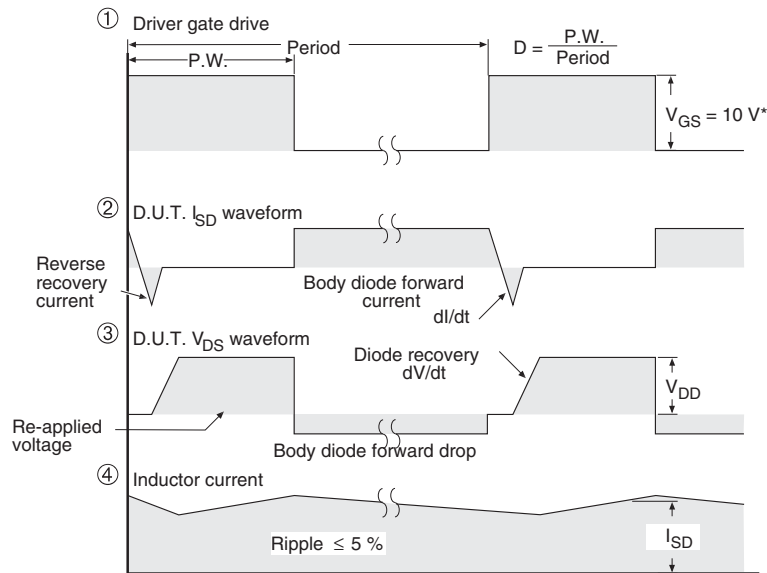
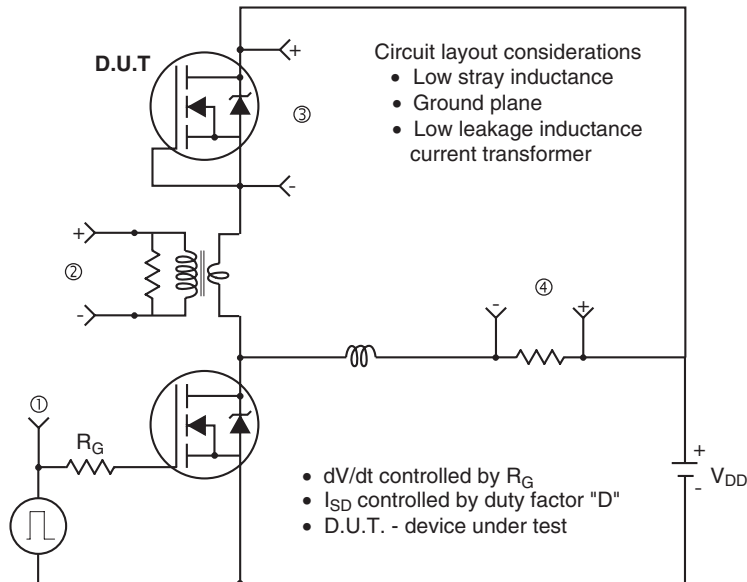


Fig. 13b - Gate Charge Test Circuit

## Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = 5 V$  for logic level and  $3 V$  drive devices

**Fig. 14 - For N-Channel**

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