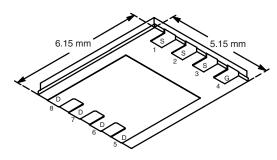




N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A) ^f	Q _g (Typ.)		
40	0.009 at V _{GS} = 10 V	47	15 nC		
	0.012 at V _{GS} = 4.5 V	40			

PowerPAK® SO-8



Bottom View

Ordering Information: Si7848BDP-T1-E3 (Lead (Pb)-free)

Si7848BDP-T1-GE3 (Lead (Pb)-free and Halogen-free)

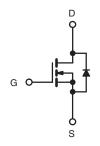
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS directive 2002/95/EC



APPLICATIONS

- DC/DC Converters
 - Synchronous Buck
 - Synchronous Rectifier



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
	Symbol	Limit	Unit		
Drain-Source Voltage		40	v		
Gate-Source Voltage		± 20			
$T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 70 ^{\circ}\text{C}$ $T_{A} = 25 ^{\circ}\text{C}$ $T_{A} = 70 ^{\circ}\text{C}$	I _D	47 38 16 ^{a, b} 12 8 ^{a, b}	A		
Pulsed Drain Current Avalanche Current		50 15	-		
L = 0.1 MH	E _{AS}	11	mJ		
Continuous Source-Drain Diode Current $ T_{C} = 25 ^{\circ}\text{C} $ $ T_{A} = 25 ^{\circ}\text{C} $		30 3.5 ^{a, b}	Α		
$T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 70 ^{\circ}\text{C}$ $T_{A} = 25 ^{\circ}\text{C}$ $T_{A} = 70 ^{\circ}\text{C}$	P _D	36 23 4.2 ^{a, b} 2.7 ^{a, b}	w		
Operating Junction and Storage Temperature Range Soldering Recommendations (Peak Temperature) ^{c, d}		- 55 to 150	°C		
	$T_{C} = 25 ^{\circ}C$ $T_{C} = 70 ^{\circ}C$ $T_{A} = 25 ^{\circ}C$ $T_{A} = 70 ^{\circ}C$ $T_{C} = 25 ^{\circ}C$ $T_{C} = 25 ^{\circ}C$ $T_{C} = 25 ^{\circ}C$ $T_{C} = 25 ^{\circ}C$ $T_{C} = 70 ^{\circ}C$	$\begin{array}{c c} & \textbf{Symbol} \\ & V_{DS} \\ \hline & V_{GS} \\ \hline & T_C = 25 ^{\circ}\text{C} \\ \hline & T_C = 70 ^{\circ}\text{C} \\ \hline & T_A = 25 ^{\circ}\text{C} \\ \hline & T_A = 70 ^{\circ}\text{C} \\ \hline & I_{DM} \\ \hline & I_{AS} \\ \hline & I_{C} = 25 ^{\circ}\text{C} \\ \hline & T_A = 25 ^{\circ}\text{C} \\ \hline & T_C = 70 ^{\circ}\text{C} \\ \hline & T_A = 25 ^{\circ}\text{C} \\ \hline & T_A = 70 ^{\circ}\text{C} \\ \hline & T_A = 70 ^{\circ}\text{C} \\ \hline & T_D = 70 ^{\circ}$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol Typical		Maximum	Unit	
Maximum Junction-to-Ambient ^{a, e}	t ≤ 10 s	R _{thJA}	25	30	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R _{th.IC}	2.9	3.5	- O/VV	

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. t = 10 s.
- c. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- d. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- e. Maximum under Steady State conditions is 70 °C/W.
- f. Based on $T_C = 25$ °C.

Si7848BDP

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SPECIFICATIONS $T_J = 25 ^{\circ}C$, Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static				1 -76-	1 114111	1	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	40			V	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Vne/Tu		40			
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 6		mV/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu A$	1		3	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current		V _{DS} = 40 V, V _{GS} = 0 V			1	μΑ	
	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C			5		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	50			Α	
	R _{DS(on)}	V _{GS} = 10 V, I _D = 16 A		0.0074	0.009	Ω	
Drain-Source On-State Resistance ^a		V _{GS} = 4.5 V, I _D = 13.8 A		0.0095	0.012		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 16 A		56		S	
Dynamic ^b				•			
Input Capacitance	C _{iss}			2000		pF	
Output Capacitance	C _{oss}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		260			
Reverse Transfer Capacitance	C _{rss}			150			
Total Gate Charge		V _{DS} = 10 V, V _{GS} = 10 V, I _D = 16 A		33	50	nC	
	Q _g			15	23		
Gate-Source Charge	Q_{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 16 \text{ A}$		6.7			
Gate-Drain Charge	Q_gd			5.1			
Gate Resistance	R_g	f = 1 MHz		1.4	2.1	Ω	
Turn-On Delay Time	t _{d(on)}			25	40	ns	
Rise Time	t _r	$V_{DD} = 20 \text{ V}, R_L = 2 \Omega$		12	20		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		25	40		
Fall Time	t _f			10	15		
Turn-On Delay Time	t _{d(on)}			10	15		
Rise Time	t _r	V_{DD} = 20 V, R_L = 2 Ω		15	25		
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω		30	45		
Fall Time	t _f			10	15		
Drain-Source Body Diode Characteristi	cs						
Continuous Source-Drain Diode Current	I _S	$T_C = 25 ^{\circ}C$			30	Α	
Pulse Diode Forward Current	I _{SM}				50	_ ^	
Body Diode Voltage	V_{SD}	I _S = 10 A, V _{GS} = 0 V		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			30	60	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	L = 10 A dl/dt = 100 A/vo T = 25 °C		26	52	nC	
Reverse Recovery Fall Time	t _a	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 °C$		17.5			
Reverse Recovery Rise Time t _b			12.5		ns		

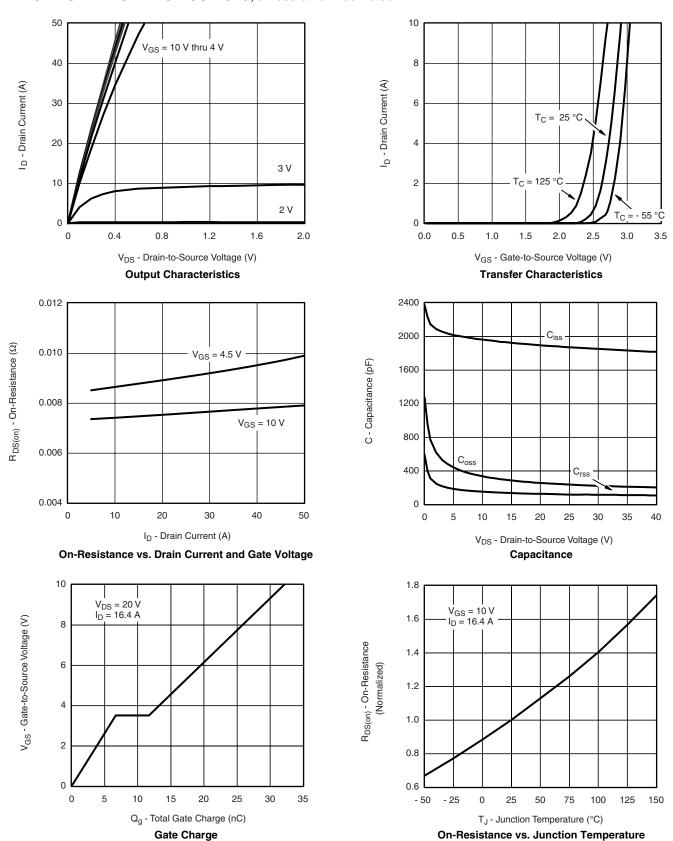
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



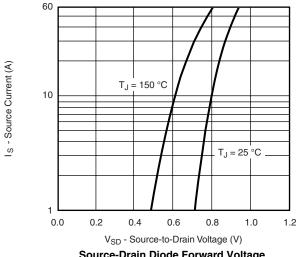
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 $I_D = 18 A$

125 °C

25 °C

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





0.030

0.025

0.020

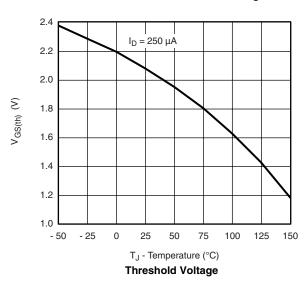
0.015

0.010

0.005

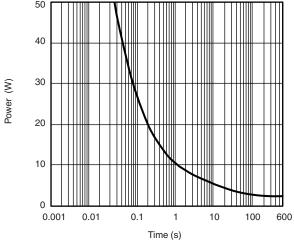
R_{DS(on)} - On-Resistance (Ω)



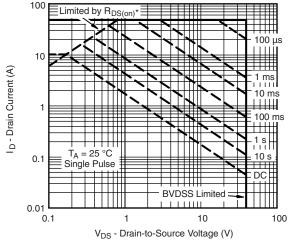




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power (Junction-to-Ambient)



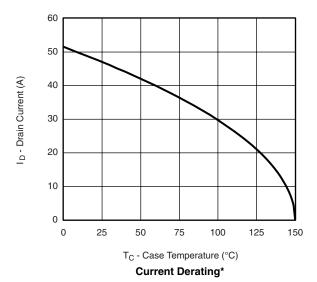
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified Safe Operating Area, Junction-to-Ambient

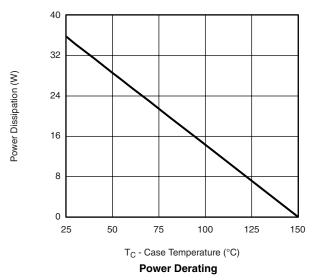




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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



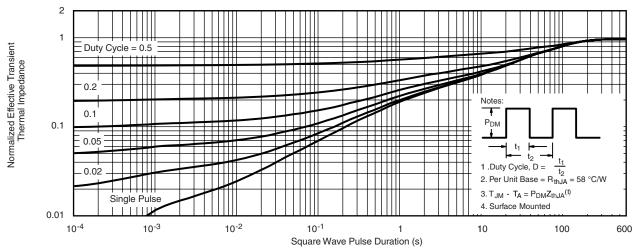


^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

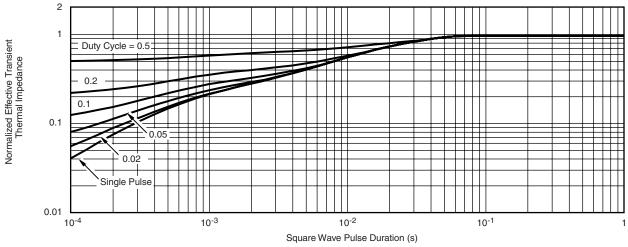
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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