

N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ZVN4424A/C

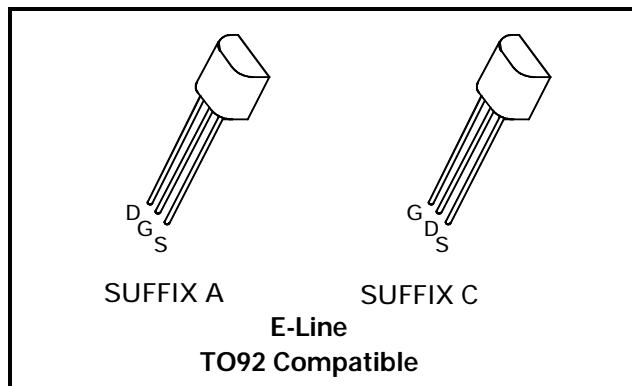
ISSUE 3 – August 1994

FEATURES

- * Compact E-LINE (TO92 style) package
- * 240 Volt V_{DS}
- * $R_{DS(on)}=4.3\Omega$ Typical at $V_{GS}=2.5V$
- * Low threshold
- * Fast switching

APPLICATIONS

- * Earth recall and dialling switches
- * Electronic hook switches
- * Battery powered equipment
- * Telecoms and high voltage dc-dc converters



ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	240	V
Continuous Drain Current at $T_{amb}=25^{\circ}C$	I_D	260	mA
Pulsed Drain Current	I_{DM}	1.5	A
Gate Source Voltage	V_{GS}	± 40	V
Power Dissipation at $T_{amb}=25^{\circ}C$	P_{tot}	750	mW
Operating and Storage Temperature Range	$T_j; T_{stg}$	-55 to +150	$^{\circ}C$

TYPICAL CHARACTERISTICS

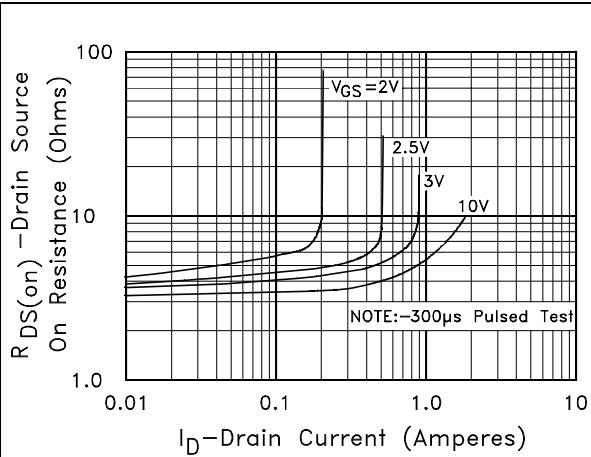


FIG. 3 Typical On Resistance vs. Drain Current

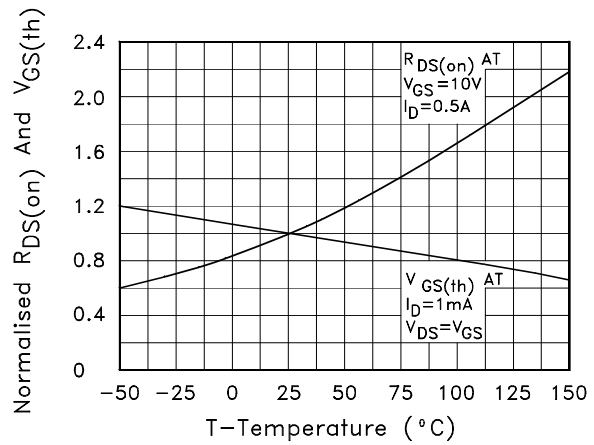


FIG. 4 Normalised $R_{DS(on)}$ And $V_{GS(th)}$ vs. Temperature

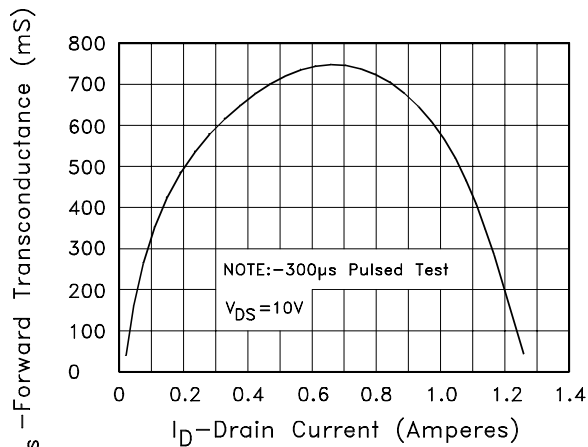


FIG. 5 Typical Transconductance vs. Drain Current

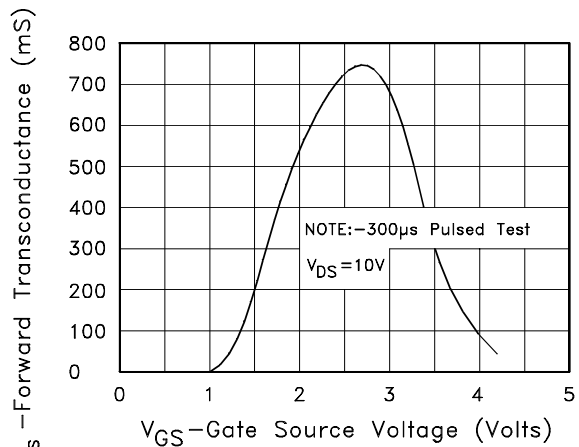


FIG. 6 Typical Transconductance vs. Gate-Source Voltage

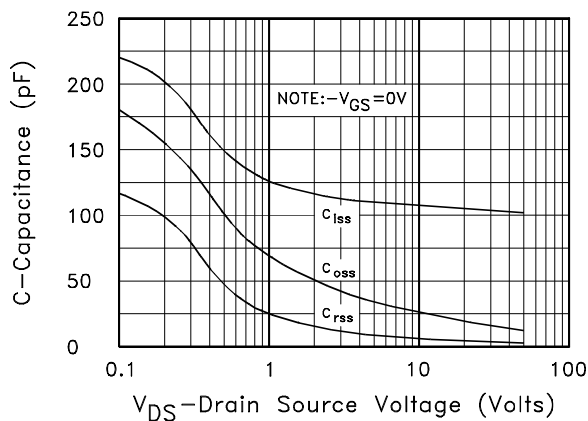


FIG. 7 Typical Capacitance vs. Drain-Source Voltage

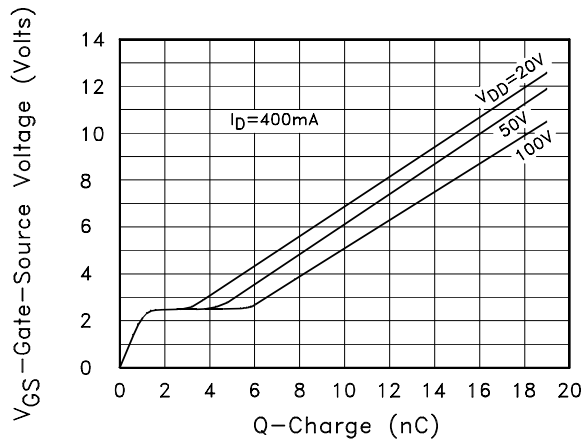


FIG. 8 Typical Gate Charge vs. Gate-Source Voltage

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ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated).

PARAMETER	SYMBOL	MIN.	TYP	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	240			V	$I_D=1\text{mA}, V_{GS}=0\text{V}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.8	1.3	1.8	V	$I_D=1\text{mA}, V_{DS}=V_{GS}$
Gate-Body Leakage	I_{GSS}			100	nA	$V_{GS}=\pm 40\text{V}, V_{DS}=0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}			10 100	μA μA	$V_{DS}=240\text{V}, V_{GS}=0$ $V_{DS}=190\text{V}, V_{GS}=0\text{V}, T=125^{\circ}\text{C}$
On-State Drain Current	$I_{D(on)}$	0.8	1.4		A	$V_{DS}=10\text{V}, V_{GS}=10\text{V}$
Static Drain-Source On-State Resistance	$R_{DS(on)}$		4 4.3	5.5 6	Ω Ω	$V_{GS}=10\text{V}, I_D=500\text{mA}$ $V_{GS}=2.5\text{V}, I_D=100\text{mA}$
Forward Transconductance (1) (2)	g_{fs}	0.4	0.75		S	$V_{DS}=10\text{V}, I_D=0.5\text{A}$
Input Capacitance (2)	C_{iss}		110	200	pF	$V_{DS}=25\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$
Common Source Output Capacitance (2)	C_{oss}		15	25	pF	
Reverse Transfer Capacitance (2)	C_{rss}		3.5	15	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		2.5	5	ns	$V_{DD}\approx 50\text{V}, I_D=0.25\text{A}, V_{GEN}=10\text{V}$
Rise Time (2)(3)	t_r		5	8	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		40	60	ns	
Fall Time (2)(3)	t_f		16	25	ns	

- (1)*Measured under pulsed conditions. Pulse width=300 μs . Duty cycle $\leq 2\%$ (2)Sample Test
 (3) Switching times measured with 50 Ω source impedance and >5ns rise time on pulse generator

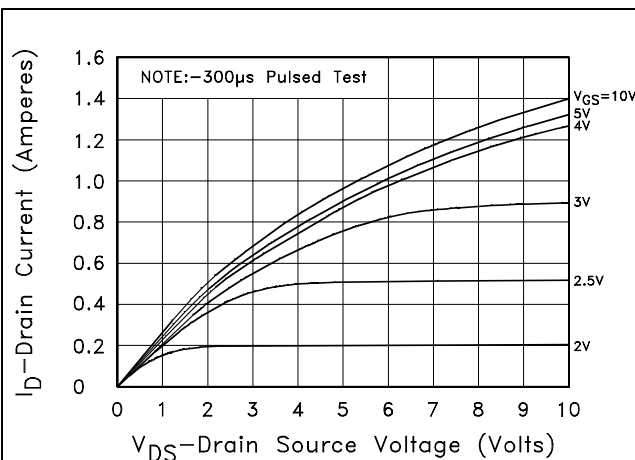


FIG. 1 Typical Saturation Characteristics

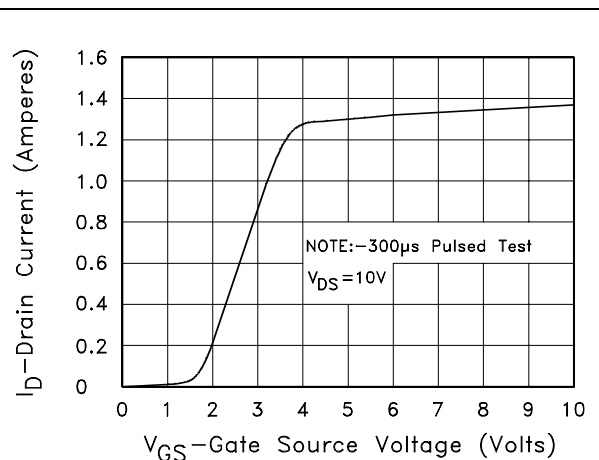
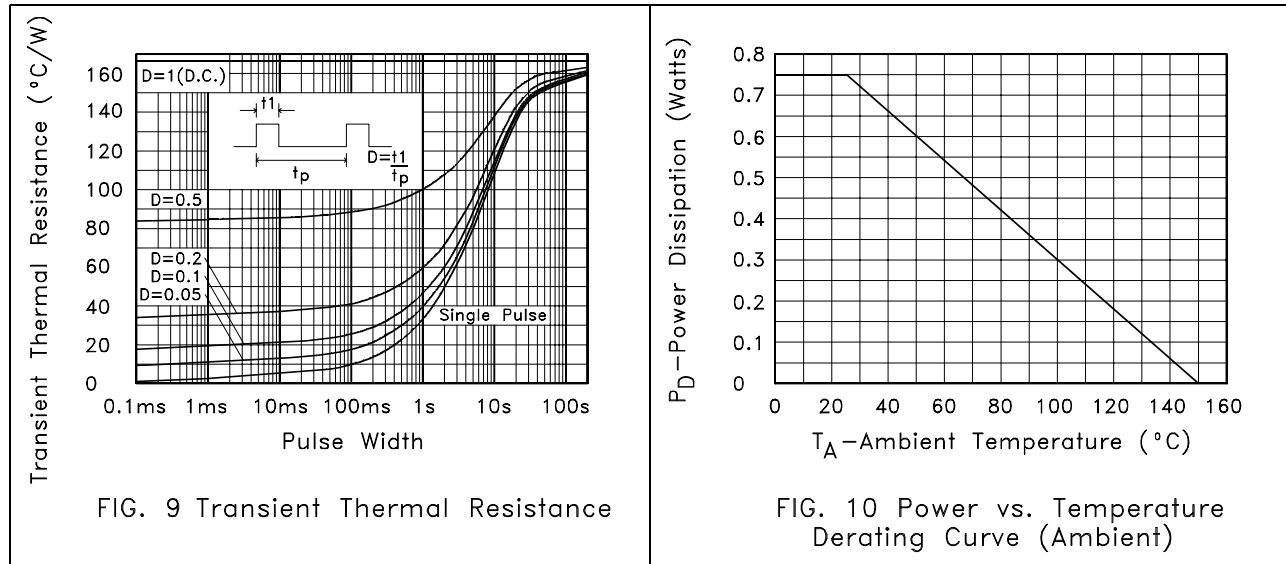


FIG. 2 Typical Transfer Characteristics

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SPICE PARAMETERS

*ZVN4424 MODEL LAST REVISION 1/94

*

.SUBCKT ZVN4424 30 40 50

* NODES: DRAIN GATE SOURCE

M1 30 20 50 50 MOD1 L=1 W=1

RG 40 20 200

RL 30 50 240E6

D1 50 30 DIODE1

.MODEL MOD1 NMOS VT0=1.25 RS=2.34 RD=1.634 IS=1E-15 KP=5.319

+CGS0=101P CGD0=4P CBD=66.2P PB=1

.MODEL DIODE1 D IS=5.516E-13 RS=0.2084 N=1.0078

.ENDS ZVN4424

For clarification of the above or for technical enquires generally please contact the Applications Dept. at Zetex plc.

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