

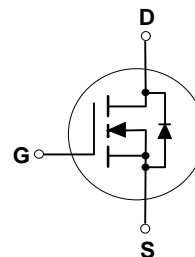
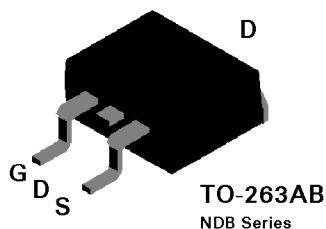
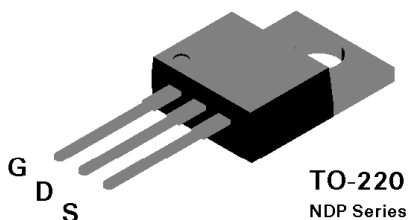
## NDP6060L / NDB6060L N-Channel Logic Level Enhancement Mode Field Effect Transistor

### General Description

These logic level N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

### Features

- 48A, 60V.  $R_{DS(ON)} = 0.025\Omega @ V_{GS} = 5V$ .
- Low drive requirements allowing operation directly from logic drivers.  $V_{GS(TH)} < 2.0V$ .
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low  $R_{DS(ON)}$ .
- TO-220 and TO-263 (D<sup>2</sup>PAK) package for both through hole and surface mount applications.



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDP6060L	NDB6060L	Units
$V_{DSS}$	Drain-Source Voltage	60		V
$V_{DGR}$	Drain-Gate Voltage ( $R_{GS} \leq 1\text{ M}\Omega$ )	60		V
$V_{GSS}$	Gate-Source Voltage - Continuous	$\pm 16$		V
	- Nonrepetitive ( $t_p < 50\ \mu\text{s}$ )	$\pm 25$		
$I_D$	Drain Current - Continuous	48		A
	- Pulsed	144		
$P_D$	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	100		W
	Derate above $25^\circ\text{C}$	0.67		W/°C
$T_J, T_{STG}$	Operating and Storage Temperature	-65 to 175		°C
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

**Electrical Characteristics** ( $T_c = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRAIN-SOURCE AVALANCHE RATINGS</b> (Note 1)						
$W_{DSS}$	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 25\text{ V}$ , $I_D = 48\text{ A}$			200	mJ
$I_{AR}$	Maximum Drain-Source Avalanche Current				48	A
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	60			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}$ , $V_{GS} = 0\text{ V}$			250	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		1	mA
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 16\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -16\text{ V}$ , $V_{DS} = 0\text{ V}$			-100	nA
<b>ON CHARACTERISTICS</b> (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1		2	V
			$T_J = 125^\circ\text{C}$	0.65	1.5	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 5\text{ V}$ , $I_D = 24\text{ A}$			0.025	$\Omega$
			$T_J = 125^\circ\text{C}$		0.04	
			$V_{GS} = 10\text{ V}$ , $I_D = 24\text{ A}$		0.02	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 5\text{ V}$ , $V_{DS} = 10\text{ V}$	48			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 24\text{ A}$	10			S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		1630	2000	pF
$C_{oss}$	Output Capacitance			460	800	pF
$C_{rss}$	Reverse Transfer Capacitance			150	400	pF
<b>SWITCHING CHARACTERISTICS</b> (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 30\text{ V}$ , $I_D = 48\text{ A}$ , $V_{GS} = 5\text{ V}$ , $R_{GEN} = 15\text{ }\Omega$ , $R_{GS} = 15\text{ }\Omega$		15	30	nS
$t_r$	Turn - On Rise Time			320	500	nS
$t_{D(off)}$	Turn - Off Delay Time			49	100	nS
$t_f$	Turn - Off Fall Time			161	300	nS
$Q_g$	Total Gate Charge	$V_{DS} = 48\text{ V}$ , $I_D = 48\text{ A}$ , $V_{GS} = 5\text{ V}$		36	60	nC
$Q_{gs}$	Gate-Source Charge			8.2		nC
$Q_{gd}$	Gate-Drain Charge			21		nC

**Electrical Characteristics** ( $T_c = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				48	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current				144	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 24\text{ A}$ (Note 1)			1.3	V
					$T_J = 125^\circ\text{C}$	
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_F = 48\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$	35	75	140	ns
$I_{rr}$	Reverse Recovery Current		2	3.6	8	A
<b>THERMAL CHARACTERISTICS</b>						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				1.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	$^\circ\text{C}/\text{W}$

Note:

 1. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Typical Electrical Characteristics

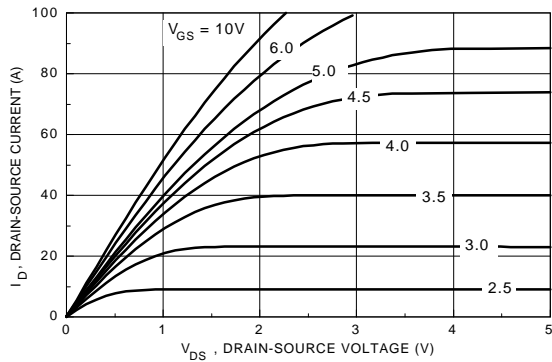


Figure 1. On-Region Characteristics.

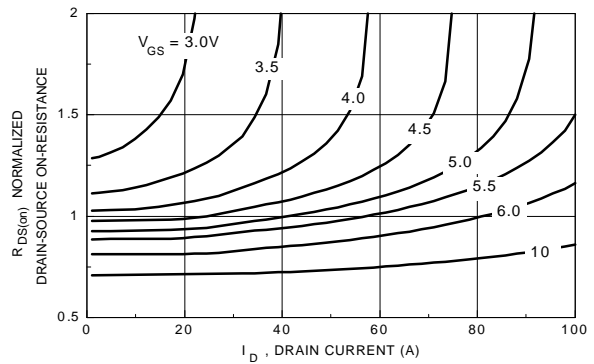


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

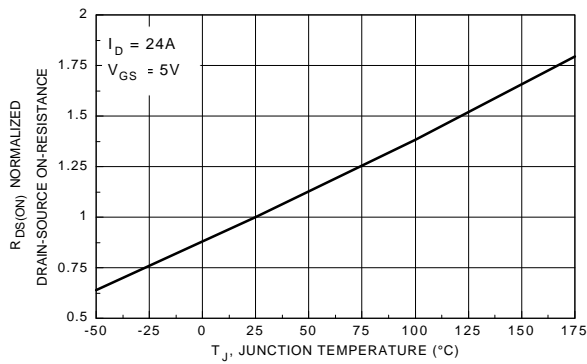


Figure 3. On-Resistance Variation with Temperature.

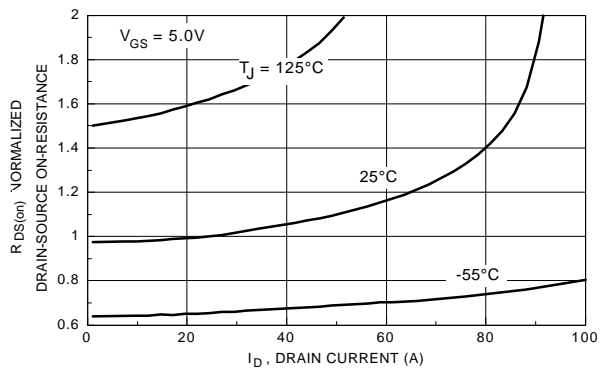


Figure 4. On-Resistance Variation with Drain Current and Temperature.

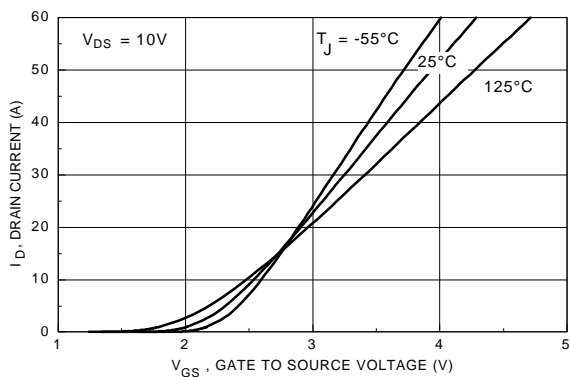


Figure 5. Transfer Characteristics.

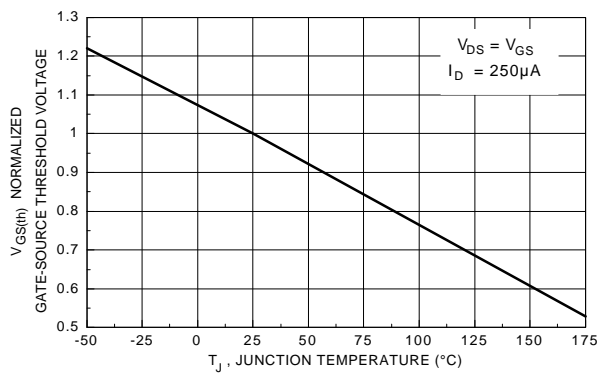
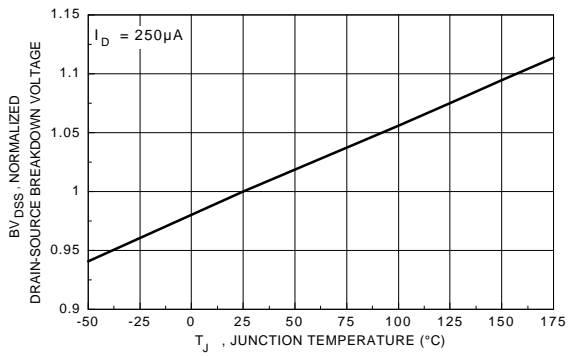
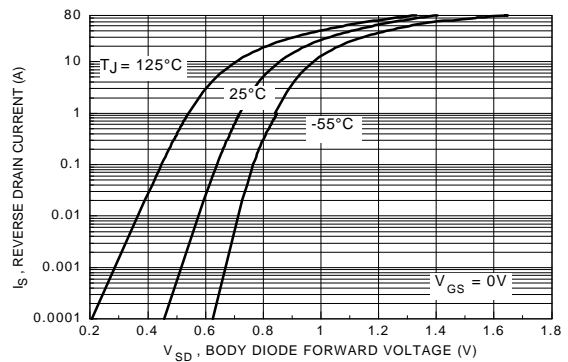


Figure 6. Gate Threshold Variation with Temperature.

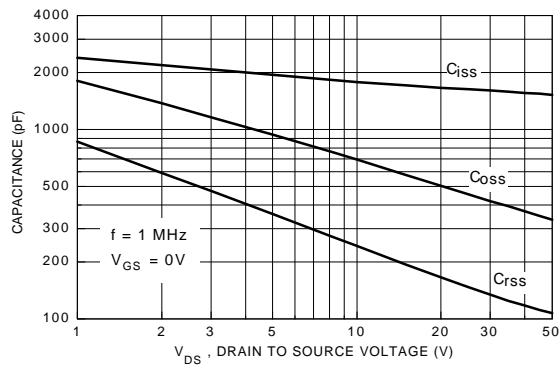
## Typical Electrical Characteristics (continued)



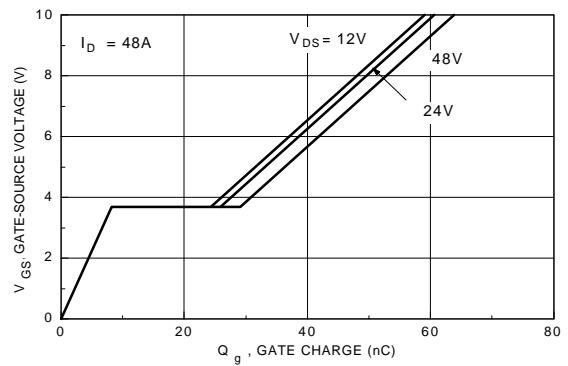
**Figure 7. Breakdown Voltage Variation with Temperature.**



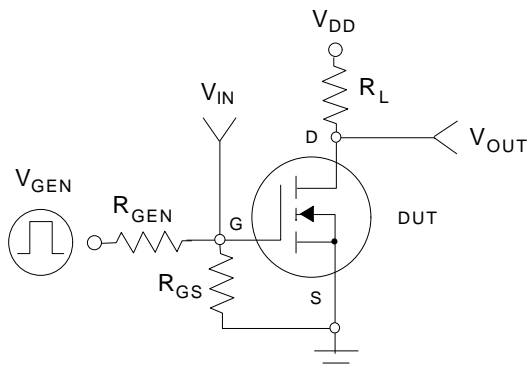
**Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.**



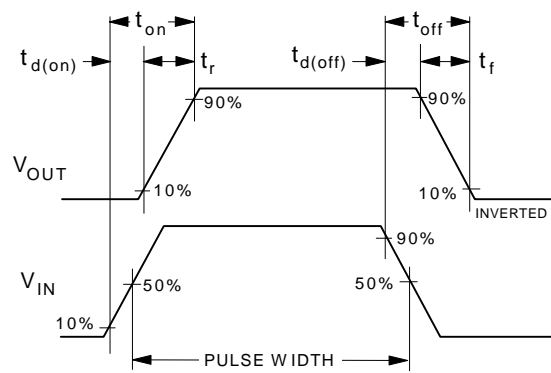
**Figure 9. Capacitance Characteristics.**



**Figure 10. Gate Charge Characteristics.**



**Figure 11. Switching Test Circuit.**



**Figure 12. Switching Waveforms.**

### Typical Electrical Characteristics (continued)

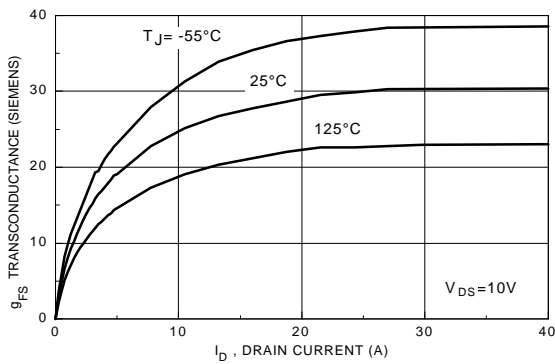


Figure 13. Transconductance Variation with Drain Current and Temperature

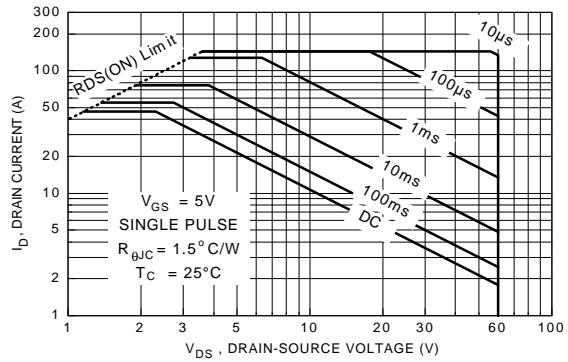


Figure 14. Maximum Safe Operating Area

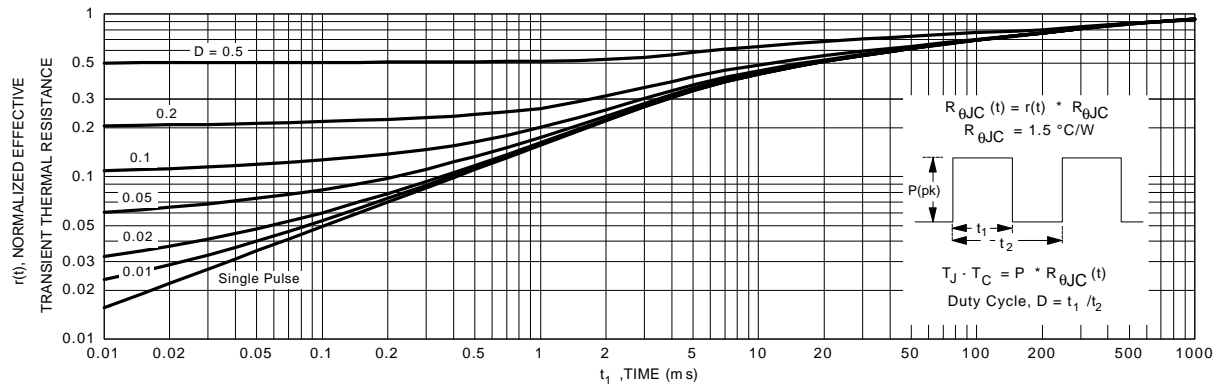
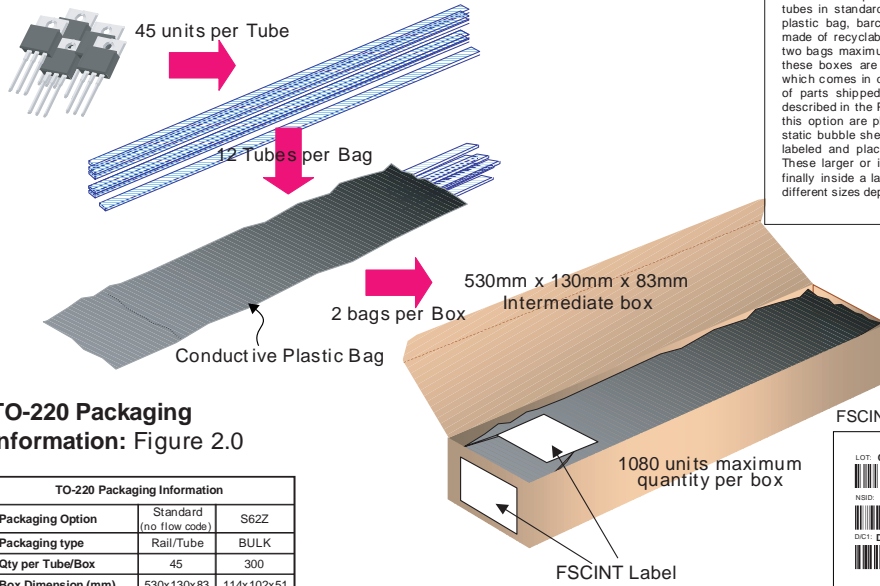


Figure 15. Transient Thermal Response Curve.

# TO-220 Tape and Reel Data and Package Dimensions



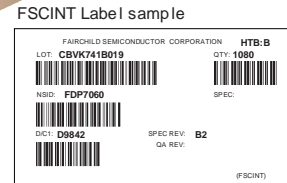
## TO-220 Tube Packing Configuration: Figure 1.0



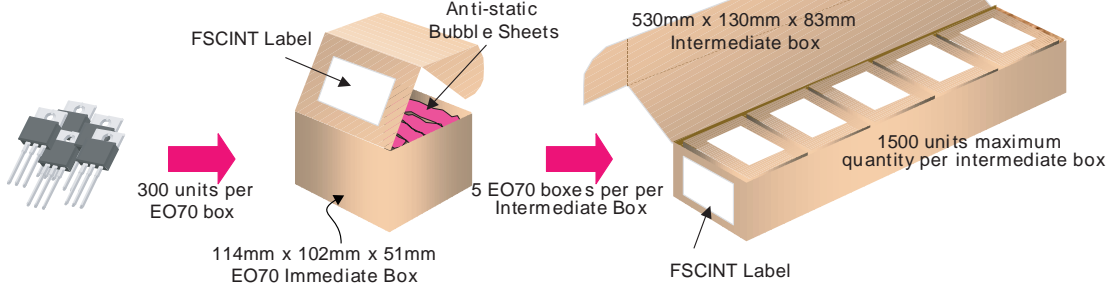
**Packaging Description:**  
 TO-220 parts are shipped normally in tube. The tube is made of PVC plastic treated with anti-static agent. These tubes in standard option are placed inside a dissipative plastic bag, barcode labeled, and placed inside a box made of recyclable corrugated paper. One box contains two bags maximum (see fig. 1.0). And one or several of these boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped. The other option comes in bulk as described in the Packaging Information table. The units in this option are placed inside a small box laid with anti-static bubble sheet. These smaller boxes are individually labeled and placed inside a larger box. (See fig. 3.0). These larger or intermediate boxes then will be placed finally inside a labeled shipping box which still comes in different sizes depending on the number of units shipped.

## TO-220 Packaging Information: Figure 2.0

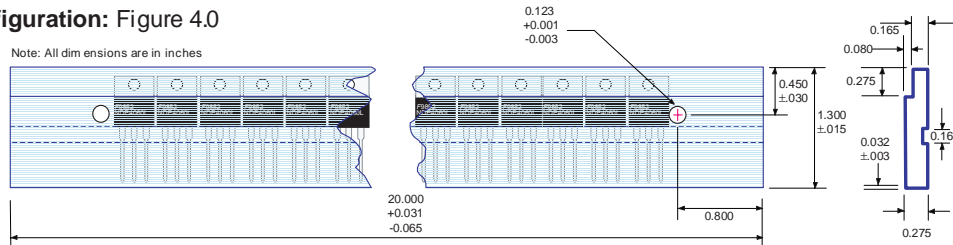
TO-220 Packaging Information		
Packaging Option	Standard (no flow code)	S62Z
Packaging type	Reel/Tube	BULK
Qty per Tube/Box	45	300
Box Dimension (mm)	530x130x83	114x102x51
Max qty per Box	1,080	1,500
Weight per unit (gm)	1.4378	1.4378
Note/Comments		



## TO-220 bulk Packing Configuration: Figure 3.0

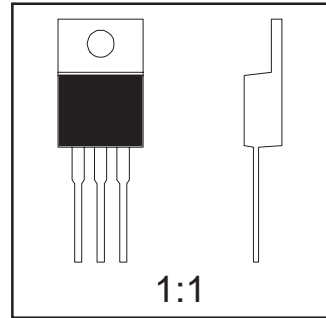
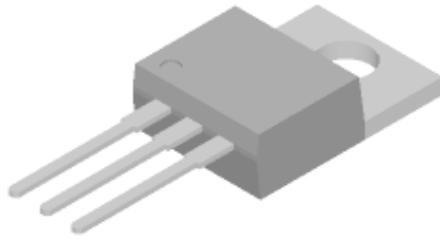


## TO-220 Tube Configuration: Figure 4.0



**TO-220 Tape and Reel Data and Package Dimensions, continued**

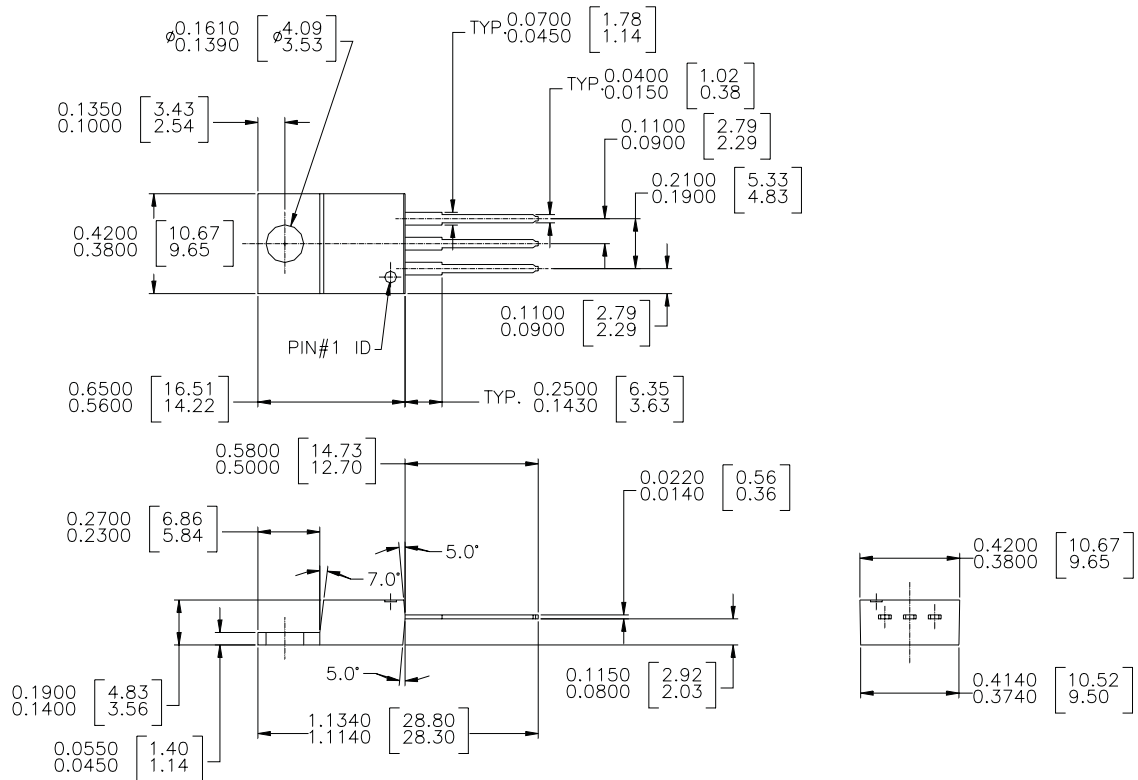
**TO-220 (FS PKG Code 37)**



Scale 1:1 on letter size paper

Dimensions shown below are in:  
inches [millimeters]

Part Weight per unit (gram): 1.4378



NOTE : UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH :  
200 MICROINCHES / 5.08 MICRON MINIMUM  
LEAD / TIN 15/85 ON OLIN 194 COPPER OR EQUIVALENT

2. DIMENSION BASED ON JEDEC STANDARD TO-220  
VARIATION AB, ISSUE J, DATED 3/24/87

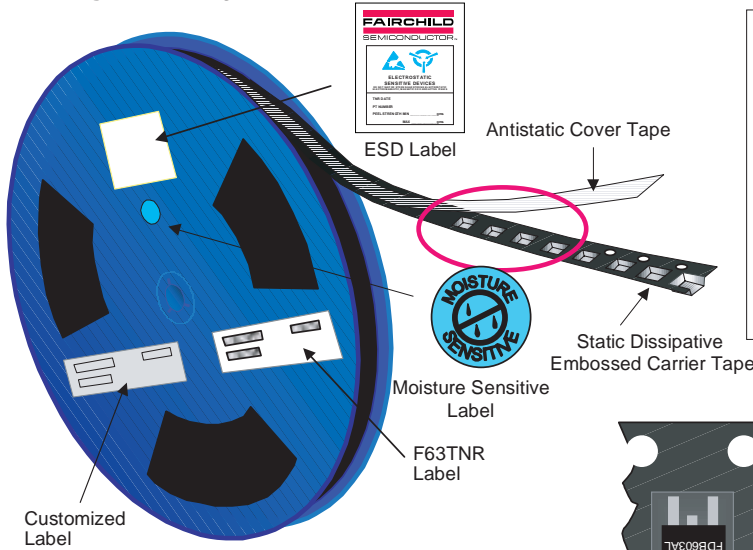
TO 220 3 LEAD



# TO-263AB/D<sup>2</sup>PAK Tape and Reel Data and Package Dimensions



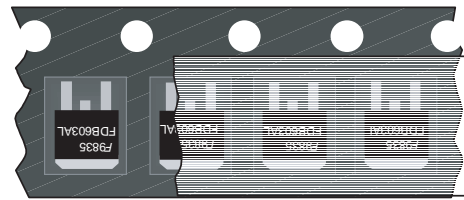
## TO-263AB/D<sup>2</sup>PAK Packaging Configuration: Figure 1.0



### Packaging Description:

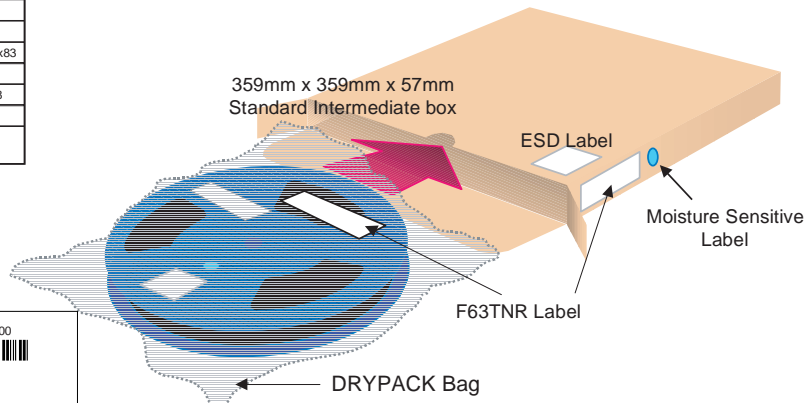
TO-263/D<sup>2</sup>PAK parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 800 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). This and some other options are further described in the Packaging Information table.

These full reels are individually barcode labeled, dry packed, and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains one reel maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.



TO-263AB/D<sup>2</sup>PAK Unit Orientation

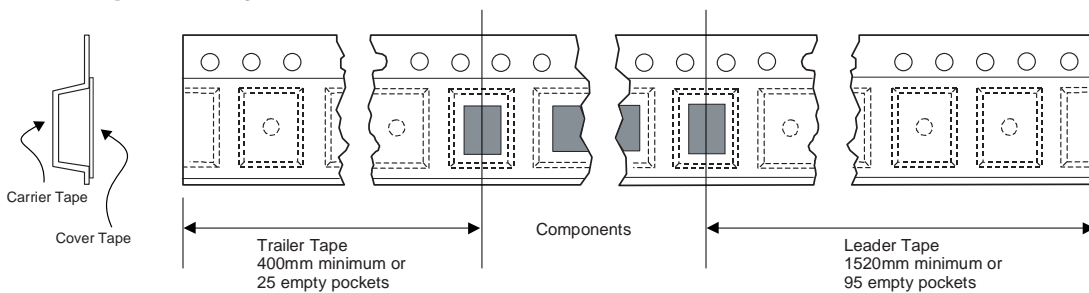
TO-263AB/D <sup>2</sup> PAK Packaging Information		
Packaging Option	Standard (no flow code)	L86Z
Packaging type	TNR	Rail/Tube
Qty per Reel/Tube/Bag	800	45
Reel Size	13" Dia	-
Box Dimension (mm)	359x359x57	530x130x83
Max qty per Box	800	1,080
Weight per unit (gm)	1.4378	1.4378
Weight per Reel	1.6050	-
Note/Comments		



### F63TNR Label sample



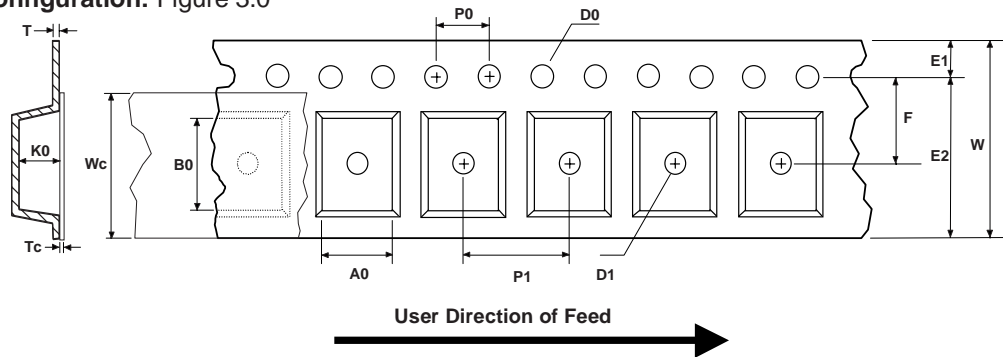
## TO-263AB/D<sup>2</sup>PAK Tape Leader and Trailer Configuration: Figure 2.0



# TO-263AB/D<sup>2</sup>PAK Tape and Reel Data and Package Dimensions, continued

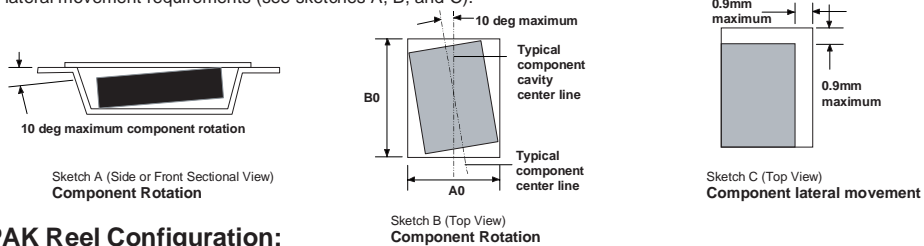
## TO-263AB/D<sup>2</sup>PAK Embossed Carrier Tape

Configuration: Figure 3.0

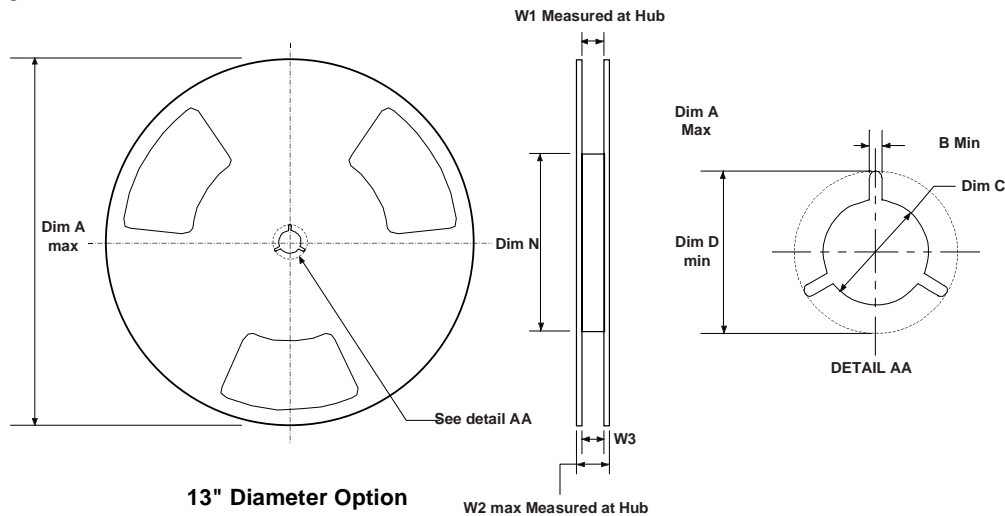


Dimensions are in millimeter														
Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
TO263AB/ D <sup>2</sup> PAK (24mm)	10.60 +/-0.10	15.80 +/-0.10	24.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	22.25 min	11.50 +/-0.10	16.0 +/-0.1	4.0 +/-0.1	4.90 +/-0.10	0.450 +/-0.150	21.0 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



## TO-263AB/D<sup>2</sup>PAK Reel Configuration: Figure 4.0

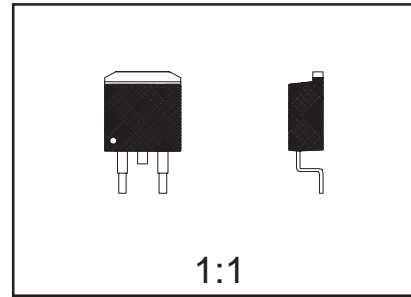
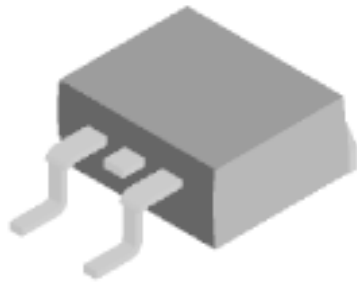


Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
24mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.961 +0.078/-0.000 24.4 +2/0	1.197 30.4	0.941 - 0.1.079 23.9 - 27.4

August 1999, Rev. B

TO-263AB/D<sup>2</sup>PAK Tape and Reel Data and Package Dimensions, continued

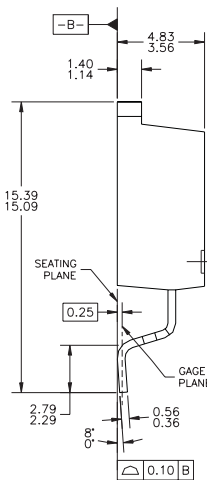
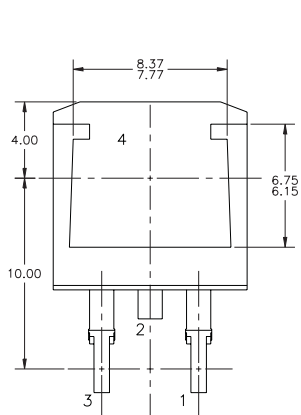
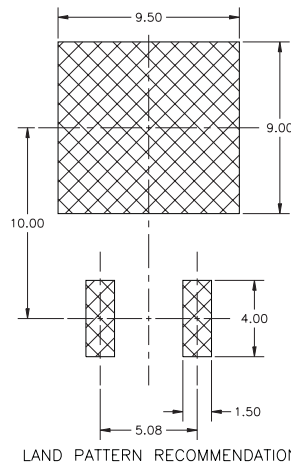
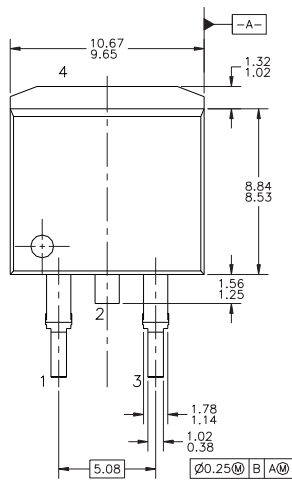
TO-263AB/D<sup>2</sup>PAK (FS PKG Code 45)



Scale 1:1 on letter size paper

Dimensions shown below are in:  
inches [millimeters]

Part Weight per unit (gram): 1.4378



- NOTES: UNLESS OTHERWISE SPECIFIED  
 A) ALL DIMENSIONS ARE IN MILLIMETERS.  
 B) STANDARD LEAD FINISH:  
 200 MICROINCHES / 5.08 MICROMETERS MIN.  
 LEAD/TIN 15/85 ON OLIN 194 COPPER OR  
 EQUIVALENT.  
 C) MAXIMUM VERTICAL BURR ON HEATSINK NOT  
 TO EXCEED 0.003 INCH / 0.05mm.  
 D) NO PACKAGE CHIPS, CRACKS OR SURFACE  
 IDENTIFICATION ALLOWED AFTER FORMING.  
 E) REFERENCE JEDEC, TO-263, ISSUE C,  
 VARIATION AB, DATED 2/92.

August 1998, Rev. A

## TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	ISOPLANAR™	SyncFET™
CoolFET™	MICROWIRE™	TinyLogic™
CROSSVOLT™	POP™	UHC™
E <sup>2</sup> CMOS™	PowerTrench®	VCX™
FACT™	QFET™	
FACT Quiet Series™	QS™	
FAST®	Quiet Series™	
FASTr™	SuperSOT™-3	
GTO™	SuperSOT™-6	
HiSeC™	SuperSOT™-8	

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.