FAIRCHILD
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FDC697P

P-Channel 1.8V PowerTrench® MOSFET

General Description

This P-Channel 1.8V specified MOSFET uses Fairchild's advanced low voltage Power Trench process. It has been optimized for battery power management applications.

Applications

- Battery management
- Load Switch
- Battery protection

Features

- −8 A, −20 V $R_{DS(ON)}$ = 20 mΩ @ V_{GS} = −4.5 V
  $R_{DS(ON)}$ = 25 mΩ @ V_{GS} = −2.5 V
  $R_{DS(ON)}$ = 35 mΩ @ V_{GS} = −1.8 V

- High performance trench technology for extremely low $R_{DS(ON)}$

- Fast switching speed

- FLMP SuperSOT-6 package: Enhanced thermal performance in industry-standard package size

SuperSOT-6™ FLMP
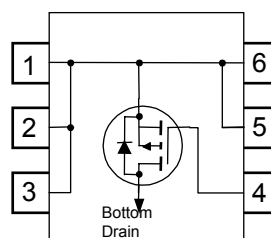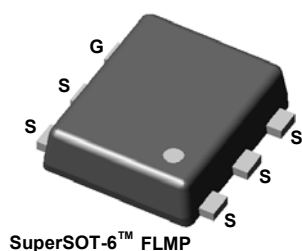
Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		−20	V
V_{GSS}	Gate-Source Voltage		±8	V
I_D	Drain Current – Continuous	(Note 1a)	−8	A
	– Pulsed		−40	
P_D	Power Dissipation	(Note 1a)	2	W
		(Note 1b)	1.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	60	°C/W
		(Note 1b)	111	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		0.5	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.697	FDC697P	7''	8mm	3000 units

Electrical Characteristics

$T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = -250$ µA	–20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250$ µA, Referenced to 25°C		–12.2		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16$ V, $V_{GS} = 0$ V			–1	µA
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm8$ V, $V_{DS} = 0$ V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -250$ µA	–0.4	–0.8	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250$ µA, Referenced to 25°C		2.9		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -4.5$ V, $I_D = -8$ A		13	20	mΩ
		$V_{GS} = -2.5$ V, $I_D = -6.8$ A		18	25	
		$V_{GS} = -1.8$ V, $I_D = -5.8$ A		26	35	
		$V_{GS} = -4.5$ V, $I_D = -8$ A, $T_J = 125°C$		16	27	
g_{FS}	Forward Transconductance	$V_{DS} = -5$ V, $I_D = -8$ A		37		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -10$ V, $V_{GS} = 0$ V, f = 1.0 MHz		3524		pF
C_{oss}	Output Capacitance			544		pF
C_{rss}	Reverse Transfer Capacitance			254		pF
R_G	Gate Resistance	$V_{GS} = 15$ mV, f = 1.0 MHz		3.8		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -10$ V, $I_D = -1$ A, $V_{GS} = -4.5$ V, $R_{GEN} = 6$ Ω		18	32	ns
t_r	Turn–On Rise Time			6	12	ns
$t_{d(off)}$	Turn–Off Delay Time			119	190	ns
t_f	Turn–Off Fall Time			43	69	ns
Q_g	Total Gate Charge	$V_{DS} = -10$ V, $I_D = -8$ A, $V_{GS} = -4.5$ V		39	55	nC
Q_{gs}	Gate–Source Charge			6	8.4	nC
Q_{gd}	Gate–Drain Charge			5.6	7.8	nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–1.6	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = -1.6$ A (Note 2)		–0.7	–1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -8$ A, $d_{iF}/d_t = 100$ A/µs		27		ns
Q_{rr}	Reverse Recovery Charge			16		nC

Notes: 1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

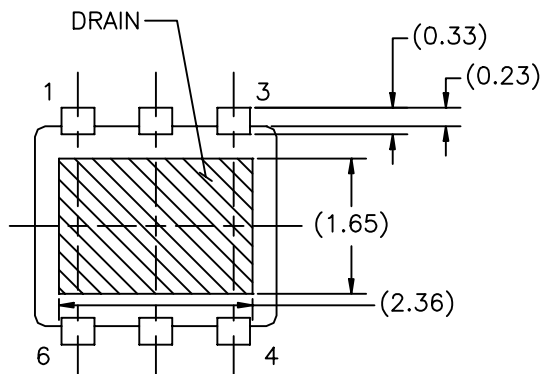a) 60°C/W when mounted on a 1in^2 pad of 2 oz copper

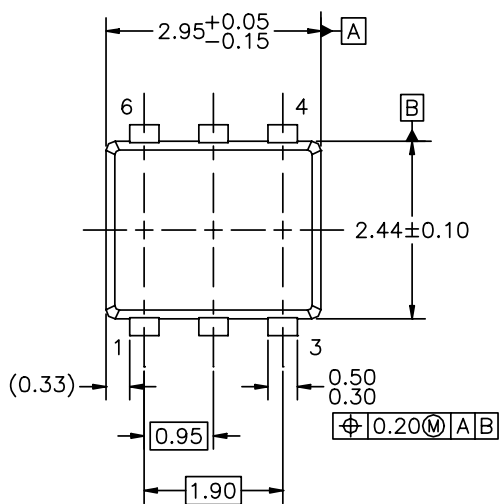b) 111°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

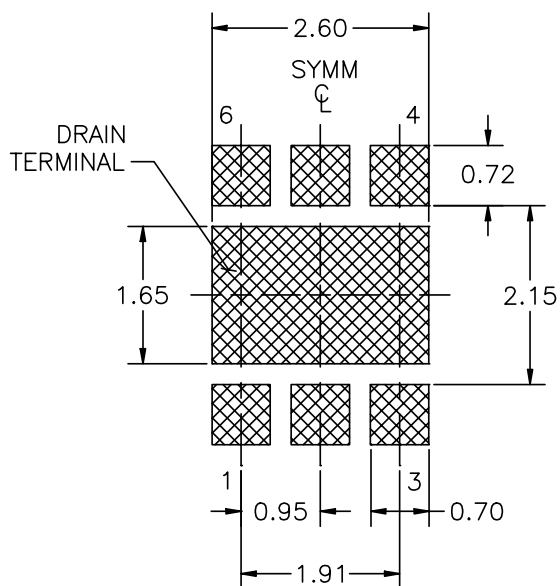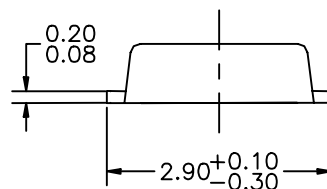**2.** Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Dimensional Outline and Pad Layout

DRAIN

1   3

(0.33)
(0.23)

(1.65)

(2.36)

6   4

Bottom View

0.85
0.65

SEATING
PLANE

0.20
0.08

$2.90^{+0.10}_{-0.30}$

$2.95^{+0.05}_{-0.15}$ A

6   4   B

2.44±0.10

1   3

(0.33)

0.50
0.30

0.95

⊕ 0.20Ⓜ A B

1.90

Top View

2.60

SYMM
C̶L

DRAIN
TERMINAL

6   4

0.72

1.65

2.15

1   3

0.95   0.70

1.91
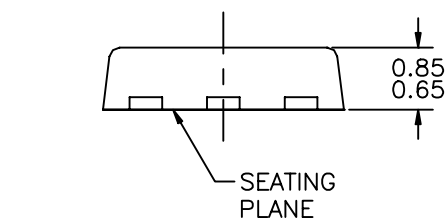
Recommended Landing Pattern

FDC697P Rev C2 (W)

Typical Characteristics
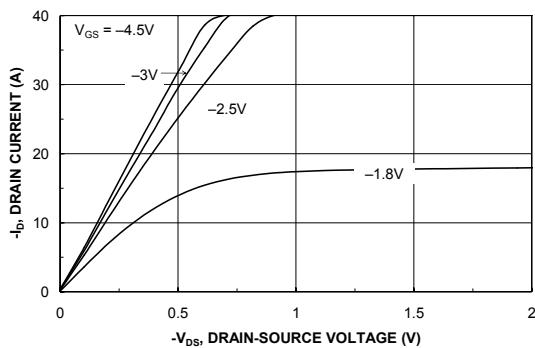
Figure 1. On-Region Characteristics.
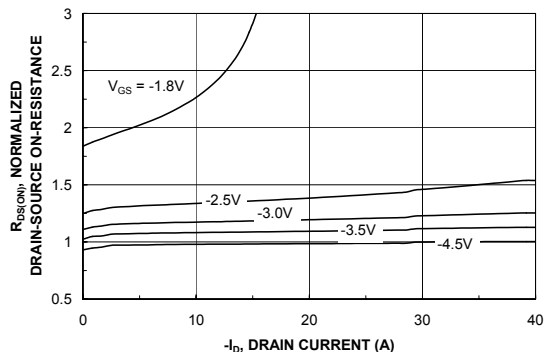
Figure 2. On-Resistance Variation with
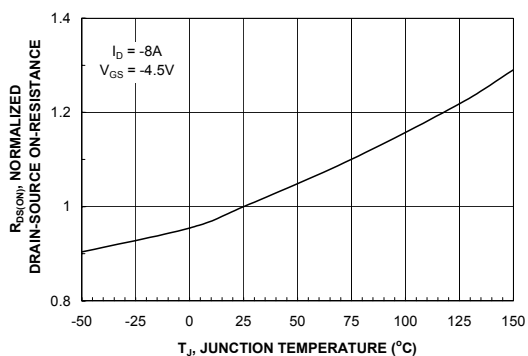Drain Current and Gate Voltage.

Figure 3. On-Resistance Variation
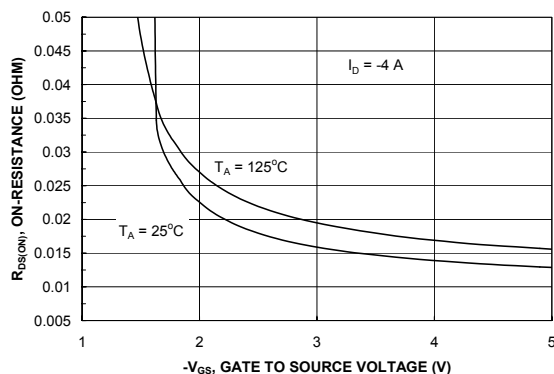withTemperature.

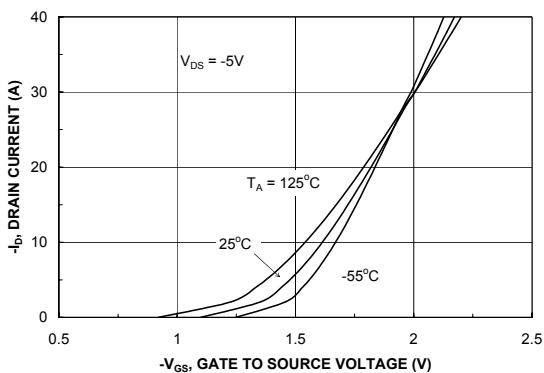Figure 4. On-Resistance Variation with
Gate-to-Source Voltage.

Figure 5. Transfer Characteristics.
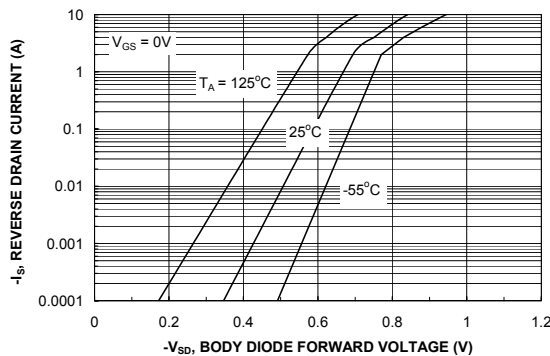

Figure 6. Body Diode Forward Voltage Variation
with Source Current and Temperature.

FDC697P Rev C2 (W)
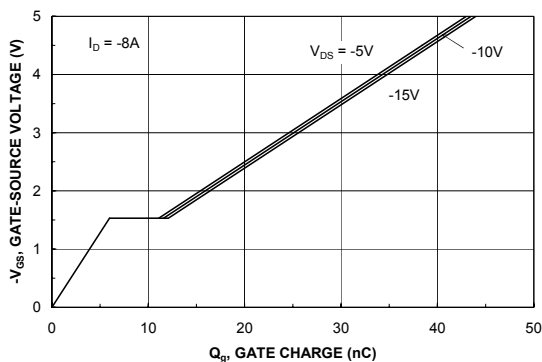
Typical Characteristics
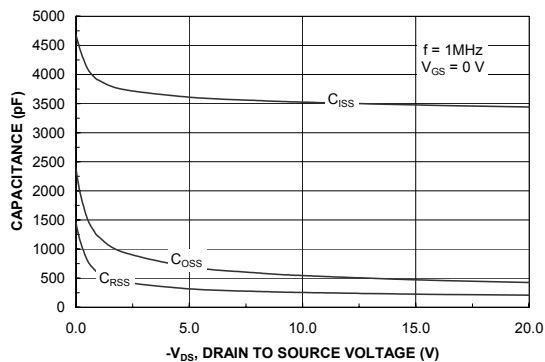

Figure 7. Gate Charge Characteristics.

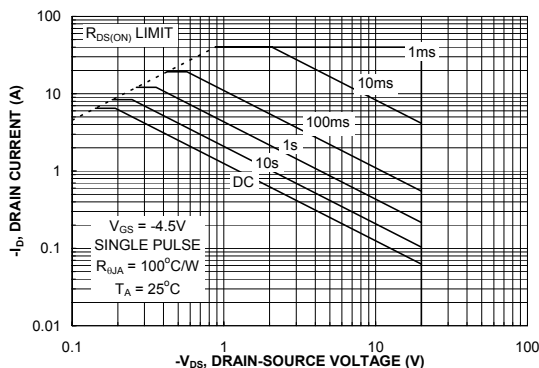Figure 8. Capacitance Characteristics.
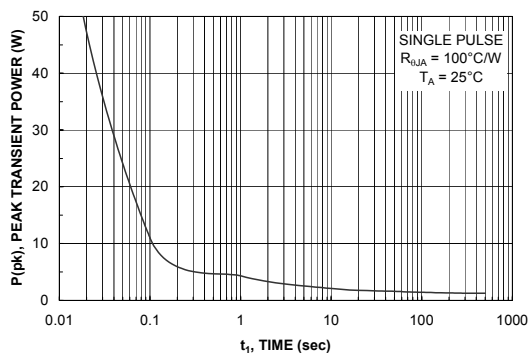

Figure 9. Maximum Safe Operating Area.

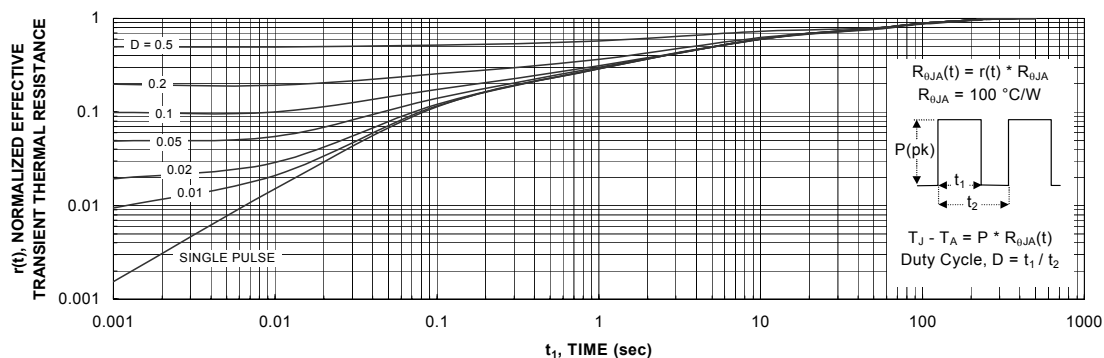Figure 10. Single Pulse Maximum
Power Dissipation.

Figure 11. Transient Thermal Response Curve.

**Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.**

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