# FDB8453LZ N-Channel PowerTrench<sup>®</sup> MOSFET 40V, 50A, 7.0mΩ

#### Features

- Max  $r_{DS(on)} = 7.0 m\Omega$  at  $V_{GS} = 10V$ ,  $I_D = 17.6A$
- Max  $r_{DS(on)} = 9.0 \text{m}\Omega$  at  $V_{GS} = 4.5 \text{V}$ ,  $I_D = 14.9 \text{A}$
- HBM ESD protection level of 7.6kV typical (note 4)
- Fast Switching
- RoHS Compliant

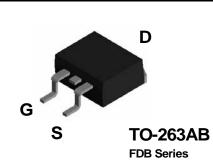


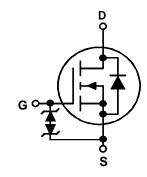
## **General Description**

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that has been especially tailored to minimize the on-state resistance and switching loss. G-S zener has been added to enhance ESD voltage level.

### Applications

- Inverter
- Power Supplies





## **MOSFET Maximum Ratings** $T_{C} = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter			Ratings	Units	
V <sub>DS</sub>	Drain to Source Voltage			40	V	
V <sub>GS</sub>	Gate to Source Voltage			±20	V	
ID	Drain Current -Continuous (Package limited)	$T_{C} = 25^{\circ}C$		50		
	-Continuous (Silicon limited)	T <sub>C</sub> = 25°C		74	^	
	-Continuous	$T_A = 25^{\circ}C$	(Note 1a)	16.1	A	
	-Pulsed			100		
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	253	mJ	
P <sub>D</sub>	Power Dissipation	$T_{C} = 25^{\circ}C$		66	14/	
	Power Dissipation $T_A = 25^{\circ}C$ (Note 1a)		(Note 1a)	3.1	W	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range			-55 to +150	°C	

## **Thermal Characteristics**

$R_{ ext{ heta}JC}$	Thermal Resistance, Junction to Case		1.88	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	40	C/vv

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB8453LZ	FDB8453LZ	TO-263AB	330mm	24mm	800 units

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Symbol	Parameter	Test Conditions	Min	Тур	Max	Units	
Off Chara	cteristics						
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_{D} = 250 \mu A, V_{GS} = 0 V$	40			V	
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu A$ , referenced to 25°C		36		mV/°0	
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 32V, V_{GS} = 0V$			1	μA	
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$			±10	μA	
On Chara	cteristics						
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250μA	1.0	1.8	3.0	V	
$\frac{\Delta V_{GS(th)}}{\Delta T_{J}}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu A$ , referenced to 25°C		-6.0		mV/°0	
j		V <sub>GS</sub> = 10V, I <sub>D</sub> = 17.6A		6.3	7.0		
-	Citatia Desia da Cauras On Desistanos	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 14.9A		7.3	9.0		
r <sub>DS(on)</sub> Static Drain to Source On Resistance	Static Drain to Source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 17.6A, T <sub>J</sub> = 125°C		9.9	11	- mΩ	
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5V, I <sub>D</sub> = 17.6A		84		S	
C <sub>iss</sub>	Characteristics Input Capacitance			2665	3545	pF	
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 20V, V_{GS} = 0V,$		325	430	pF	
C <sub>rss</sub>	Reverse Transfer Capacitance	f = 1MHz		200	295	pF	
R <sub>g</sub>	Gate Resistance	f = 1MHz		2.2		Ω	
	g Characteristics			1		1	
t <sub>d(on)</sub>	Turn-On Delay Time			11	20	ns	
t <sub>r</sub>	Rise Time	$V_{DD} = 20V, I_D = 17.6A,$ $V_{GS} = 10V, R_{GEN} = 6Ω$		6	13	ns	
t <sub>d(off)</sub>	Turn-Off Delay Time	*GS = 10*, 1\GEN = 0\2		37	60	ns	
t <sub>f</sub>	Fall Time			5	11	ns	
Qg	Total Gate Charge	$V_{GS} = 0V \text{ to } 10V$ $V_{GS} = 0V \text{ to } 5V$ $V_{DD} = 20V,$ $V_{DD} = 17.64$		47	66	nC	
Qg	Total Gate Charge	$V_{GS} = 0V \text{ to } 5V$ $V_{DD} = 20V,$ $I_{D} = 17.6A$		25	35	nC	
Q <sub>gs</sub>	Gate to Source Charge	- ID = 17.0A		7		nC	
Q <sub>gd</sub>	Gate to Drain "Miller" Charge			9		nC	
	was Diada Characteristica						
Drain-So	urce Diode Characteristics			07	4.0	I	
		$V_{GS} = 0V, I_S = 2.6A$ (Note 2)		0.7	1.2	17	
<b>Drain-So</b> V <sub>SD</sub>	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = 2.6A$ (Note 2) $V_{GS} = 0V, I_S = 17.6A$ (Note 2)		0.7	1.2	V	
						V ns	

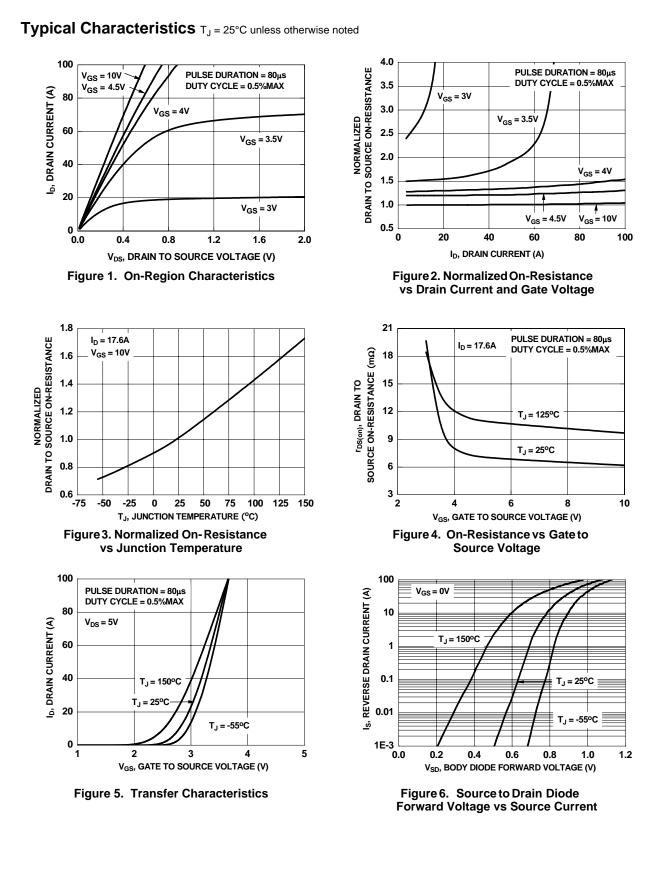
I R<sub>0,L</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>0,JC</sub> is guaranteed by design while R<sub>0,JA</sub> is determined by the user's board design.

a. 40°C/W when mounted on a 1  $\mbox{in}^2\,\mbox{pad}$  of 2 oz copper

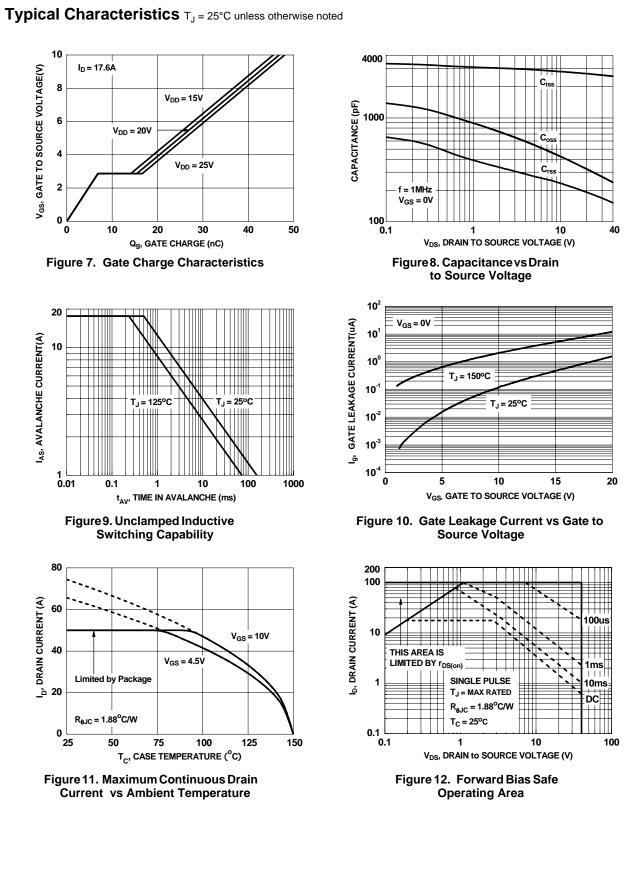
b. 62.5°C/W when mounted on a minimum pad.

Pulse Test: Pulse Width < 300µs, Duty cycle < 2.0%.</li>
 Starting T<sub>J</sub> = 25°C, L = 3mH, I<sub>AS</sub> = 13A, V<sub>DD</sub> = 40V, V<sub>GS</sub> = 10V.
 The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

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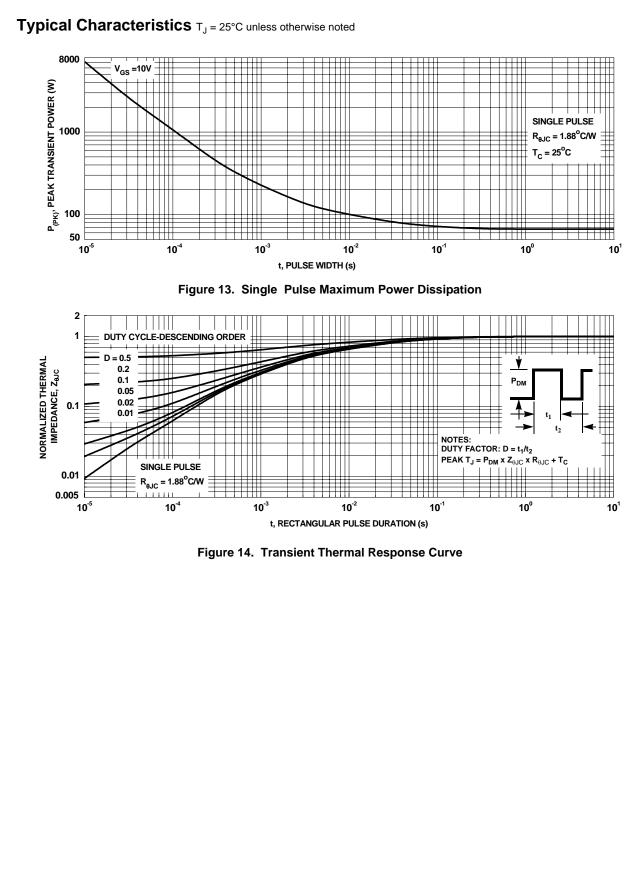
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