

Date Created : 2009/04/03
Date Issued On : 2009/04/14
PCN# : Q2091404

DESIGN/PROCESS CHANGE NOTIFICATION -- FINAL

This is to inform you that a design and/or process change will be made to the following product(s). This notification is for your information and concurrence.

If you require data or samples to qualify this change, please contact **Fairchild Semiconductor within 30 days of receipt of this notification.**

Updated process quality documentation, such as FMEAs and Control Plans, are available for viewing upon request.

If you have any questions concerning this change, please contact:

Technical Contact:

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Implementation of change:

Expected 1st Device Shipment Date: 2009/07/13

Earliest Year/Work Week of Changed Product: 0929

Change Type Description: Assembly Process, Lead Finish Composition, Package Change (Lead Frame), Package External Dimension

Description of Change (From): Selected MOSFET products assembled in Power 56 package, in which the current Die Attach Pad & Leadpost plating is NiPdAu; current Gate Leadpost Plating is NiPdAu; current Gate Interconnect is 5mil Al wire; current Singulation Method is Saw-Singulation and current Plating Finish is NiPdAu. To view "From/To" Dimensional Outline, please refer to the attached table "Dimensional Outline."

Description of Change (To): The alternate Die Attach Pad & Leadpost plating will be Bare Cu; alternate Gate Leadpost Plating will be Ag; alternate Gate Interconnect will be 2mil Cu wire; alternate Singulation Method will be Punch-singulation and the alternate Plating Finish will be Pure Sn.

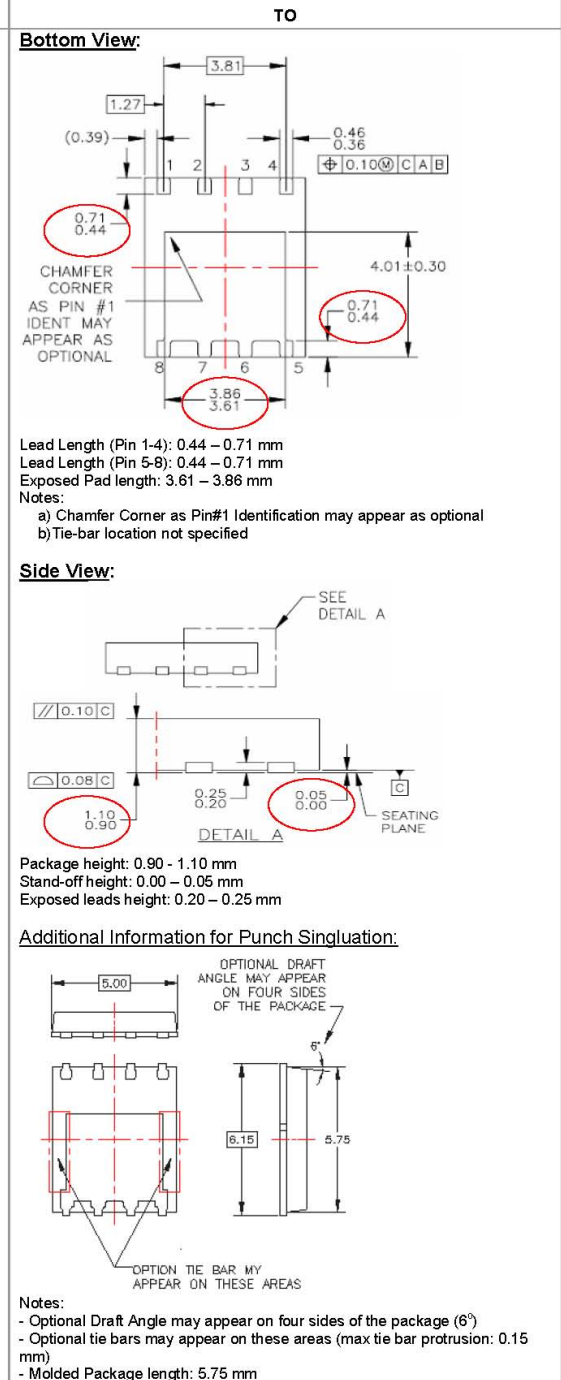
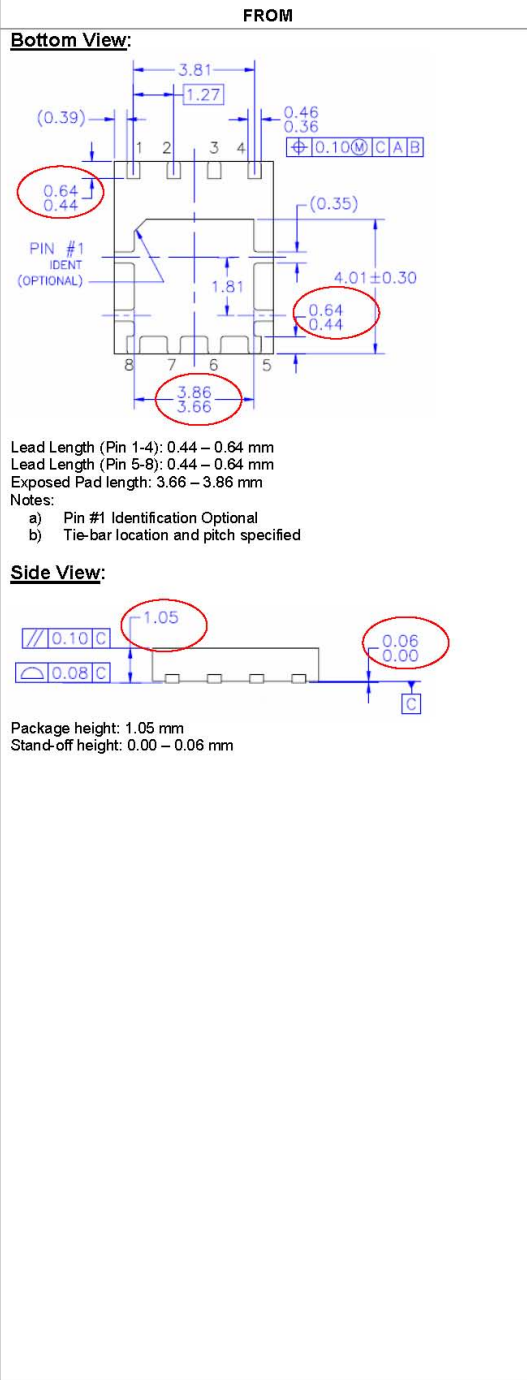
Reason for Change : In addition to the current qualified Saw-singulated Power 56 package, Fairchild Semiconductor intends to qualify the Punch-singulated Power 56 to support volume ramp. There will be no change to the part number as the Punch and Saw-singulated Power 56 share common land pattern dimensions and are interchangeable

Change From

Description of Change:	FROM:	TO:
1. Die Attach Pad & Source Leadpost plating	NiPdAu	Bare Cu
2. Gate Leadpost Plating	NiPdAu	Ag
3. Gate Interconnect	5mil Al wire	2mil Cu wire
4. Singulation Method	Saw Singulation	Punch Singulation
5. Plating Finish	NiPdAu	Pure Sn

Change To

Description of Change: 6. Dimensional Outline



Qual/REL Plan Numbers : Q20090181

Qualification :

This change will not affect the devices' specifications or functional performance. Product quality, reliability and MSL performance will be maintained. There will be no change to the part number as both the Punch and Saw-singulated Power 56 share common land pattern dimensions

and are interchangeable. The reliability qualification is complete and results are detailed in the attached table:

Results/Discussion for Qual Plan Number Q20090181

Test: (Board Level Temperature Cycle) Conditions: -10C, 100C Standard: IPC-9701					
Lot	Device	100-HOURS	500-HOURS	1000	Failure Code
Q20090181AABTMCL	FDMS8692	0/77			
			0/77		
				0/77	
Q20090181BABTMCL	FDMS8672AS	0/77			
			0/77		
				0/77	
Q20090181CABTMCL	FDMS8670AS	0/77			
			0/77		
				0/77	
Test: (High Temperature Reverse Bias) Conditions: 125C, 24V Standard: JESD22-A108					
Lot	Device	168-HOURS	500-HOURS	Failure Code	
Q20090181BAHTRB	FDMS8672AS	0/77			
Q20090181BAHTRB	FDMS8672AS		0/77		
Q20090181CAHTRB	FDMS8670AS	0/77			
Q20090181CAHTRB	FDMS8670AS		0/77		
Test: (High Temperature Reverse Bias) Conditions: 175C, 24V Standard: JESD22-A108					
Lot	Device	168-HOURS	500-HOURS	Failure Code	
Q20090181AAHTRB	FDMS8692	0/77			
Q20090181AAHTRB	FDMS8692		0/77		
Test: (High Temperature Storage Life) Conditions: 175C Standard: JESD22-A103					
Lot	Device	500-HOURS	Failure Code		
Q20090181AAHTSL	FDMS8692	0/77			
Q20090181BAHTSL	FDMS8672AS	0/77			
Q20090181CAHTSL	FDMS8670AS	0/77			
Test: (Highly Accelerated Stress Test) Conditions: 85%RH, 130C, 24V Standard: JESD22-A110					
Lot	Device	96-HOURS	Failure Code		
Q20090181AAHAST1	FDMS8692	0/77			
Q20090181BAHAST1	FDMS8672AS	0/77			
Q20090181CAHAST1	FDMS8670AS	0/77			
Test: (Power Cycle) Conditions: Delta 100C, 2 Min cycle Standard: MIL-STD-750-1036					
Lot	Device	5000-CYCLES	10000-CYCLES	Failure Code	
Q20090181AAPRCL	FDMS8692	0/77			
Q20090181AAPRCL	FDMS8692		0/77		
Q20090181BAPRCL	FDMS8672AS	0/77			
Q20090181BAPRCL	FDMS8672AS		0/77		
Q20090181CAPRCL	FDMS8670AS	0/77			
Q20090181CAPRCL	FDMS8670AS		0/77		
Test: (Precondition) Conditions: Standard: JESD22-A113					
Lot	Device	Results	Failure Code		
Q20090181AAPCNL1A	FDMS8692	0/231			
Q20090181BAPCNL1A	FDMS8672AS	0/231			
Q20090181CAPCNL1A	FDMS8670AS	0/231			
Test: (Temperature Cycle) Conditions: -65C, 150C Standard: JESD22-A104					
Lot	Device	100-CYCLES	500-CYCLES	Failure Code	
Q20090181AATMCL1	FDMS8692	0/77			
Q20090181AATMCL1	FDMS8692		0/77		
Q20090181BATMCL1	FDMS8672AS	0/77			
Q20090181BATMCL1	FDMS8672AS		0/77		
Q20090181CATMCL1	FDMS8670AS	0/77			
Q20090181CATMCL1	FDMS8670AS		0/77		
Test: (Unbiased HAST) Conditions: 85%RH, 130C Standard: JESD22-A118					
Lot	Device	96-HOURS	Failure Code		
Q20090181AAUHAST1	FDMS8692	0/77			
Q20090181BAUHAST1	FDMS8672AS	0/77			
Q20090181CAUHAST1	FDMS8670AS	0/77			

Product Id Description : Fairchild Semiconductor's selected MOSFET devices assembled in

Power 56 package will be affected by this change. Please refer to the Affected FSIDs section.

Affected FSIDs :

FDMS3500	FDMS3662	FDMS5352
FDMS6673BZ	FDMS6681Z	FDMS7660
FDMS7670	FDMS7672	FDMS8460
FDMS86101	FDMS8660AS	FDMS8662
FDMS8670	FDMS8670AS	FDMS8670S
FDMS8670S_SB82233	FDMS8672AS	FDMS8672S
FDMS8674	FDMS8680	FDMS8692
FDMS8848NZ	FDMS8880	