Date Created : **2009/06/11**
Date Issued On : **2009/11/24**
PCN# : **Q2092401**

DESIGN/PROCESS CHANGE NOTIFICATION -- FINAL

This is to inform you that a design and/or process change will be made to the following product(s). This notification is for your information and concurrence.

If you require data or samples to qualify this change, please contact **Fairchild Semiconductor within 30 days of receipt of this notification.**

Updated process quality documentation, such as FMEAs and Control Plans, are available for viewing upon request.

If you have any questions concerning this change, please contact:

Technical Contact:
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PCN Originator:
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Implementation of change:
Expected 1st Device Shipment Date: 2010/02/22

Earliest Year/Work Week of Changed Product: 1006

Change Type Description: Alternate Assembly/Test Location/Qualification, Assembly Process, Lead Finish Composition, Package External Dimension

Description of Change (From): Selected MOSFET products currently assembled in Power 56 package at Fairchild Semiconductor in Cebu, Philippines. Current singulation method is Saw Singulation; current plating finish is NiPdAu; and current Die Attach Pad & Leadpost plating is NiPdAu. To view "From/To" Marketing Outline Dimensions, please refer to the attached table "Marketing Outline Dimensions."

Description of Change (To): Selected MOSFET products assembled in Power 56 package will also be assembled at GEM Shanghai, China. The alternate singulation method will be Punched Singulation; alternate plating finish will be Pure Sn; and alternate Die Attach Pad & Leadpost plating will be Bare Cu.

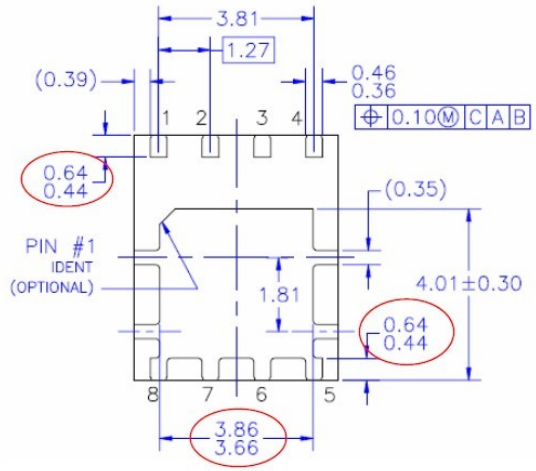
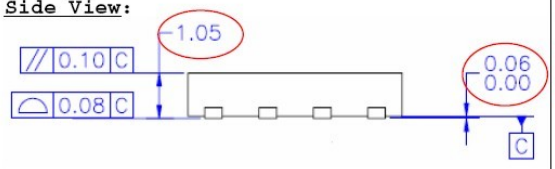
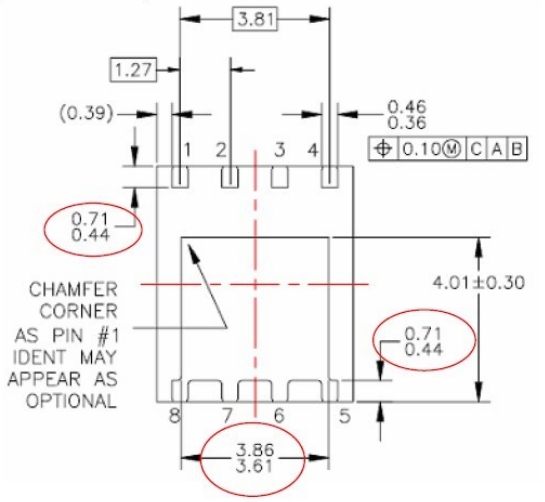
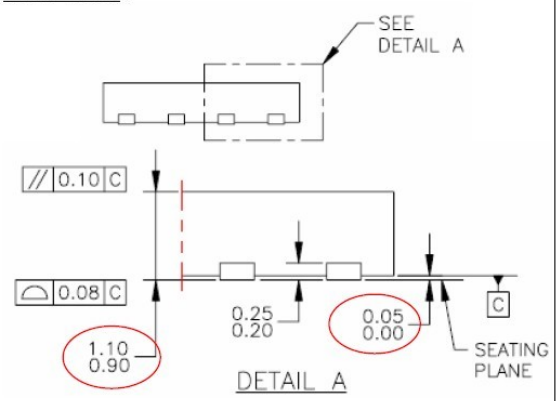
Reason for Change : Fairchild Semiconductor intends to qualify GEM Shanghai as an alternate assembly site for Power 56 package to support volume ramp. The Marketing Outline drawing has been updated to accommodate the dimensions for a punched singulated Power56, as illustrated in the table. There will be no change on the Part number as both parts share common landpattern dimensions and thus should be interchangeable from their end. The reference landpattern drawing is shown for reference. Fairchild Semiconductor's selected MOSFET devices assembled in Power 56 package will be affected by this change.

Qual/REL Plan Numbers : Q20080150

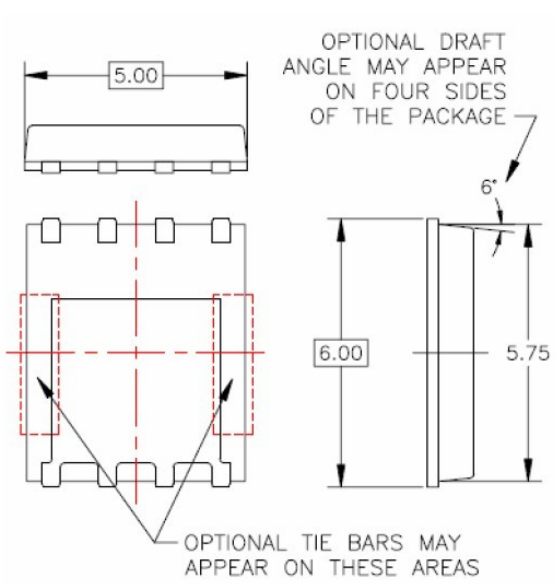
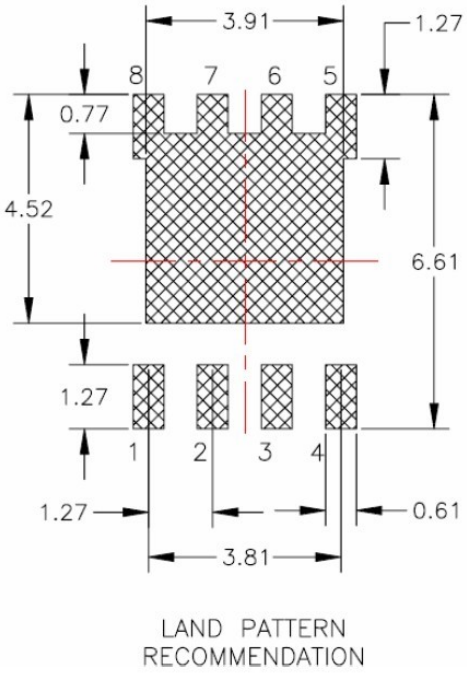
Qualification :

This change will not affect the devices' specifications or functional performance. Product quality, reliability and MSL performance will be maintained. There will be no change on the Part number as both parts share common landpattern dimensions and thus should be interchangeable from their end. The reliability qualification is complete and results are detailed in the attached table.

Change From

Description of Change: 5. Marketing Outline Dimensions	
FROM	**TO**
Bottom View:  **Leadlength (Pin 1-4): 0.44 – 0.64 mm** **Leadlength (Pin 5-8): 0.44 – 0.64 mm** **Exposed Pad length: 3.66 – 3.86 mm** **Notes:** **a) Pin #1 Identification Optional** **b) Tie-bar location and pitch specified** **Side View:**  **Package height: 1.05 mm** **Stand-off height: 0.00 – 0.06 mm**	**Bottom View:**  **Leadlength (Pin 1-4): 0.44 – 0.71 mm** **Leadlength (Pin 5-8): 0.44 – 0.71 mm** **Exposed Pad length: 3.61 – 3.86 mm** **Notes:** **a) Chamfer Corner as Pin#1 Ident may appear as optional** **b) Tie-bar location not specified** **Side View:**  **Package height: 0.90 – 1.10 mm** **Stand-off height: 0.00 – 0.05 mm** **Exposed leads height: 0.20 – 0.25 mm**

Change To

CHANGE TO: (Additional information)	LAND PATTERN RECOMMENDATION
 Notes: - Optional Draft Angle may appear on four sides of the package (6°) - Optional tie bars may appear on these areas - Molded Package length: 5.75 mm	 Both parts share common landpattern dimensions; the Marketing Outline drawing has also been updated to accommodate the dimensions for a punched singulated Power56

Results/Discussion for Qual Plan NumberQ20080150

Test: (High Temperature Gate Bias) | Conditions: 150C, 20V | Standard: JESD22-A108					
Lot	Device	168-HOURS	500-HOURS	1000-HOURS	Failure Code
Q20080150AAHTGB	FDMS8670S	0/77			
			0/77		
				0/77	
Q20080150ABHTGB		0/77			
			0/77		
				0/77	
Q20080150ACHTGB		0/77			
			0/77		
				0/77	
Q20080150BAHTGB	FDMS8680	0/77			
			0/77		
				0/77	

Test: (High Temperature Reverse Bias) | Conditions: 125C, 24V | Standard: JESD22-A108					
Lot	Device	168-HOURS	500-HOURS	1000-HOURS	Failure Code
Q20080150AAHTRB	FDMS8670S	0/77			
			0/77		
				0/77	
Q20080150ABHTRB		0/77			
			0/77		
				0/77	
Q20080150ACHTRB		0/77			
			0/77		
				0/77	

Test: (High Temperature Reverse Bias) | Conditions: 150C, 24V | Standard: JESD22-A108					
Lot	Device	168-HOURS	500-HOURS	1000-HOURS	Failure Code
Q20080150BAHTRB	FDMS8680	0/77			
			0/77		
				0/77	

Test: (Highly Accelerated Stress Test) | Conditions: 85%RH, 130C, 24V | Standard: JESD22-A110			
Lot	Device	96-HOURS	Failure Code
Q20080150AAHAST1	FDMS8670S	0/77	
Q20080150ABHAST1	FDMS8670S	0/77	
Q20080150ACHAST1	FDMS8670S	0/77	
Q20080150BAHAST1	FDMS8680	0/77	

Test: (Power Cycle) | Conditions: Delta 100C, 2 Min cycle | Standard: MIL-STD-750-1036				
Lot	Device	5000-CYCLES	10000-CYCLES	Failure Code
Q20080150AAPRCL	FDMS8670S	0/77		
Q20080150AAPRCL	FDMS8670S		0/77	
Q20080150ABPRCL	FDMS8670S	0/77		
Q20080150ABPRCL	FDMS8670S		0/77	
Q20080150ACPRCL	FDMS8670S	0/77		
Q20080150ACPRCL	FDMS8670S		0/77	
Q20080150BAPRCL	FDMS8680	0/77		
Q20080150BAPRCL	FDMS8680		0/77	

Test: (Precondition) | Conditions: | Standard: JESD22-A113			
Lot	Device	Results	Failure Code
Q20080150AAPCNL1A	FDMS8670S	0/154	
Q20080150ABPCNL1A	FDMS8670S	0/154	
Q20080150ACPCNL1A	FDMS8670S	0/154	
Q20080150BAPCNL1A	FDMS8680	0/154	

Test: (Temperature Cycle) | Conditions: -65C, 150C | Standard: JESD22-A104				
Lot	Device	100-CYCLES	500-CYCLES	Failure Code
Q20080150AATMCL1	FDMS8670S	0/77		
Q20080150AATMCL1	FDMS8670S		0/77	
Q20080150ABTMCL1	FDMS8670S	0/77		
Q20080150ABTMCL1	FDMS8670S		0/77	
Q20080150ACTMCL1	FDMS8670S	0/77		
Q20080150ACTMCL1	FDMS8670S		0/77	
Q20080150BATMCL1	FDMS8680	0/77		
Q20080150BATMCL1	FDMS8680		0/77	

Product Id Description : Fairchild Semiconductor's selected MOSFET devices assembled in Power 56 package will be affected by this change. Please refer to the Affected FSIDs section.

Affected FSIDs :

FDMS8680	FDMS8692	FDMS8880