# Trench Small Signal MOSFET

## 8 V, Dual P-Channel, SC-88 ESD Protection

#### **Features**

- Leading –8 V Trench for Low R<sub>DS(ON)</sub> Performance
- ESD Protected Gate
- Small Footprint (2 x 2 mm)
- Same Package as SC-70-6
- Pb-Free Packages are Available

#### **Applications**

- Load Power switching
- DC-DC Conversion
- Li-Ion Battery Charging Circuits
- Cell Phones, Media Players, Digital Cameras, PDAs

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise stated)

Param	Symbol	Value	Unit			
Drain-to-Source Voltage	V <sub>DSS</sub>	-8.0	V			
Gate-to-Source Voltage	) -		V <sub>GS</sub>	±8.0	V	
Continuous Drain Current	Steady State	T <sub>A</sub> = 25 °C	I <sub>D</sub>	-0.775	Α	
(Based on R <sub>θJA</sub> )	State	T <sub>A</sub> = 85 °C		-0.558		
Power Dissipation			$P_{D}$	0.27	W	
(Based on R <sub>θJA</sub> )	State	T <sub>A</sub> = 85 °C		0.14		
Continuous Drain Current	Steady State	T <sub>A</sub> = 25 °C	I <sub>D</sub>	-1.1	Α	
(Based on R <sub>θJL</sub> )	State	T <sub>A</sub> = 85 °C		-0.8		
Power Dissipation			_	0.55	W	
(Based on R <sub>θJL</sub> )	State	T <sub>A</sub> = 85 °C	$P_{D}$	0.29		
Pulsed Drain Current	I <sub>DM</sub>	±1.2	Α			
Operating Junction and	T <sub>J</sub> , T <sub>STG</sub>	–55 to 150	°C			
Continuous Source Curr	IS	-0.775	Α			
Lead Temperature for So (1/8" from case for 10 s)	TL	260	°C			

#### THERMAL RESISTANCE RATINGS (Note 1)

Parameter	Symbol	Тур	Max	Unit
Junction-to-Ambient - Steady State	$R_{\theta JA}$	400	460	°C/W
Junction-to-Lead (Drain) - Steady State	$R_{ heta JL}$	194	226	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted on FR4 board using 1 oz Cu area = 0.9523 in sq.

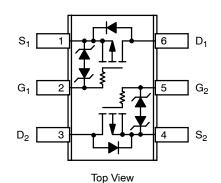


#### ON Semiconductor®

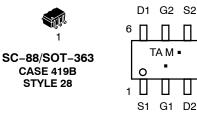
#### http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> Max		
	0.22 Ω @ -4.5 V			
-8 V	0.32 Ω @ -2.5 V	–0.775 A		
	0.51 Ω @ –1.8 V			

#### SOT-363 SC-88 (6 LEADS)



### MARKING DIAGRAM & PIN ASSIGNMENT



TA = Device Code
M = Date Code
Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

#### **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub>=25°C unless otherwise stated)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS			<u>.</u>				
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D$	-8.0	-10.5		V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	V(BR)DSS/ T <sub>J</sub>				-6.0		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 \text{ V}, V_{D}$	<sub>S</sub> = -6.4 V			1.0	μΑ
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{G}$	<sub>iS</sub> = ±8.0 V			10	μΑ
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , ID	= -250 μA	-0.45	-0.83	-1.0	V
Gate Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				2.2		mV/ °C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I	<sub>D</sub> = -0.57 A		0.22	0.3	Ω
		V <sub>GS</sub> = -2.5 V, I	<sub>D</sub> = -0.48 A		0.32	0.46	1
		V <sub>GS</sub> = -1.8 V, I	<sub>D</sub> = -0.20 A		0.51	0.9	7
Forward Transconductance	9FS	$V_{GS} = -4.0 \text{ V}, I_D =$	-0.57 A		2.0		S
CHARGES AND CAPACITANCES							
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f =	1.0 MHz,		160	225	pF
Output Capacitance	C <sub>OSS</sub>	V <sub>DS</sub> = −8.0 V			38	55	7
Reverse Transfer Capacitance	C <sub>RSS</sub>				28	40	7
Total Gate Charge	Q <sub>G(TOT)</sub>	$V_{GS} = -4.5 \text{ V, V}$ $I_{D} = -0$	<sub>DS</sub> = -5.0 V,		2.2	4.0	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	I <sub>D</sub> = -0	.6 A		0.1		7
Gate-to-Source Charge	$Q_{GS}$		Ī		0.5		
Gate-to-Drain Charge	$Q_{GD}$	1	Ī		0.5		7
SWITCHING CHARACTERISTICS (No	ote 3)						
Turn-On Delay Time	td <sub>(ON)</sub>	V <sub>GS</sub> = -4.5 V, V	<sub>DD</sub> = -4.0 V,		13		ns
Rise Time	tr	$V_{GS} = -4.5 \text{ V}, V_{DD} = -4.0 \text{ V},$ $I_{D} = -0.5 \text{ A}, R_{G} = 8.0 \Omega$			23		7
Turn-Off Delay Time	td <sub>(OFF)</sub>				50		7
Fall Time	tf				36		1
DRAIN-SOURCE DIODE CHARACTE	RISTICS						
Forward Diode Voltage	$V_{SD}$	V <sub>GS</sub> = 0 V,	T <sub>J</sub> = 25°C		0.76	1.1	V
		$I_S = -0.23 \text{ A}$ $T_J = 125^{\circ}\text{C}$			0.63		7
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, } dI_{S}/dt = 100 \text{ A/}\mu\text{s,}$ $I_{S} = -0.77 \text{ A}$			78		ns

Pulse Test: pulse width ≤ 300μs, duty cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

#### TYPICAL PERFORMANCE CURVES (T<sub>J</sub> = 25°C unless otherwise noted)

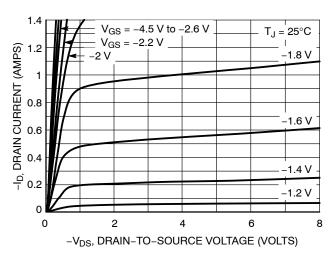


Figure 1. On-Region Characteristics

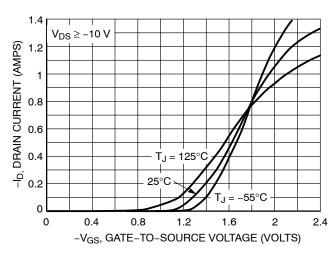


Figure 2. Transfer Characteristics

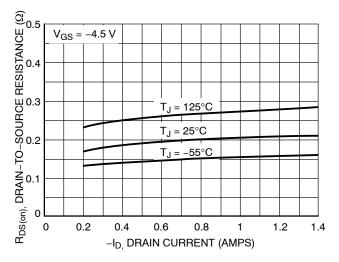


Figure 3. On-Resistance vs. Drain Current and Temperature

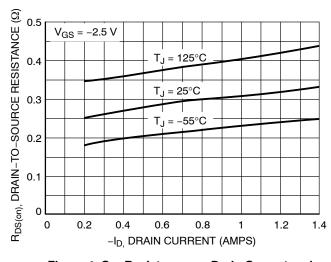


Figure 4. On–Resistance vs. Drain Current and Temperature

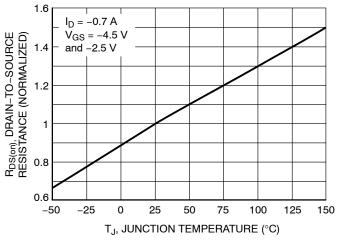


Figure 5. On–Resistance Variation with Temperature

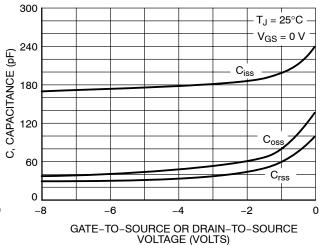


Figure 6. Capacitance Variation

#### TYPICAL PERFORMANCE CURVES ( $T_J = 25^{\circ}C$ unless otherwise noted)

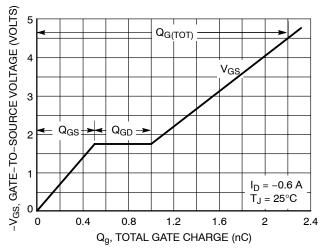


Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

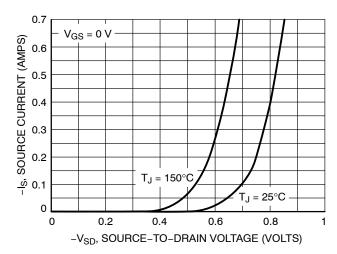


Figure 8. Diode Forward Voltage vs. Current

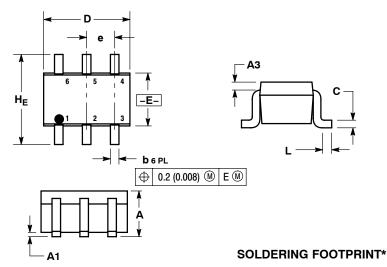
#### **ORDERING INFORMATION**

Device Order Number	Package Type	Tape and Reel Size <sup>†</sup>
NTJD2152PT1	SOT-363	3000 / Tape & Reel
NTJD2152PT1G	SOT-363 (Pb-Free)	3000 / Tape & Reel
NTJD2152PT2	SOT-363	3000 / Tape & Reel
NTJD2152PT2G	SOT-363 (Pb-Free)	3000 / Tape & Reel
NTJD2152PT4	SOT-363	10,000 / Tape & Reel
NTJD2152PT4G	SOT-363 (Pb-Free)	10,000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

#### SC-88/SC70-6/SOT-363 CASE 419B-02 **ISSUE W**



#### NOTES:

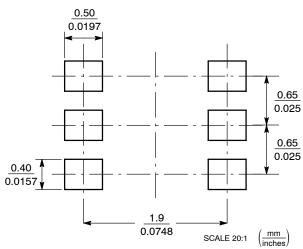
- DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
- 419B-01 OBSOLETE, NEW STANDARD 419B-02.

		MIL	LIMETE	ERS	INCHES			
D	MIC	MIN	NOM	MAX	MIN	NOM	MAX	
	Α	0.80	0.95	1.10	0.031	0.037	0.043	
	41	0.00	0.05	0.10	0.000	0.002	0.004	
	43	0.20 REF 0.008 REF				EF.		
	b	0.10	0.21	0.30	0.004	0.008	0.012	
	၁	0.10	0.14	0.25	0.004	0.005	0.010	
	D	1.80	2.00	2.20	0.070	0.078	0.086	
	Е	1.15 1.25		1.35	0.045	0.049	0.053	
	е	0.65 BSC			0.026 BSC			
	L	0.10	0.20	0.30	0.004	0.008	0.012	
H	ΙE	2.00	2.10	2.20	0.078	0.082	0.086	

#### STYLE 26:

- PIN 1. SOURCE 1 2. GATE 1

  - 3. DRAIN 2
  - 4. SOURCE 2
  - GATE 2 DRAIN



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and 📖 are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### **PUBLICATION ORDERING INFORMATION**

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 61312, Phoenix, Arizona 85082-1312 USA Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free

Japan: ON Semiconductor, Japan Customer Focus Center 2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051 Phone: 81-3-5773-3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.

NTJD2152P/D