

FDW2512NZ

Dual N-Channel 2.5V Specified PowerTrench® MOSFET

Features

- 6A, 20V $r_{DS(ON)} = 0.028\Omega$, $V_{GS} = 4.5V$
 $r_{DS(ON)} = 0.036\Omega$, $V_{GS} = 2.5V$
- Extended V_{GS} range ($\pm 12V$) for battery applications
- HBM ESD Protection Level of 3.5kV Typical (note 3)
- High performance trench technology for extremely low $r_{DS(ON)}$
- Low profile TSSOP-8 package

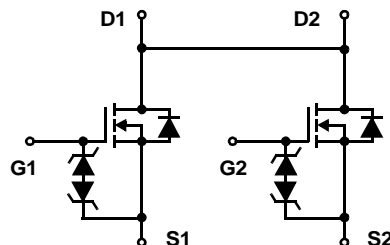
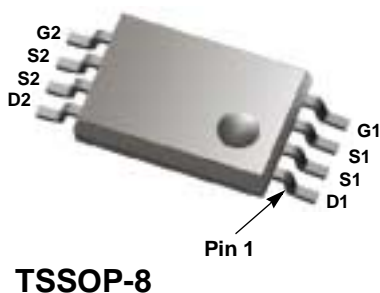
Applications

- Load switch
- Battery charge
- Battery disconnect circuits



General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance. These devices are well suited for portable electronics applications.



FDW2512NZ Dual N-Channel 2.5V Specified PowerTrench® MOSFET

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	20	V
V_{GS}	Gate to Source Voltage	± 12	V
I_D	Drain Current		
	Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 4.5\text{V}$, $R_{\theta JA} = 77^\circ\text{C/W}$)	6.0	A
	Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 2.5\text{V}$, $R_{\theta JA} = 77^\circ\text{C/W}$)	3.3	A
	Pulsed	Figure 4	A
P_D	Power dissipation	1.6	W
	Derate above 25°C	13	mW/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 1)	77	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 2)	114	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
2512NZ	FDW2512NZ	TSSOP-8	13"	12 mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{V}$ $V_{GS} = 0\text{V}$	-	-	1	μA
		$T_A = 100^\circ\text{C}$	-	-	5	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{V}$	-	-	± 10	μA
		$V_{GS} = \pm 4.5\text{V}$			± 250	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	0.6	0.8	1.5	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 6.0\text{A}$, $V_{GS} = 4.5\text{V}$	-	0.017	0.028	Ω
		$I_D = 5.9\text{A}$, $V_{GS} = 4.0\text{V}$	-	0.018	0.029	
		$I_D = 5.3\text{A}$, $V_{GS} = 3.1\text{V}$	-	0.019	0.035	
		$I_D = 5.3\text{A}$, $V_{GS} = 2.5\text{V}$	-	0.022	0.036	

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 10\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	670	-	pF	
C_{OSS}	Output Capacitance		-	170	-	pF	
C_{RSS}	Reverse Transfer Capacitance		-	115	-	pF	
R_G	Gate Resistance	$V_{GS} = 0.5\text{V}$, $f = 1\text{MHz}$	-	4.2	-	Ω	
$Q_{g(TOT)}$	Total Gate Charge at 4.5V	$V_{GS} = 0\text{V}$ to 4.5V	$V_{DD} = 10\text{V}$ $I_D = 6.0\text{A}$ $I_g = 1.0\text{mA}$	-	8	12	nC
$Q_{g(2.5)}$	Total Gate Charge at 2.5V	$V_{GS} = 0\text{V}$ to 2.5V		-	5.1	7.6	nC
Q_{gs}	Gate to Source Gate Charge			-	1.1	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	2.2	-	nC

Switching Characteristics ($V_{GS} = 4.5V$)

t_{ON}	Turn-On Time	$V_{DD} = 10V, I_D = 6.0A$ $V_{GS} = 4.5V, R_{GS} = 16\Omega$	-	-	98	ns
$t_{d(ON)}$	Turn-On Delay Time		-	8	-	ns
t_r	Rise Time		-	57	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	47	-	ns
t_f	Fall Time		-	58	-	ns
t_{OFF}	Turn-Off Time		-	-	158	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 1.3A$	-	0.7	1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 6.0A, dI_{SD}/dt = 100A/\mu s$	-	-	24	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 6.0A, dI_{SD}/dt = 100A/\mu s$	-	-	13	nC

Notes:

- $R_{\theta JA}$ is 77 °C/W (steady state) when mounted on a 1 inch² copper pad on FR-4.
- $R_{\theta JA}$ is 114 °C/W (steady state) when mounted on a minimum copper pad on FR-4.
- The diode connected to the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristic $T_A = 25^\circ\text{C}$ unless otherwise noted

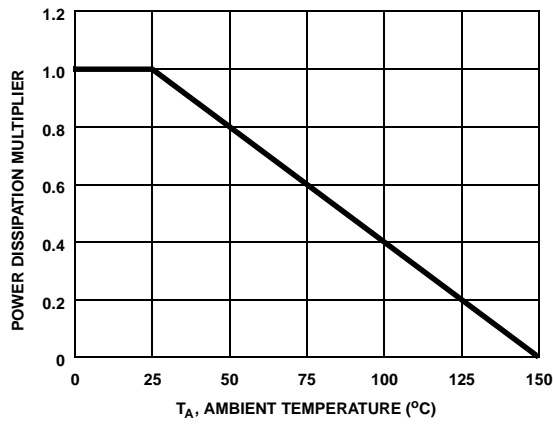


Figure 1. Normalized Power Dissipation vs Ambient Temperature

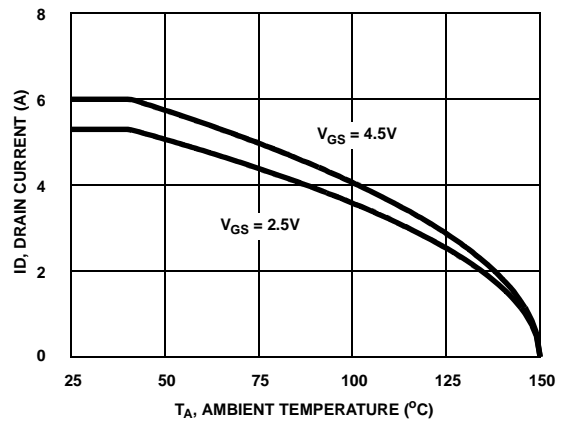


Figure 2. Maximum Continuous Drain Current vs Ambient Temperature

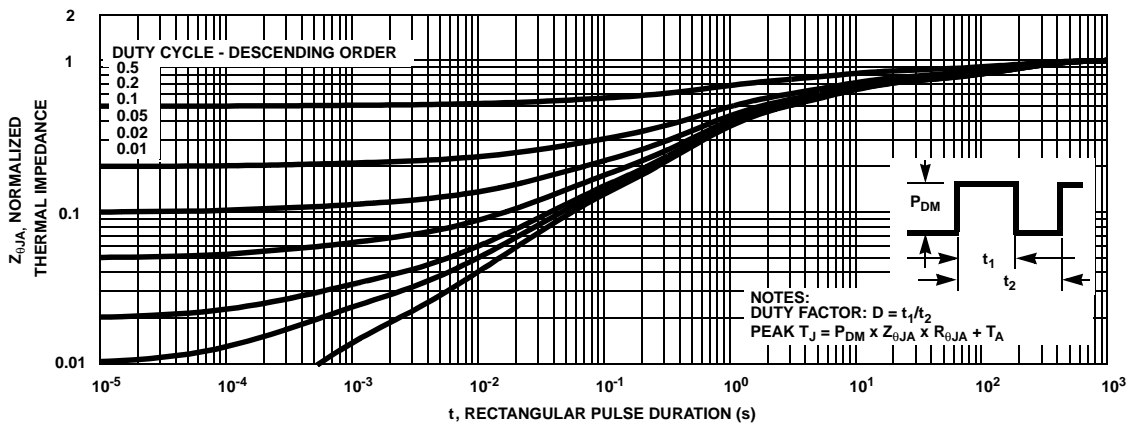


Figure 3. Normalized Maximum Transient Thermal Impedance

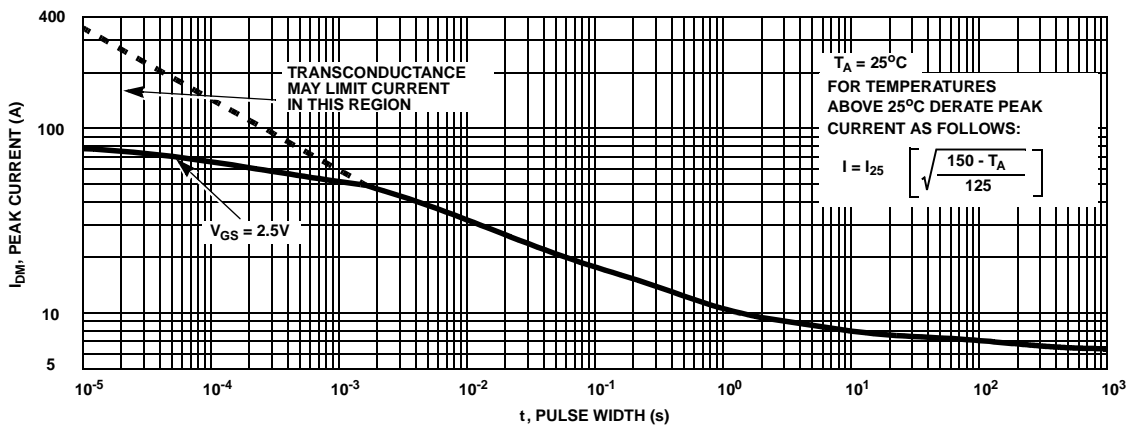


Figure 4. Peak Current Capability

Typical Characteristic (Continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

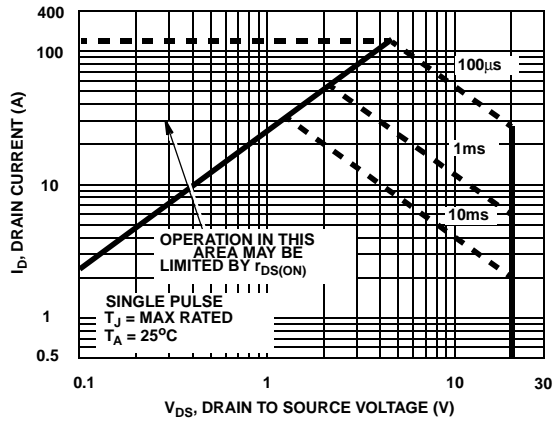


Figure 5. Forward Bias Safe Operating Area

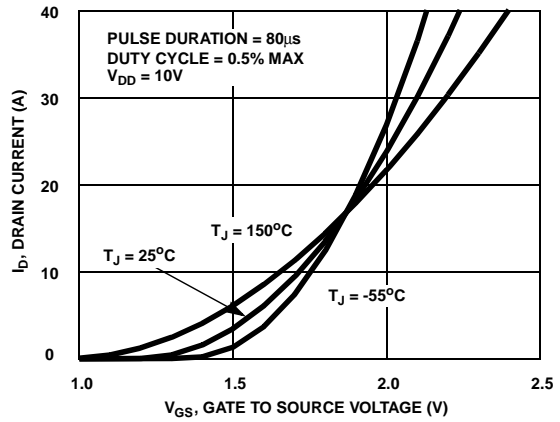


Figure 6. Transfer Characteristics

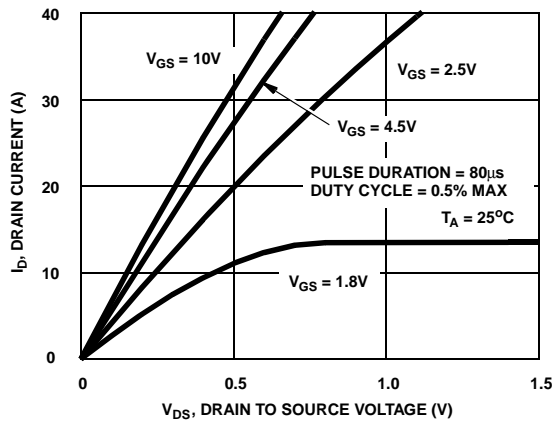


Figure 7. Saturation Characteristics

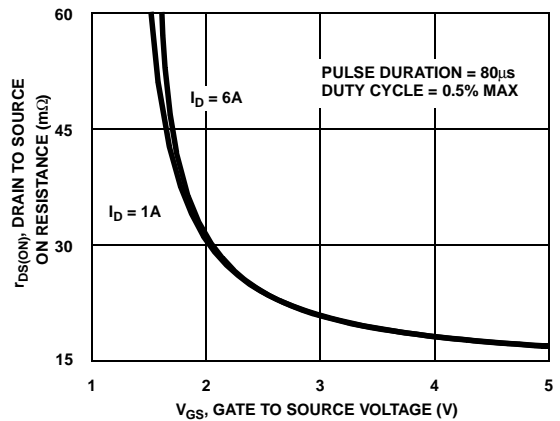


Figure 8. Drain to Source On Resistance vs Gate Voltage and Drain Current

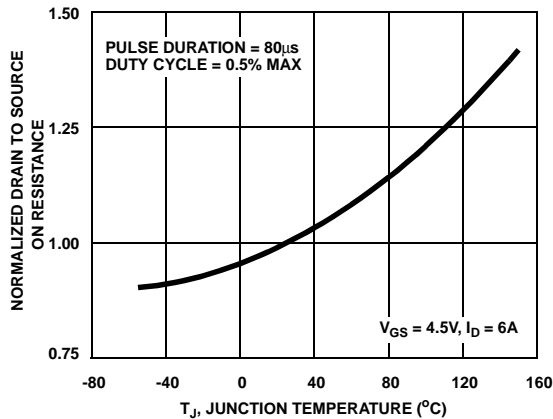


Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature

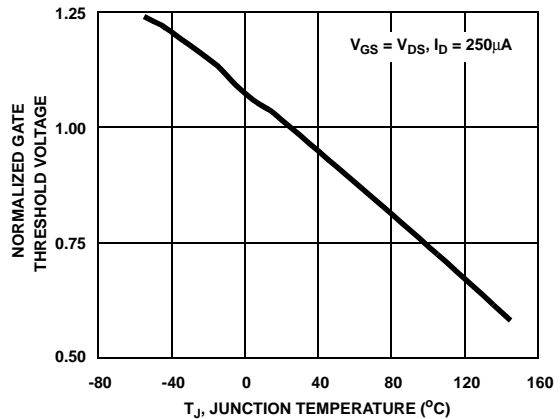


Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

Typical Characteristic (Continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

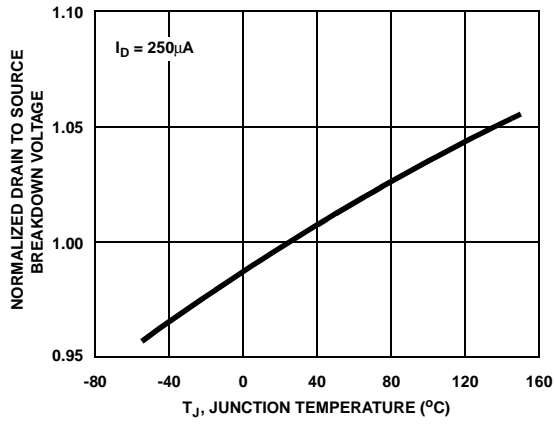


Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

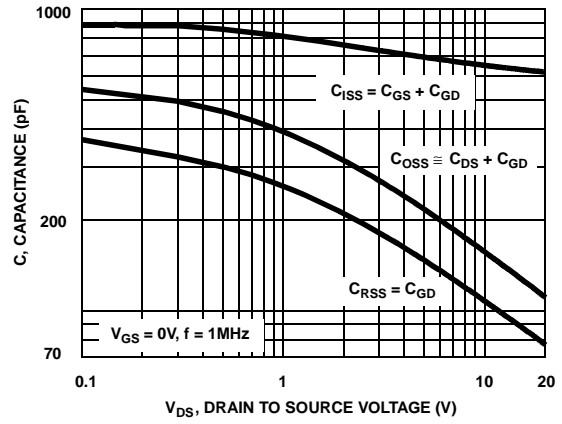


Figure 12. Capacitance vs Drain to Source Voltage

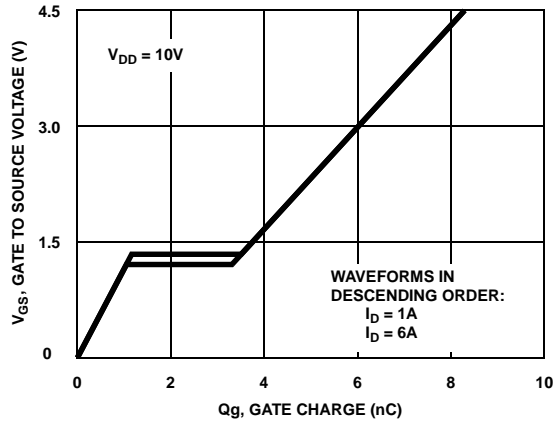


Figure 13. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms

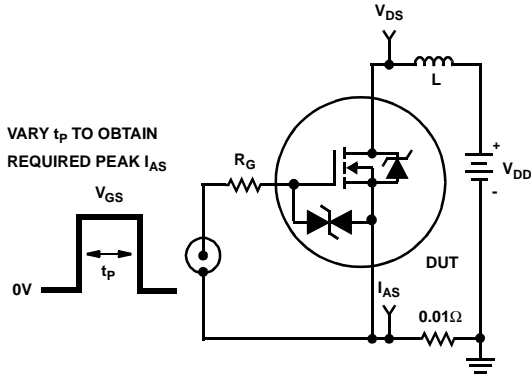


Figure 14. Unclamped Energy Test Circuit

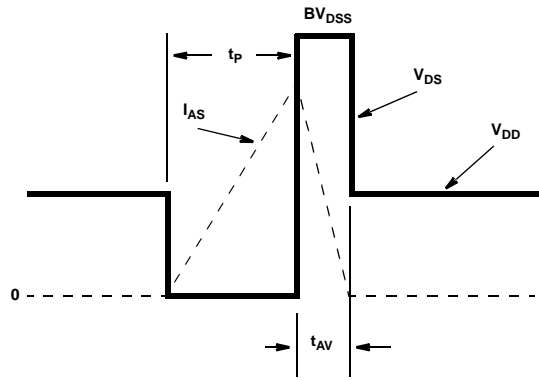


Figure 15. Unclamped Energy Waveforms

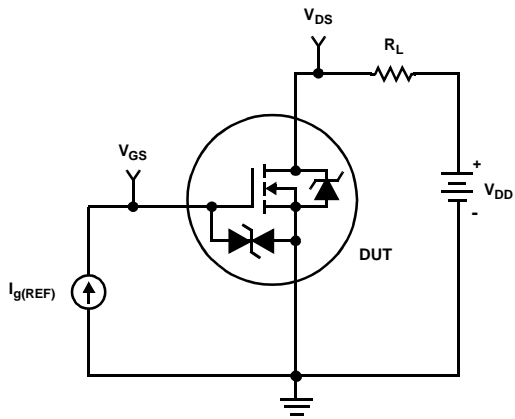


Figure 16. Gate Charge Test Circuit

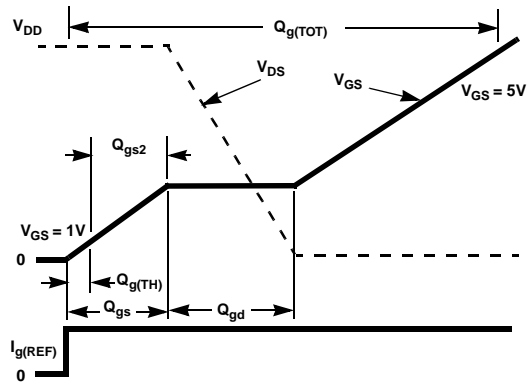


Figure 17. Gate Charge Waveforms

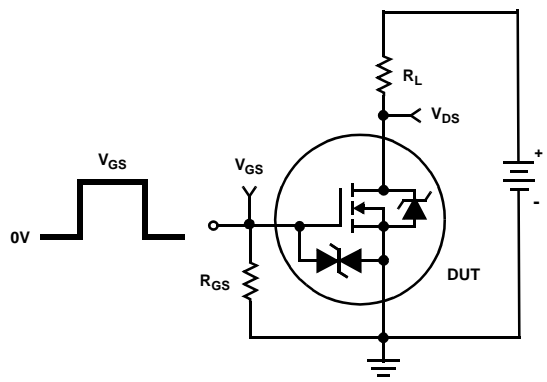


Figure 18. Switching Time Test Circuit

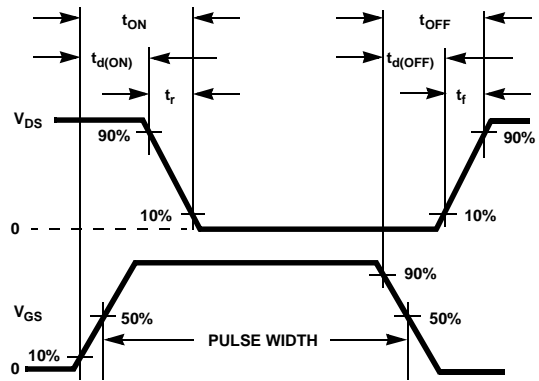


Figure 19. Switching Time Waveforms

PSPICE Electrical Model

.SUBCKT FDW2512NZ 2 1 3 ; rev July 2004
 CA 12 8 8.8e-10
 CB 15 14 8.8e-10
 CIN 6 8 0.5e-9

DBODY 5 7 DBODYMOD
 DBREAK 5 11 DBREAKMOD
 DPLCAP 10 5 DPLCAPMOD
 DESD1 91 9 DESD1MODE
 DESD2 91 7 DESD2MOD
 EBREAK 7 11 17 18 22.2
 EDS 14 8 5 8 1
 EGS 13 8 6 8 1
 ESG 6 10 8 6 1
 EVTHRES 6 21 19 8 1
 EVTEMP 6 20 18 22 1
 IT 8 17 1
 LGATE 1 9 1.49e-9
 LDRAIN 2 5 1e-9 1
 LGATE 1 9 1.49e-9
 LSOURCE 3 7 0.2e-9

RLDRAIN 2 5 10
 RLGATE 1 9 14.9
 RLSOURCE 3 7 2.0

MMED 16 6 8 8 MMEDMOD
 MSTRO 16 6 8 8 MSTROMOD
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
 RDRAIN 50 16 RDRAINMOD 13.1e-3
 RGATE 9 20 5.57
 RSLC1 5 51 RSLCMOD 1e-6
 RSLC2 5 50 1e3
 RSOURCE 8 7 RSOURCEMOD 2e-4
 RVTHRES 22 8 RVTHRESMOD 1
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
 S1B 13 12 13 8 S1BMOD
 S2A 6 15 14 13 S2AMOD
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

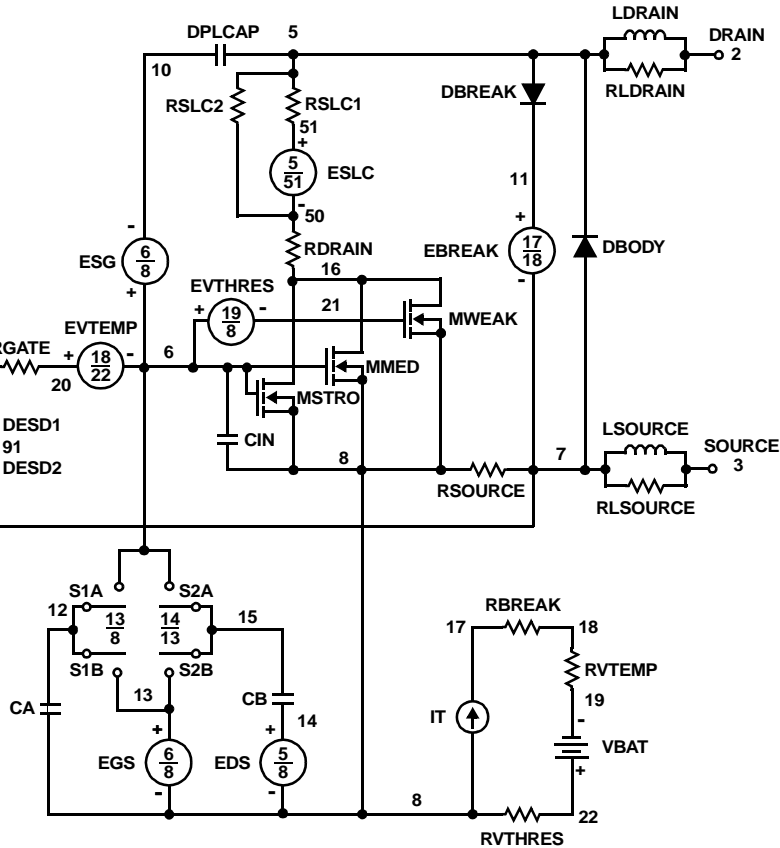
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*120),2.5))}

.MODEL DBODYMOD D (IS = 7.3e-12 N=0.93 RS = 20.6e-3 IKF=0.2 TRS1 = 1.7e-3 TRS2 = 2e-6 XTI=0.2 TIKF=0.001
 CJO = 2.0e-10 TT=1.05e-8 M = 0.58)
 .MODEL DBREAKMOD D (RS = 1e-1 TRS1 = 9e-3 TRS2 = -2e-5)
 .MODEL DPLCAPMOD D (CJO = 0.37e-9 IS = 1e-30 N = 10 M = 0.51)
 .MODEL DESD1MOD D (BV=14 RS=1)
 .MODEL DESD2MOD D (BV=14 N=1.3 RS=1)
 .MODEL MMEDMOD NMOS (VTO = 0.96 KP = 1.98 IS=1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 5.57)
 .MODEL MSTROMOD NMOS (VTO = 1.2 KP = 72 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
 .MODEL MWEAKMOD NMOS (VTO = 0.72 KP = 0.02 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 55.7 RS = 0.1)

.MODEL RBREAKMOD RES (TC1 = 6e-4 TC2 = -5e-7)
 .MODEL RDRAINMOD RES (TC1 = 6e-4 TC2 = 1.2e-5)
 .MODEL RSLCMOD RES (TC1 = 1e-9 TC2 = 1e-8)
 .MODEL RSOURCEMOD RES (TC1 = 8.2e-2 TC2 = 1e-6)
 .MODEL RVTHRESMOD RES (TC1 = -13e-4 TC2 = -2.5e-6)
 .MODEL RVTEMPMOD RES (TC1 = -1.0e-3 TC2 = 1e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5 VOFF = -1.5)
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.5 VOFF = -5)
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.4 VOFF = 0.4)
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.4 VOFF = -0.4)
 ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SPICE Thermal Model

REV July 2004
 FDW2512NZ_JA Junction Ambient
 Minimum copper pad area

CTHERM1 Junction c2 5.7e-4
 CTHERM2 c2 c3 5.72e-4
 CTHERM3 c3 c4 5.8e-4
 CTHERM4 c4 c5 4.7e-3
 CTHERM5 c5 c6 5.1e-3
 CTHERM6 c6 c7 0.02
 CTHERM7 c7 c8 0.2
 CTHERM8 c8 Ambient 6

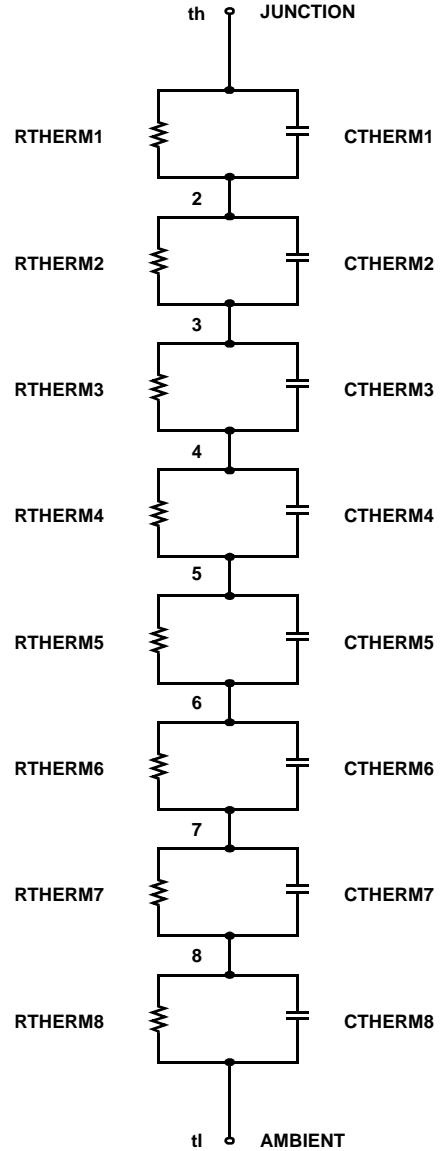
RTHERM1 Junction c2 0.003
 RTHERM2 c2 c3 0.25
 RTHERM3 c3 c4 1.0
 RTHERM4 c4 c5 1.1
 RTHERM5 c5 c6 7.5
 RTHERM6 c6 c7 33.6
 RTHERM7 c7 c8 33.7
 RTHERM8 c8 Ambient 33.8

SABER Thermal Model

SABER thermal model FDW2512NZ
 Minimum copper pad area
 template thermal_model th tl
 thermal_c th, tl

```
{
    ctherm.ctherm1 th c2 = 5.7e-4
    ctherm.ctherm2 c2 c3 = 5.72e-4
    ctherm.ctherm3 c3 c4 = 5.8e-4
    ctherm.ctherm4 c4 c5 = 4.7e-3
    ctherm.ctherm5 c5 c6 = 5.1e-3
    ctherm.ctherm6 c6 c7 = 0.02
    ctherm.ctherm7 c7 c8 = 0.2
    ctherm.ctherm8 c8 tl = 6
}
```




```
rtherm.rtherm1 th c2 = 0.003
rtherm.rtherm2 c2 c3 = 0.25
rtherm.rtherm3 c3 c4 = 1.0
rtherm.rtherm4 c4 c5 = 1.1
rtherm.rtherm5 c5 c6 = 7.5
rtherm.rtherm6 c6 c7 = 33.6
rtherm.rtherm7 c7 c8 = 33.7
rtherm.rtherm8 c8 tl = 33.8
}
```





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