

NTGD4167C

Power MOSFET

Complementary, 30 V, +2.9/-2.2 A,
TSOP-6 Dual

Features

- Complementary N-Channel and P-Channel MOSFET
- Small Size (3 x 3 mm) Dual TSOP-6 Package
- Leading Edge Trench Technology for Low On Resistance
- Reduced Gate Charge to Improve Switching Response
- Independently Connected Devices to Provide Design Flexibility
- This is a Pb-Free Device

Applications

- DC-DC Conversion Circuits
- Load/Power Switching with Level Shift

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V _{DSS}	30	V
Gate-to-Source Voltage (N-Ch & P-Ch)		V _{GS}	±12	V
N-Channel Continuous Drain Current (Note 1)	Steady State T _A = 25°C T _A = 85°C	I _D	2.6 1.9	A
	t ≤ 5 s T _A = 25°C		2.9	
P-Channel Continuous Drain Current (Note 1)	Steady State T _A = 25°C T _A = 85°C	I _D	-1.9 -1.4	A
	t ≤ 5 s T _A = 25°C		-2.2	
Power Dissipation (Note 1)	Steady State T _A = 25°C	P _D	0.9	W
	t ≤ 5 s		1.1	
Pulsed Drain Current	N-Ch P-Ch	I _{DM}	8.6 -6.3	A
Operating Junction and Storage Temperature		T _J , T _{STG}	-55 to 150	°C
Source Current (Body Diode)		I _S	±0.9	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T _L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient - Steady State (Note 1)	R _{θJA}	140	°C/W
Junction-to-Ambient - t ≤ 5 s (Note 1)	R _{θJA}	110	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

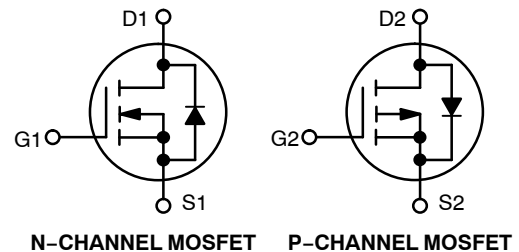
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).



ON Semiconductor®

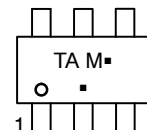
<http://onsemi.com>

V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX (Note 1)
N-Ch 30 V	90 mΩ @ 4.5 V	2.6 A
	125 mΩ @ 2.5 V	2.2 A
P-Ch -30 V	170 mΩ @ -4.5 V	-1.9 A
	300 mΩ @ -2.5 V	-1.0 A



TSOP-6
CASE 318G
STYLE 13

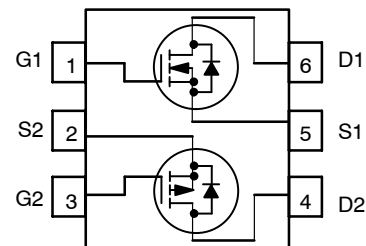
MARKING DIAGRAM



TA = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTION



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	N	V _{GS} = 0 V	I _D = 250 μA	30		V
		P		I _D = -250 μA	-30		
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	N			21.4		mV/°C
		P			22.2		
Zero Gate Voltage Drain Current	I _{DSS}	N	V _{GS} = 0 V, V _{DS} = 24 V	T _J = 25 °C		1.0	μA
		P	V _{GS} = 0 V, V _{DS} = -24 V			-1.0	
		N	V _{GS} = 0 V, V _{DS} = 24 V	T _J = 85 °C		10	
		P	V _{GS} = 0 V, V _{DS} = -24 V			-10	
Gate-to-Source Leakage Current	I _{GSS}	N	V _{DS} = 0 V, V _{GS} = ±12 V			±100	nA
		P	V _{DS} = 0 V, V _{GS} = ±12 V			±100	

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V _{GS(TH)}	N	V _{GS} = V _{DS}	I _D = 250 μA	0.5	0.9	1.5	V	
		P		I _D = -250 μA	-0.5	-1.1	-1.5		
Drain-to-Source On Resistance	R _{DS(on)}	N	V _{GS} = 4.5 V, I _D = 2.6 A	V _{GS} = 2.5 V, I _D = 2.2 A		52	90	mΩ	
							67		125
		P			V _{GS} = -4.5 V, I _D = -1.9 A		130		170
							V _{GS} = -2.5 V, I _D = -1.0 A		
Forward Transconductance	g _{FS}	N	V _{DS} = 15 V, I _D = 2.6 A		2.6		S		
		P	V _{DS} = -15 V, I _D = -1.9 A		2.6				

CHARGES AND CAPACITANCES

Input Capacitance	C _{ISS}	N	f = 1 MHz, V _{GS} = 0 V	V _{DS} = 15 V		295		pF
Output Capacitance	C _{OSS}					48		
Reverse Transfer Capacitance	C _{RSS}					27		
Input Capacitance	C _{ISS}	P		V _{DS} = -15 V		419		
Output Capacitance	C _{OSS}					51		
Reverse Transfer Capacitance	C _{RSS}					26		
Total Gate Charge	Q _{G(TOT)}	N	V _{GS} = 4.5 V, V _{DS} = 15 V, I _D = 2.0 A		3.7	5.5	nC	
Threshold Gate Charge	Q _{G(TH)}				0.6			
Gate-to-Source Gate Charge	Q _{GS}				0.9			
Gate-to-Drain "Miller" Charge	Q _{GD}				0.8			
Total Gate Charge	Q _{G(TOT)}	P		V _{GS} = -4.5 V, V _{DS} = -15 V, I _D = -2.0 A		3.9		6.0
Threshold Gate Charge	Q _{G(TH)}					0.6		
Gate-to-Source Gate Charge	Q _{GS}					1.0		
Gate-to-Drain "Miller" Charge	Q _{GD}					1.0		

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	t _{d(ON)}	N	V _{GS} = 4.5 V, V _{DD} = 15 V, I _D = 1.0 A, R _G = 6.0 Ω		7.0		ns	
Rise Time	t _r				4.0			
Turn-Off Delay Time	t _{d(OFF)}				14			
Fall Time	t _f				2.0			
Turn-On Delay Time	t _{d(ON)}	P		V _{GS} = -4.5 V, V _{DD} = -15 V, I _D = -1.0 A, R _G = 6.0 Ω		8.0		
Rise Time	t _r					8.0		
Turn-Off Delay Time	t _{d(OFF)}					22		
Fall Time	t _f					8.0		

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

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3. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V _{SD}	N	V _{GS} = 0 V, T _J = 25 °C	I _S = 0.9 A	0.7	1.2	V
		P		I _S = -0.9 A	-0.8	-1.2	
Reverse Recovery Time	t _{RR}	N	V _{GS} = 0 V, dI _S / dt = 100 A/μs, I _S = 0.9 A		8.0		ns
Charge Time	t _a				5.0		
Discharge Time	t _b				3.0		
Reverse Recovery Charge	Q _{RR}				3.0		
Reverse Recovery Time	t _{RR}	P	V _{GS} = 0 V, dI _S / dt = 100 A/μs, I _S = -0.9 A		12		ns
Charge Time	t _a				10		
Discharge Time	t _b				2.0		
Reverse Recovery Charge	Q _{RR}				7.0		

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N-CHANNEL TYPICAL CHARACTERISTICS

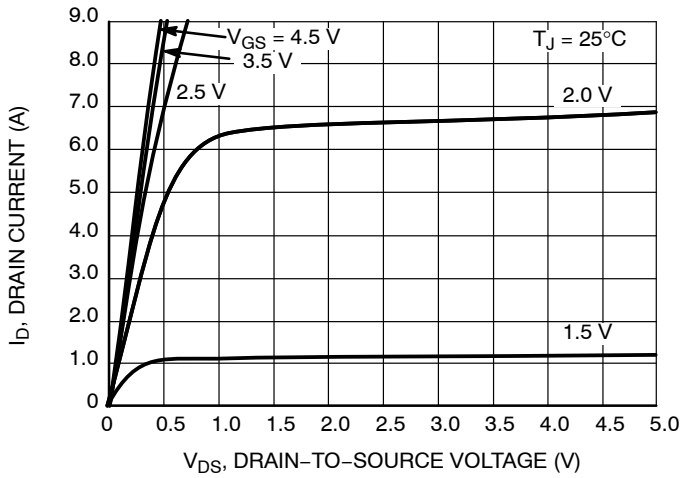


Figure 1. On-Region Characteristics

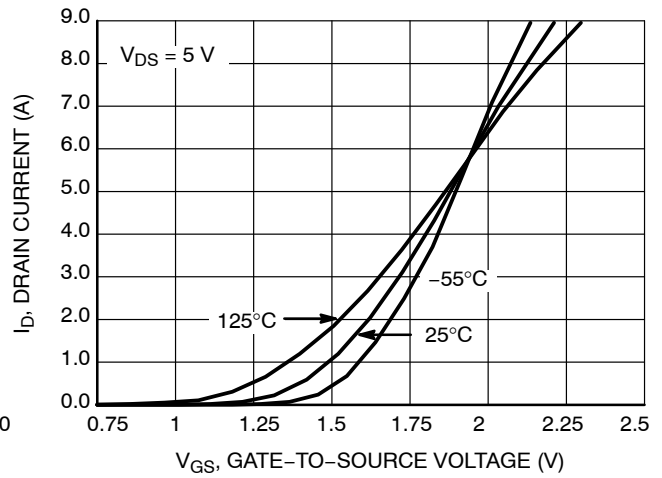


Figure 2. Transfer Characteristics

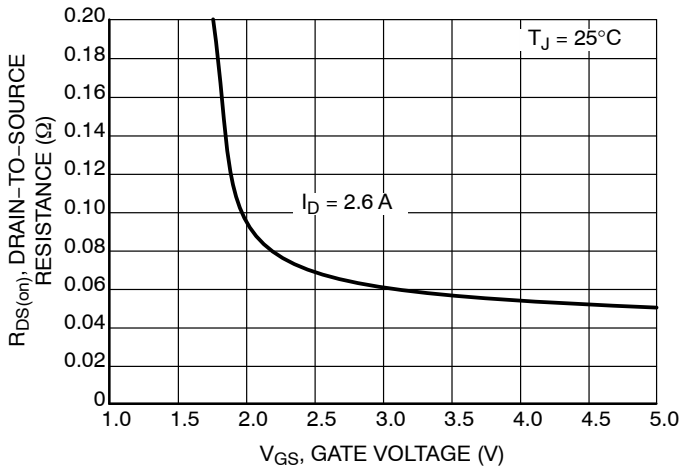


Figure 3. On-Region vs. Gate-To-Source Voltage

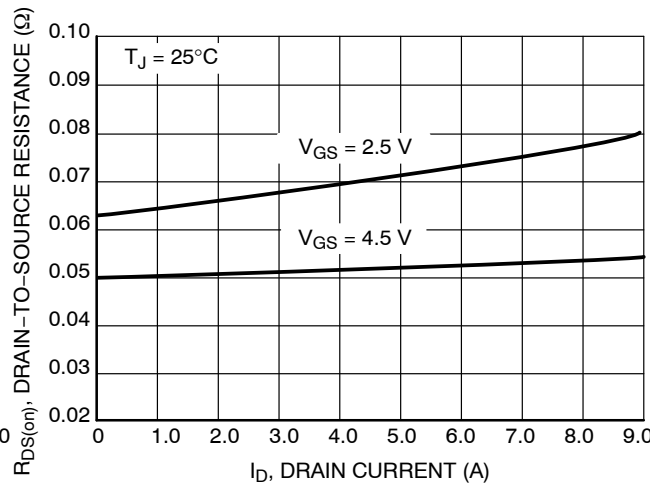


Figure 4. On-Resistance vs. Drain Current and Temperature

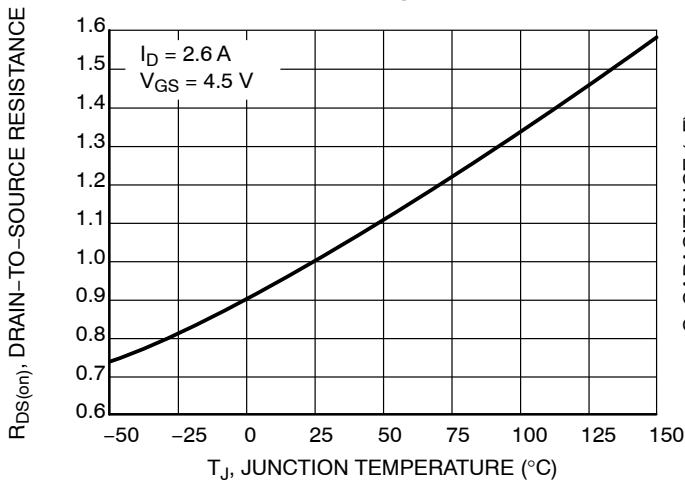


Figure 5. On-Resistance Variation with Temperature

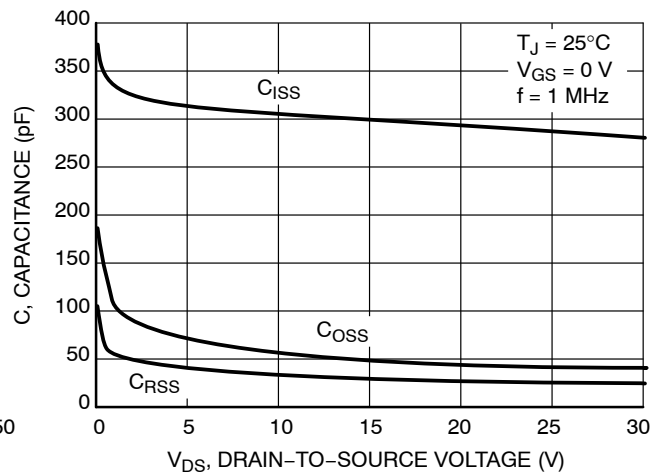


Figure 6. Capacitance Variation

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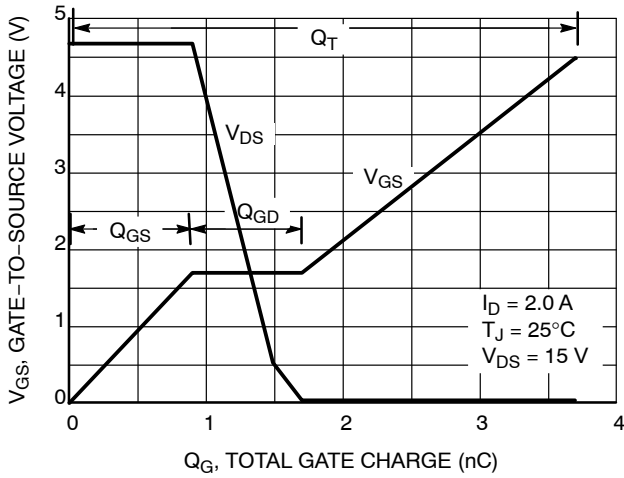


Figure 7. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

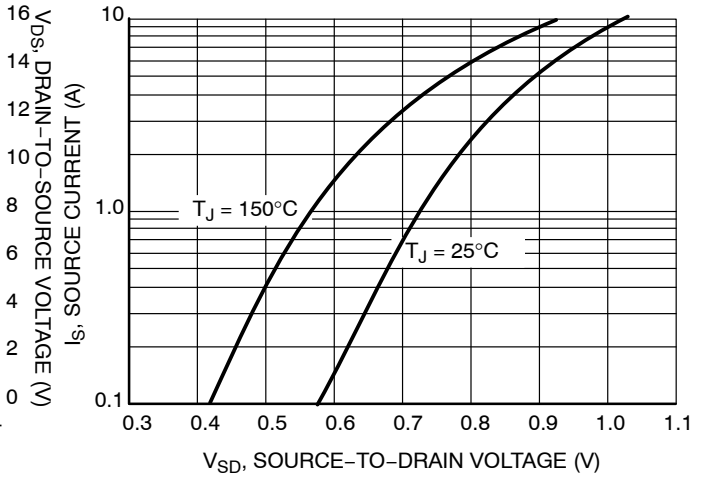


Figure 8. Diode Forward Voltage versus Current

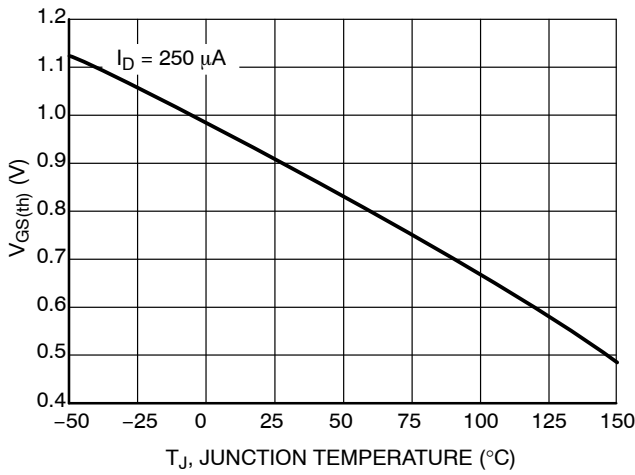


Figure 9. Threshold Voltage

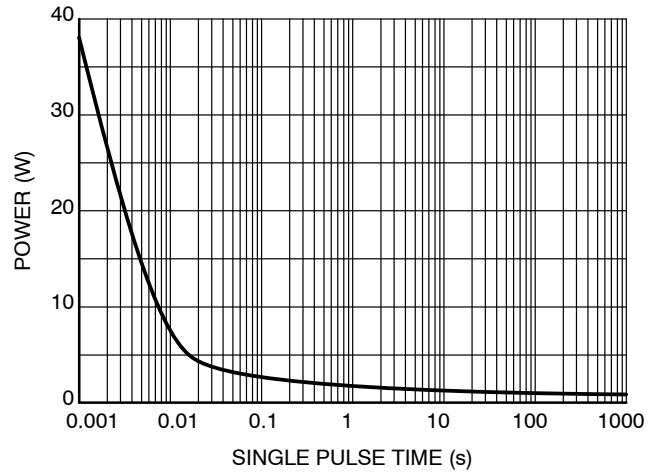


Figure 10. Single Pulse Maximum Power Dissipation

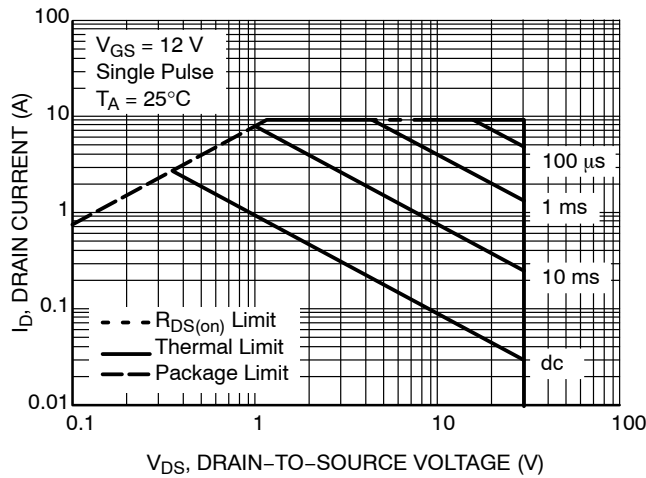


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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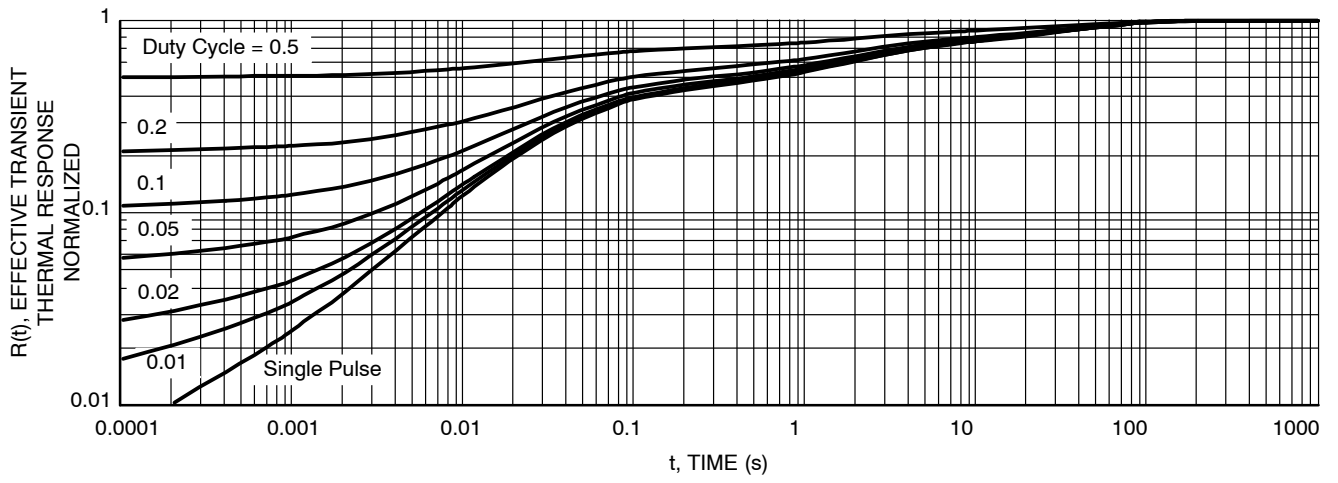


Figure 12. FET Thermal Response

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P-CHANNEL TYPICAL CHARACTERISTICS

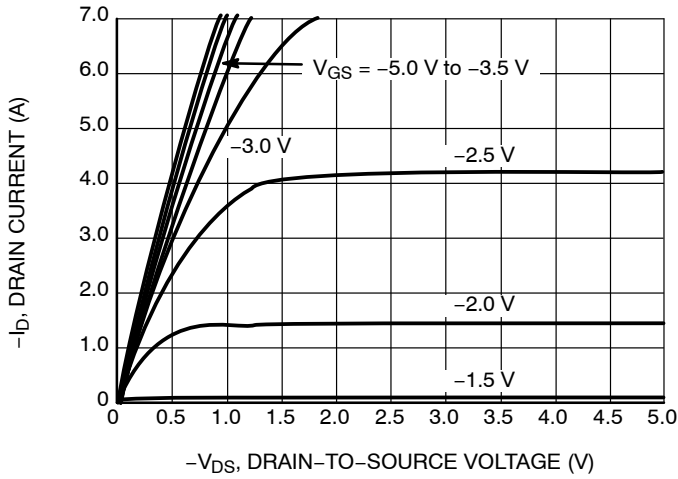


Figure 13. On-Region Characteristics

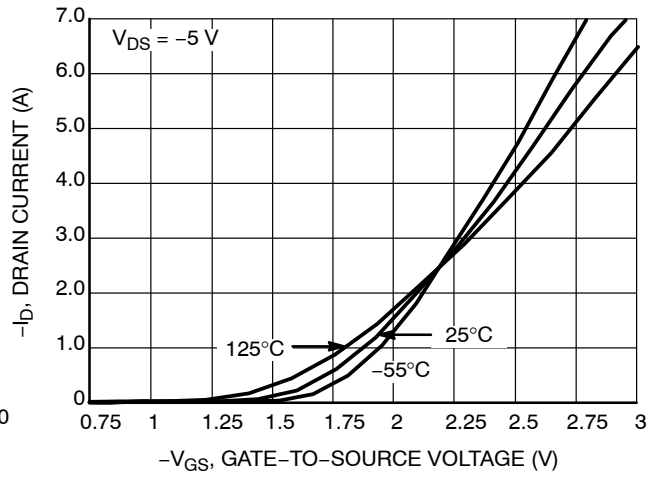


Figure 14. Transfer Characteristics

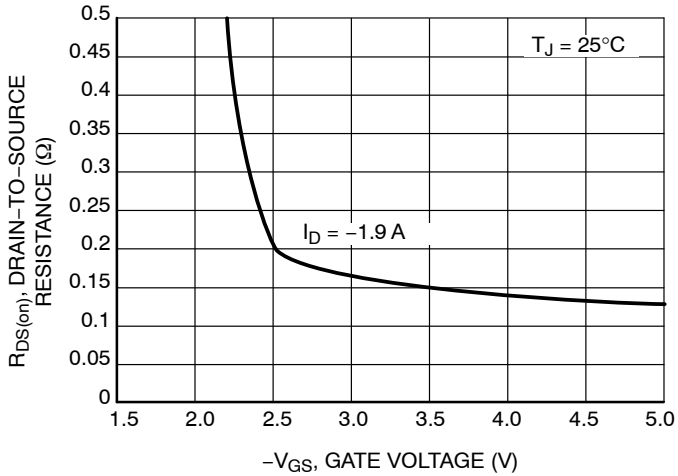


Figure 15. On-Region vs. Gate-To-Source Voltage

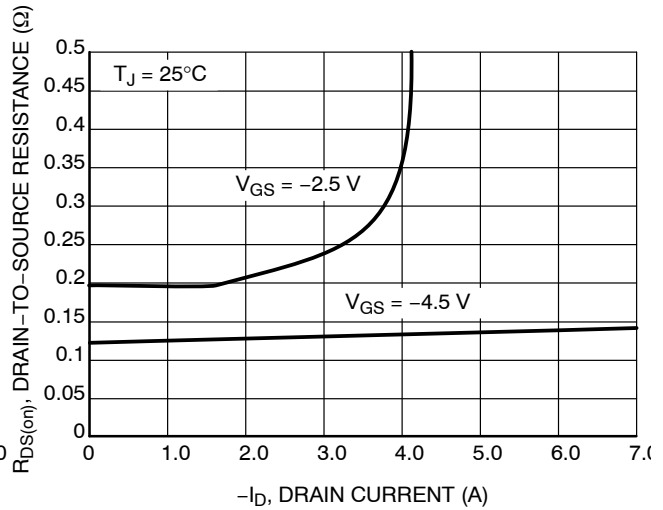


Figure 16. On-Resistance vs. Drain Current and Temperature

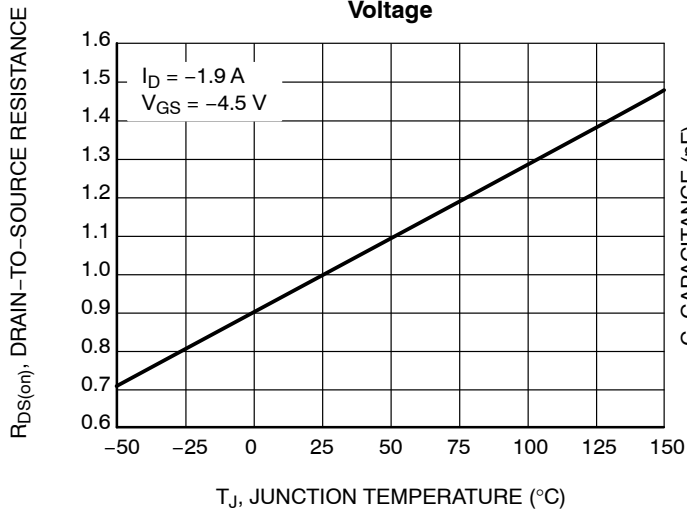


Figure 17. On-Resistance Variation with Temperature

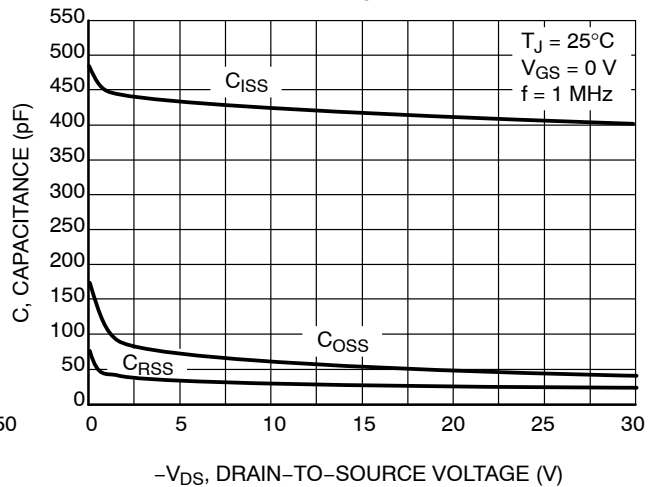


Figure 18. Capacitance Variation

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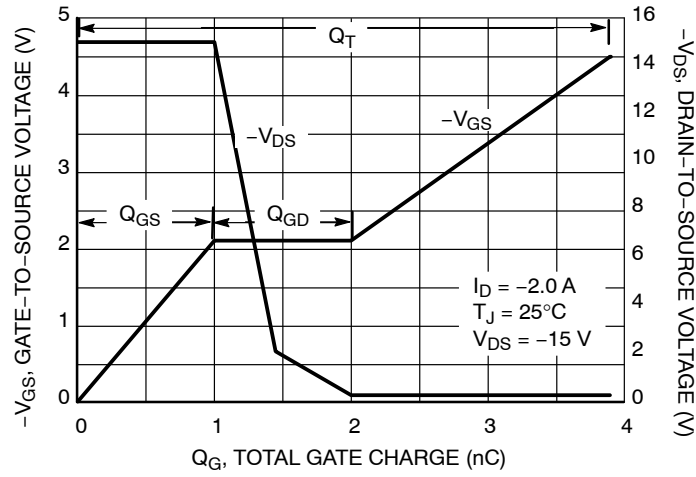


Figure 19. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

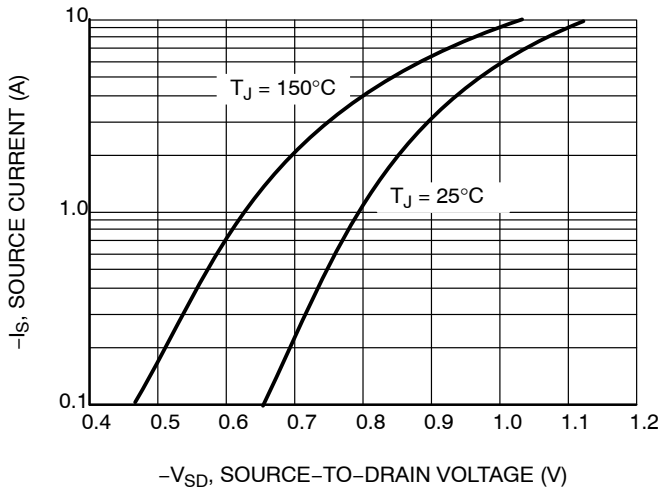


Figure 20. Diode Forward Voltage versus Current

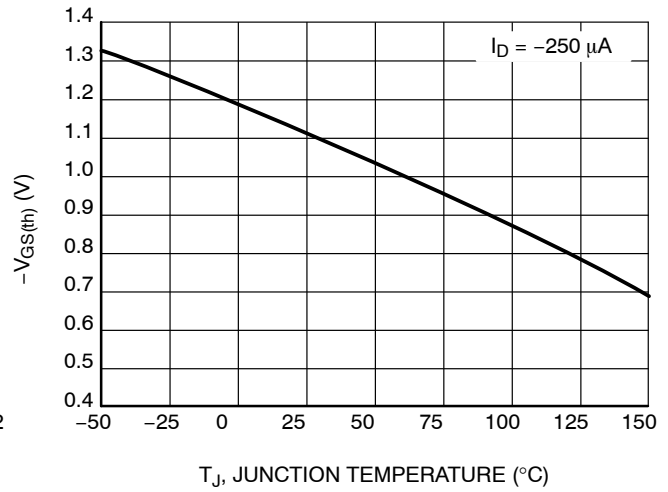


Figure 21. Threshold Voltage

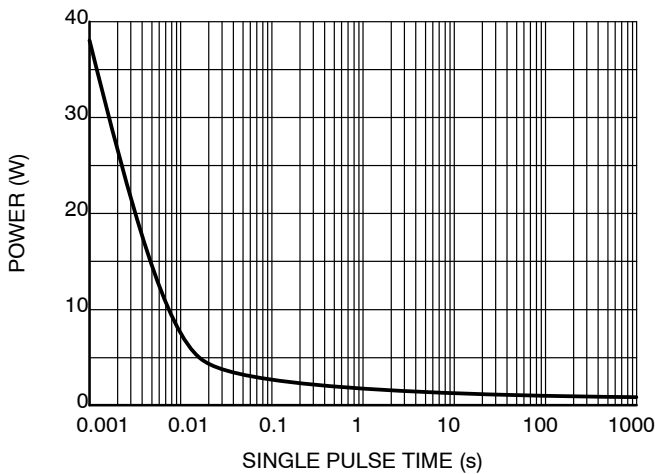


Figure 22. Single Pulse Maximum Power Dissipation

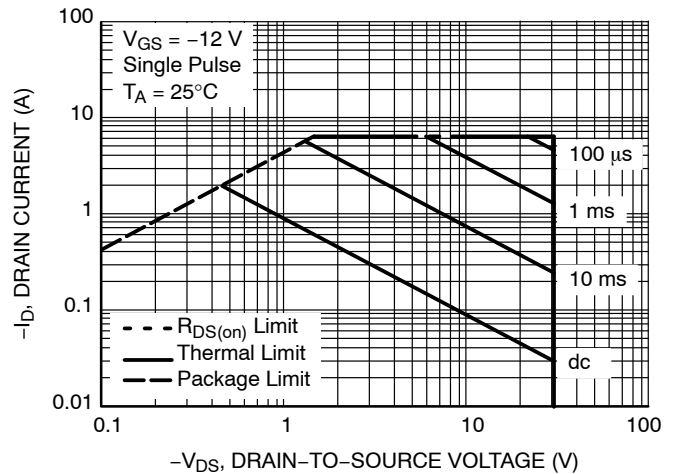


Figure 23. Maximum Rated Forward Biased Safe Operating Area

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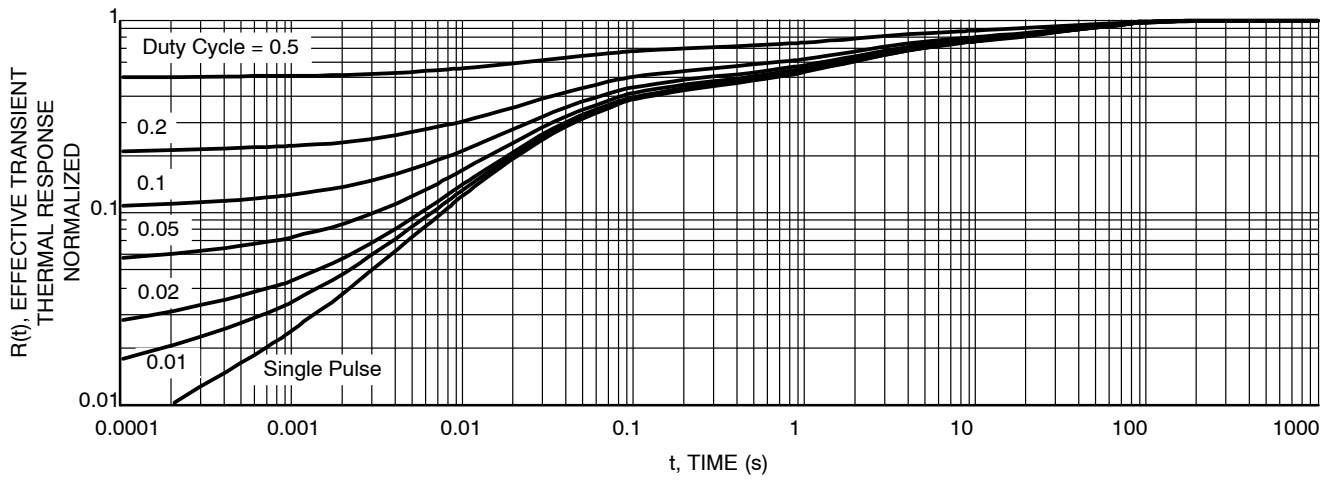


Figure 24. FET Thermal Response

ORDERING INFORMATION

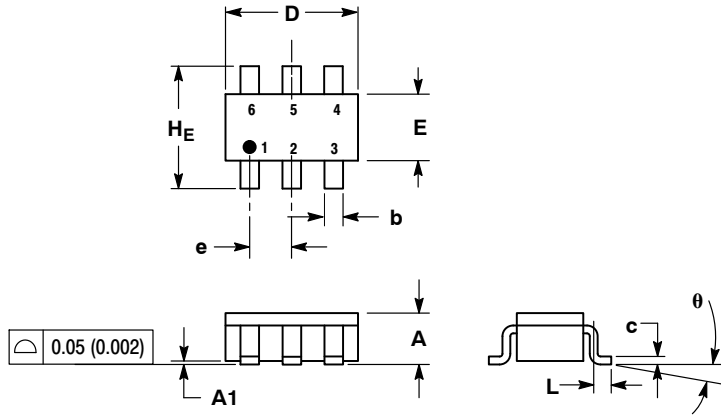
Device	Package	Shipping [†]
NTGD4167CT1G	TSOP6 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

TSOP-6
CASE 318G-02
ISSUE T



NOTES:

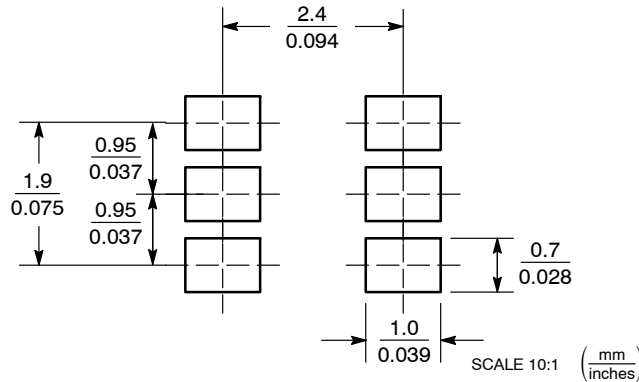
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	-	10°	0°	-	10°

STYLE 13:

- PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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