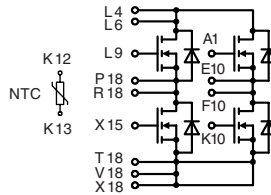


HiPerFET™ Power MOSFET

H-Bridge Topology in ECO-PAC 2

N-Channel Enhancement Mode
High dv/dt, Low t_{rr} , HDMOS™ Family

$I_{D25} = 75 \text{ A}$
 $V_{DSS} = 100 \text{ V}$
 $R_{DS(on)} = 25 \text{ m}\Omega$
 $t_{rr} \leq 200 \text{ ns}$



Pin arrangement see outlines

MOSFETs				
Symbol	Conditions	Maximum Ratings		
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	100	V	
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1 \text{ M}\Omega$	100	V	
V_{GS}	Continuous	± 20	V	
V_{GSM}	Transient	± 30	V	
I_{D25}	$T_C = 25^\circ\text{C}$	75	A	
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	300	A	
I_{AR}	$T_C = 25^\circ\text{C}$	75	A	
E_{AR}	$T_C = 25^\circ\text{C}$	30	mJ	
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$, $R_G = 2 \Omega$	5	V/ns	
P_D	$T_C = 25^\circ\text{C}$	300	W	
Symbol	Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
V_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	100		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 4 \text{ mA}$	2.0		V
I_{GSS}	$V_{GS} = \pm 20 V_{DC}$, $V_{DS} = 0$			$\pm 100 \text{ nA}$
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$; $T_J = 25^\circ\text{C}$ $V_{GS} = 0 \text{ V}$; $T_J = 125^\circ\text{C}$			250 μA 1 mA
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = 0.5 I_{D25}$ Pulse test, $t \leq 300 \mu\text{s}$, duty cycle $d \leq 2\%$			25 m Ω
g_{fs}	$V_{DS} = 10 \text{ V}$; $I_D = I_{D25}$, pulse test	25	30	S
C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$	4500		pF
C_{oss}		1600		pF
C_{rss}		800		pF
$t_{d(on)}$	$V_{GS} = 10 \text{ V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 I_{D25}$ $R_G = 2 \Omega$, (External)	20	30	ns
t_r		60	110	ns
$t_{d(off)}$		80	110	ns
t_f		60	90	ns
$Q_{g(on)}$	$V_{GS} = 10 \text{ V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 I_{D25}$	180	260	nC
Q_{gs}		36	70	nC
Q_{gd}		85	160	nC
R_{thJC}	with heatsink compound (0.42 K/m.K; 50 μm)	0.5		KW
R_{thCK}		0.25		KW

Features

- HiPerFET™ technology
 - low $R_{DS(on)}$
 - low gate charge for high frequency operation
 - unclamped inductive switching (UIS) capability
 - dv/dt ruggedness
 - fast intrinsic reverse diode
- ECO-PAC 2 package
 - isolated back surface
 - enlarged creepage towards heatsink
 - application friendly pinout
 - low inductive current path
 - high reliability
 - solderable pins for PCB mounting

Applications

- drives and power supplies
- battery or fuel cell powered
- automotive, industrial vehicle etc.
- secondary side of mains power supplies

IXYS reserves the right to change limits, test conditions and dimensions.

Source-Drain Diode

Symbol	Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
I_S	$V_{GS} = 0\text{ V}$			75 A
I_{SM}	Repetitive;			300 A
V_{SD}	$I_F = I_{D25}$, $V_{GS} = 0\text{ V}$, Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$			1.75 V
t_{rr}	$I_F = 25\text{ A}$, $-di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$ $V_R = 25\text{ V}$ $T_J = 125^\circ\text{C}$	300		200 ns ns

Temperature Sensor NTC

Symbol	Conditions	Characteristic Values		
		min.	typ.	max.
R_{25}	$T = 25^\circ\text{C}$	4.75	5.0	5.25 k Ω
$B_{25/50}$			3375	K

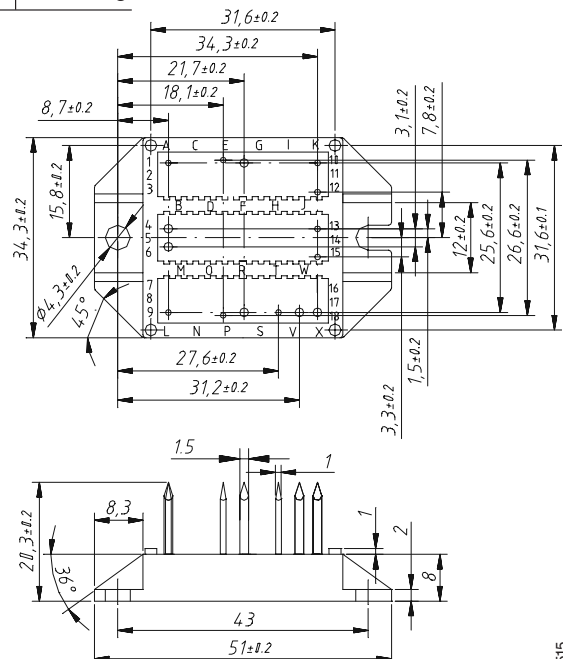
Module

Symbol	Conditions	Maximum Ratings	
T_{VJ}		-40...+150	$^\circ\text{C}$
T_{stg}		-40...+125	$^\circ\text{C}$
V_{ISOL}	$I_{ISOL} \leq 1\text{ mA}$; 50/60 Hz; $t = 1\text{ s}$	3600	V~
M_d	mounting torque (M4)	1.5 - 2.0 14 - 18	Nm lb.in.
a	Max. allowable acceleration	50	m/s^2

Symbol	Conditions	Characteristic Values		
		min.	typ.	max.
d_s	Creepage distance on surface (Pin to heatsink)	11.2		mm
d_A	Strike distance in air (Pin to heatsink)	11.2		mm
Weight		24		g

Data according to IEC 60747 refer to a single diode or transistor unless otherwise stated

Dimensions in mm (1 mm = 0.0394")



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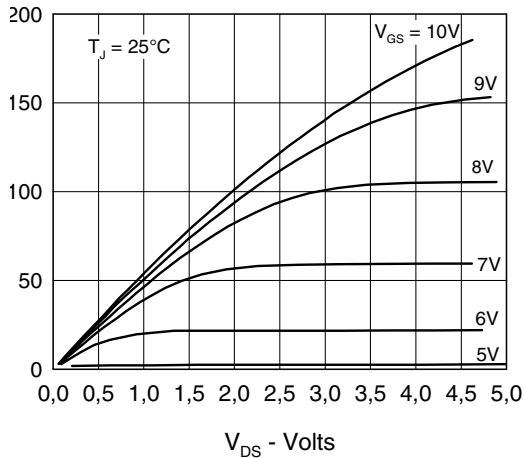


Fig. 1 Output Characteristics

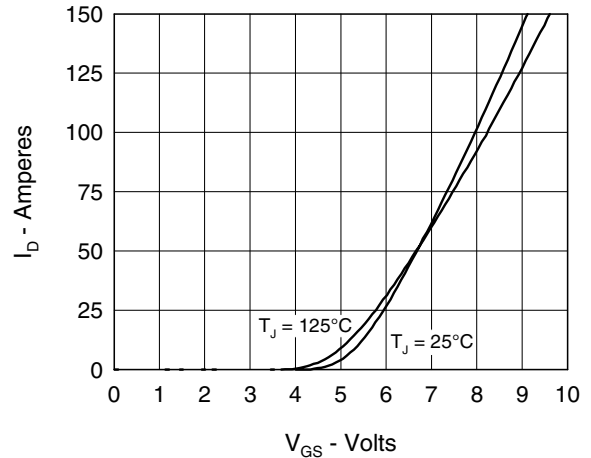


Fig. 2 Input Admittance

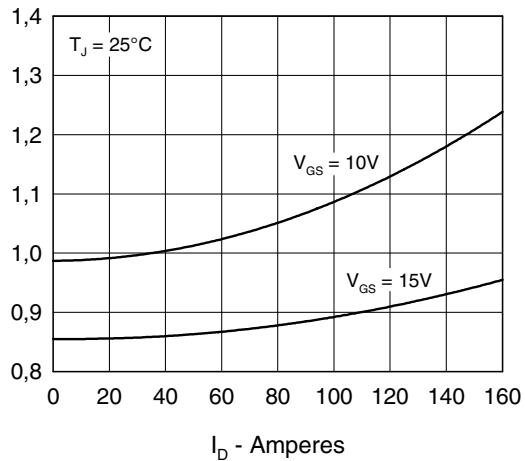


Fig. 3 $R_{DS(on)}$ vs. Drain Current

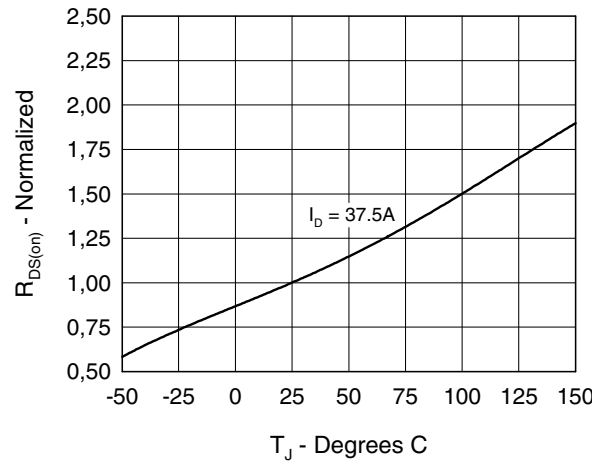


Fig. 4 Temperature Dependence of Drain to Source Resistance

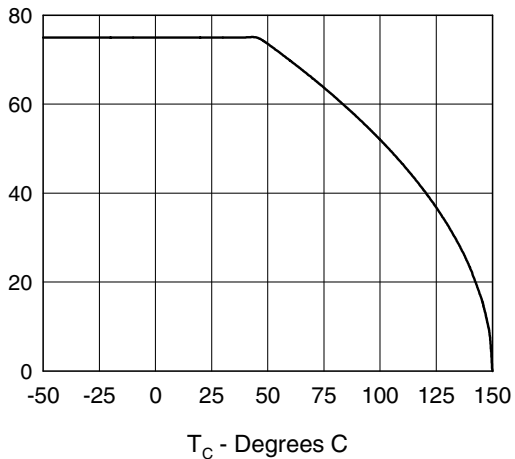


Fig. 5 Drain Current vs. Case Temperature

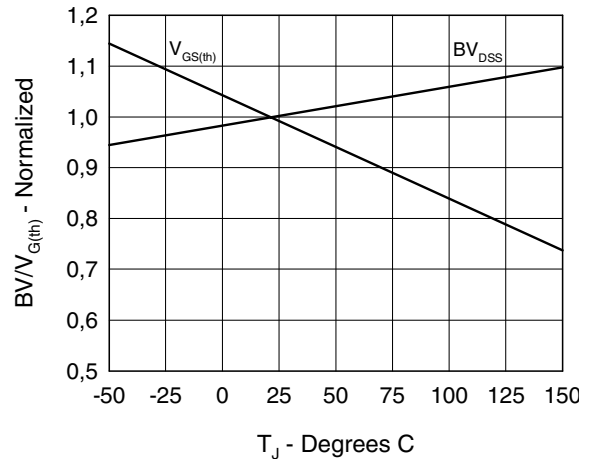


Fig. 6 Temperature Dependence of Breakdown and Threshold Voltage

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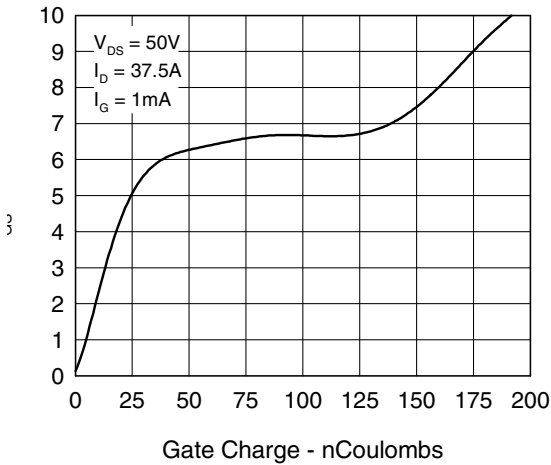


Fig.7 Gate Charge Characteristic Curve

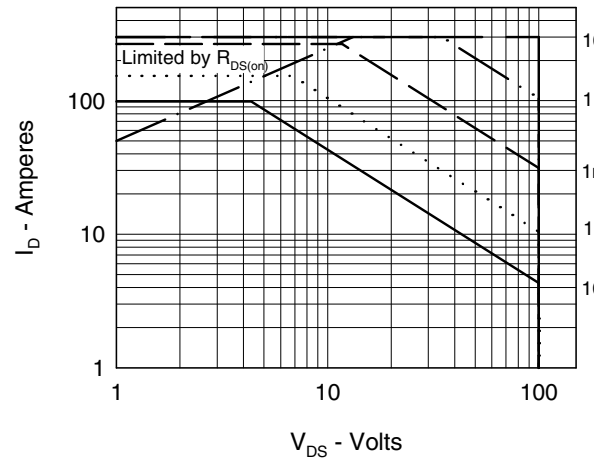


Fig.8 Forward Bias Safe Operating Area

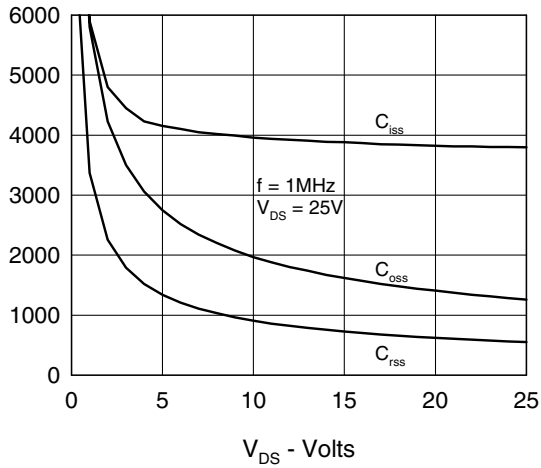


Fig.9 Capacitance Curves

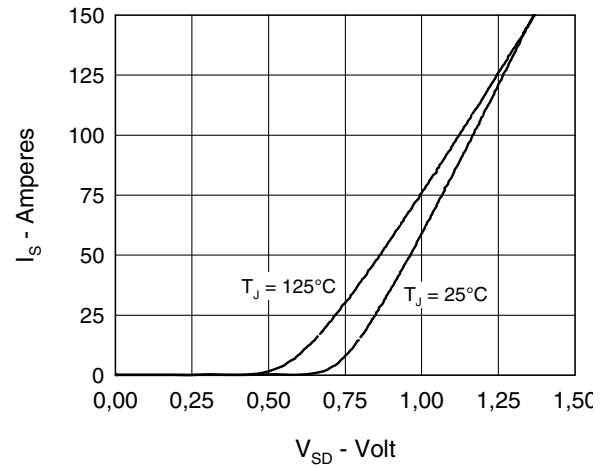


Fig.10 Source Current vs. Source to Drain Voltage

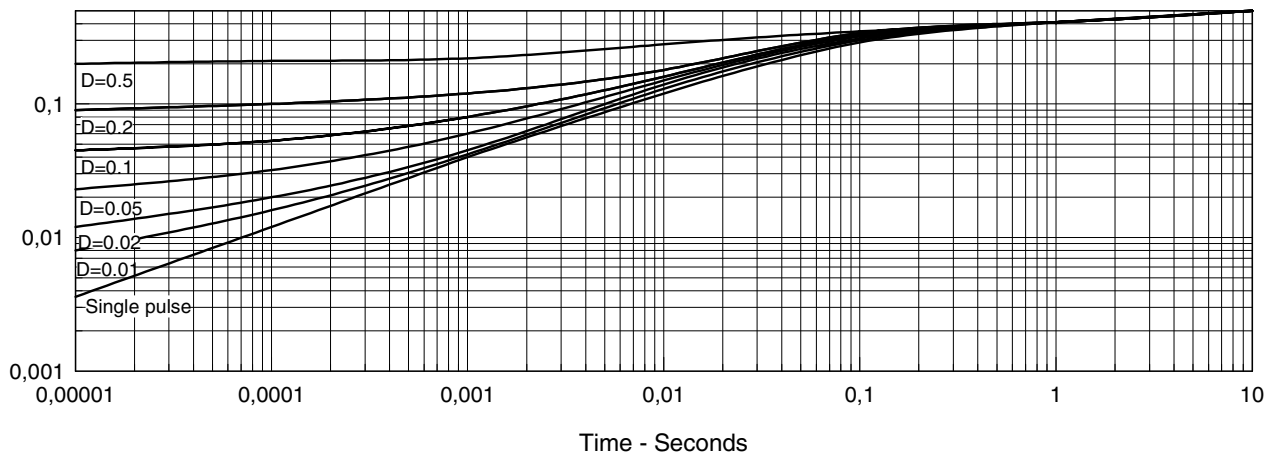


Fig.11 Transient Thermal Impedance