

AO4612

60V Complementary Enhancement Mode Field Effect Transistor

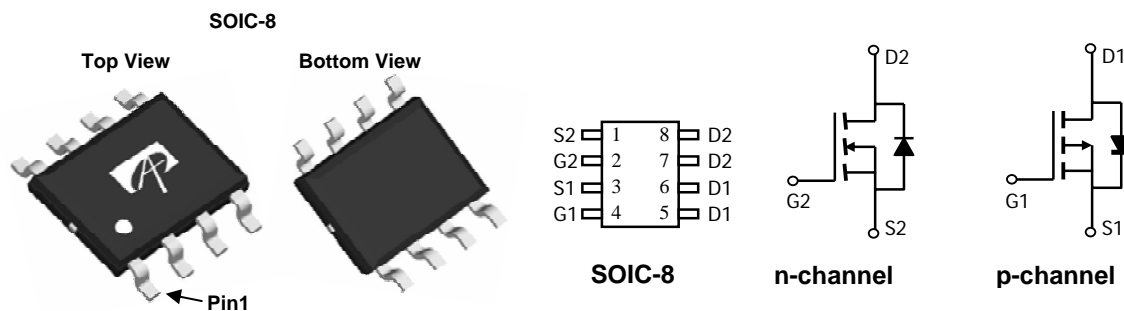
General Description

The AO4612 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.

Features

n-channel	p-channel
V_{DS} (V) = 60V	-60V
I_D = 4.5A ($V_{GS}=10V$)	-3.2A ($V_{GS} = -10V$)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 56m Ω ($V_{GS}=10V$)	< 105m Ω ($V_{GS} = -10V$)
< 77m Ω ($V_{GS}=4.5V$)	< 135m Ω ($V_{GS} = -4.5V$)

100% Rg tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	60	-60	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current ^A	I_D	$T_A=25^\circ\text{C}$	4.5	-3.2
		$T_A=70^\circ\text{C}$	3.6	-2.6
Pulsed Drain Current ^B	I_{DM}	20	-20	A
Power Dissipation	P_D	$T_A=25^\circ\text{C}$	2	2
		$T_A=70^\circ\text{C}$	1.28	1.28
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	-55 to 150	$^\circ\text{C}$

Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A $t \leq 10\text{s}$	$R_{\theta JA}$	48	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A Steady-State		74	90	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C Steady-State	$R_{\theta JL}$	35	40	$^\circ\text{C/W}$

N Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =48V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1	2.1	3	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	20			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =4.5A T _J =125°C		46 79	56	mΩ
		V _{GS} =4.5V, I _D =3A		64	77	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =4.5A		11		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.74	1	V
I _S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =30V, f=1MHz		450	540	pF
C _{oss}	Output Capacitance			60		pF
C _{rss}	Reverse Transfer Capacitance			25		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		1.65	2	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =30V, I _D =4.5A		8.5	10.5	nC
Q _g (4.5V)	Total Gate Charge			4.3	5.5	nC
Q _{gs}	Gate Source Charge			1.6		nC
Q _{gd}	Gate Drain Charge			2.2		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =30V, R _L =6.7Ω, R _{GEN} =3Ω		4.7	7	ns
t _r	Turn-On Rise Time			2.3	4.5	ns
t _{D(off)}	Turn-Off DelayTime			15.7	24	ns
t _f	Turn-Off Fall Time			1.9	4	ns
t _{rr}	Body Diode Reverse Recovery Time		I _F =4.5A, dI/dt=100A/μs		27.5	35
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =4.5A, dI/dt=100A/μs		32		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any a given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The SOA curve provides a single pulse rating. Rev3: Oct 2010

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CANNEL

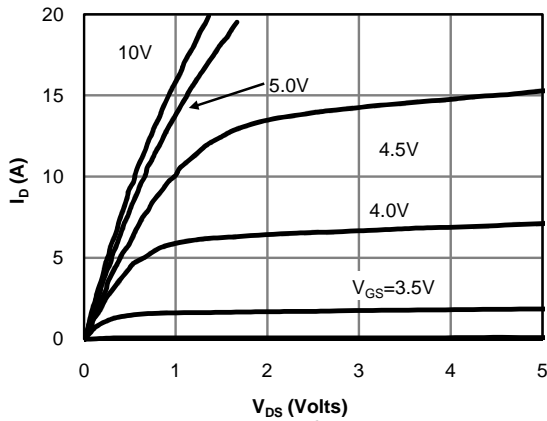


Fig 1: On-Region Characteristics

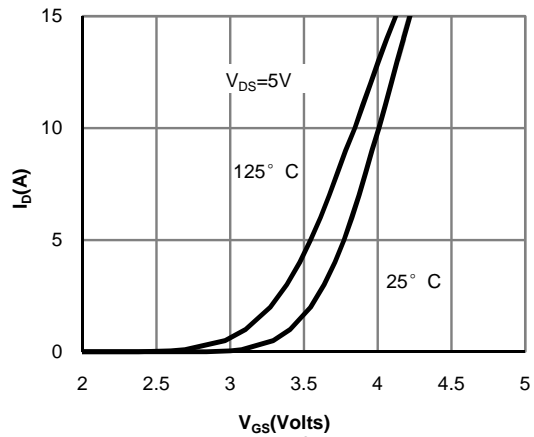


Figure 2: Transfer Characteristics

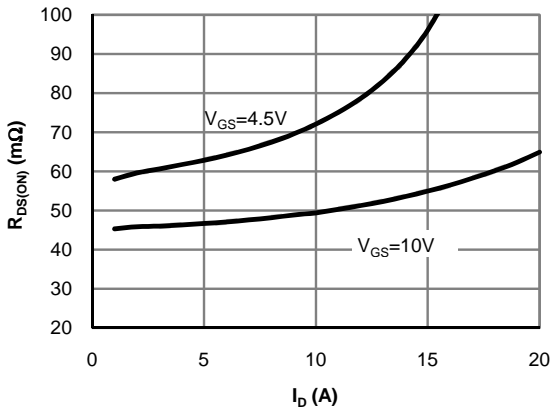


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

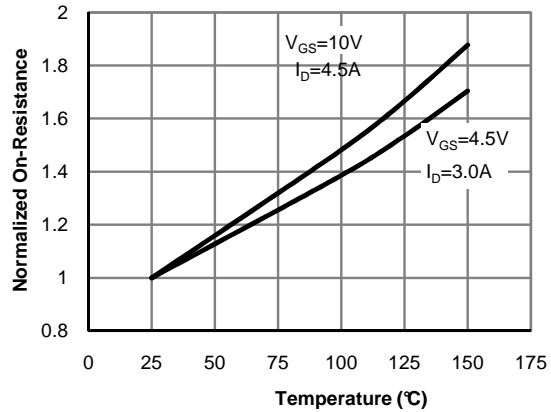


Figure 4: On-Resistance vs. Junction Temperature

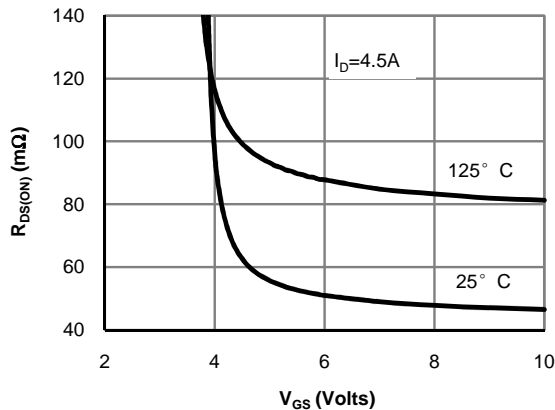


Figure 5: On-Resistance vs. Gate-Source Voltage

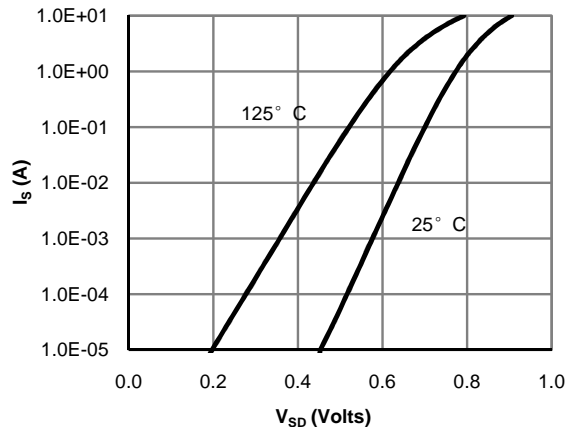


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CANNEL

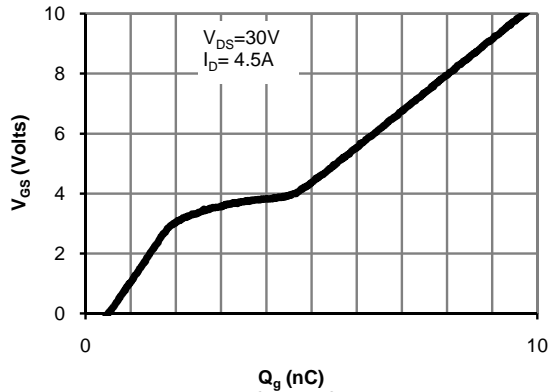


Figure 7: Gate-Charge Characteristics

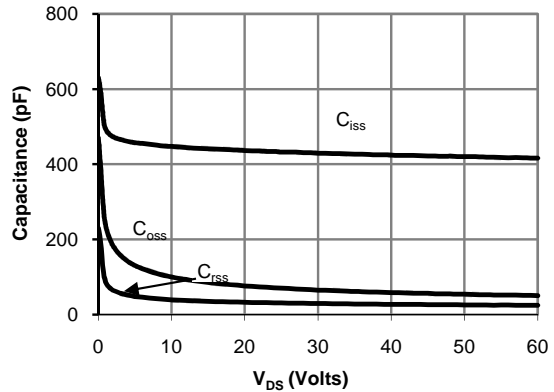


Figure 8: Capacitance Characteristics

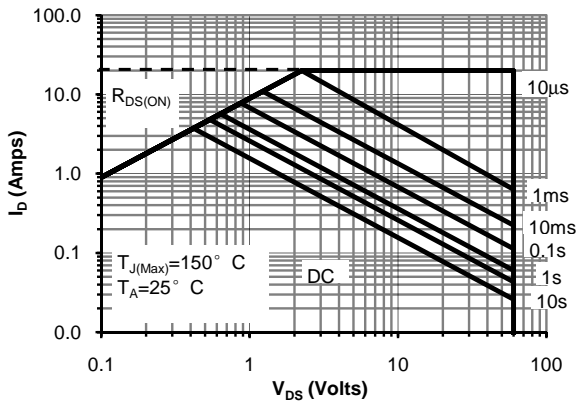


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

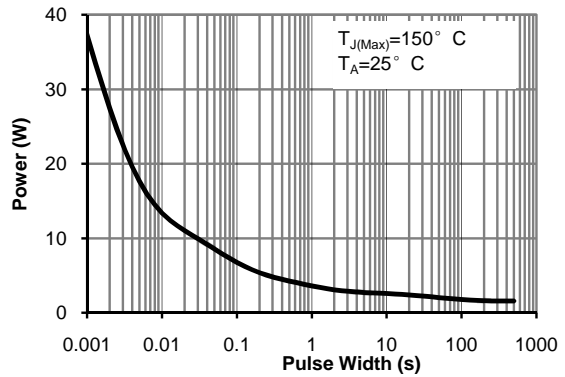


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

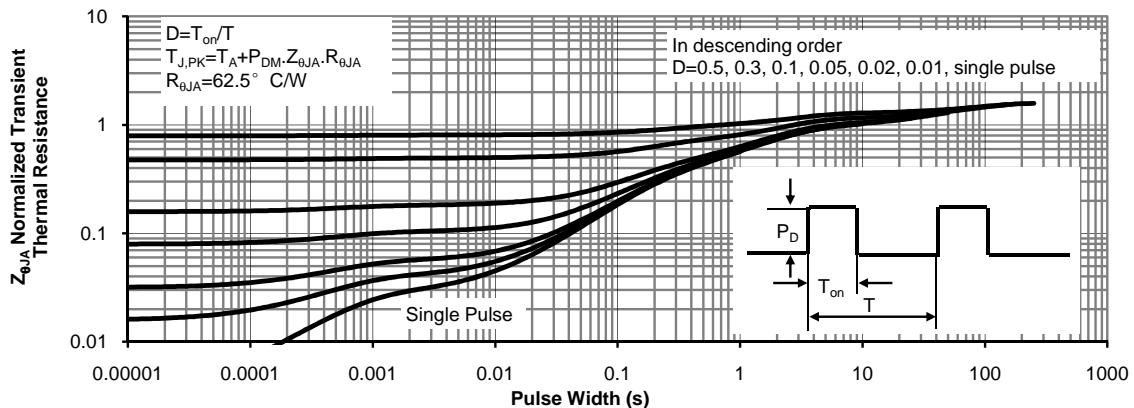
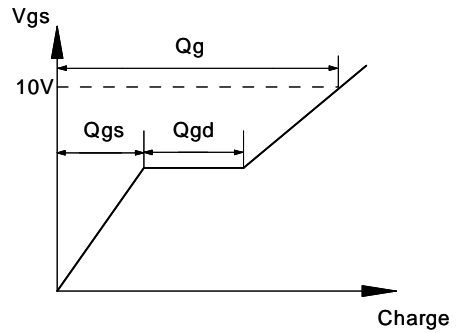
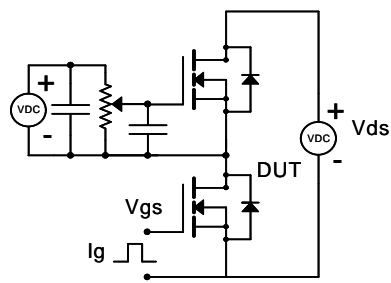
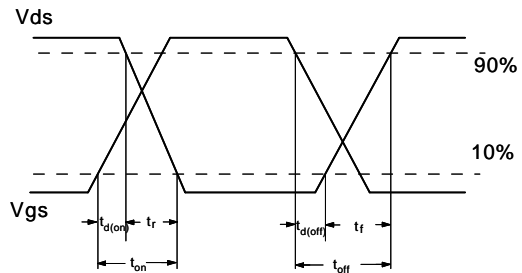
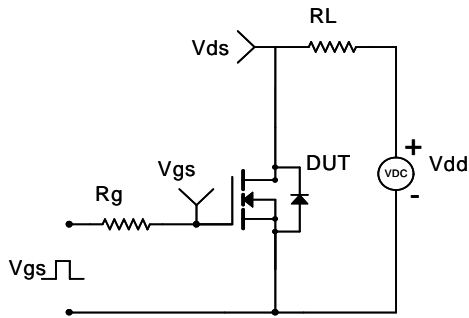


Figure 11: Normalized Maximum Transient Thermal Impedance

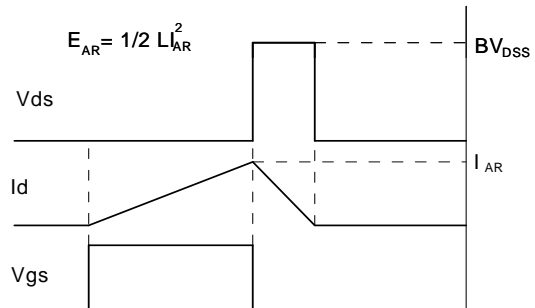
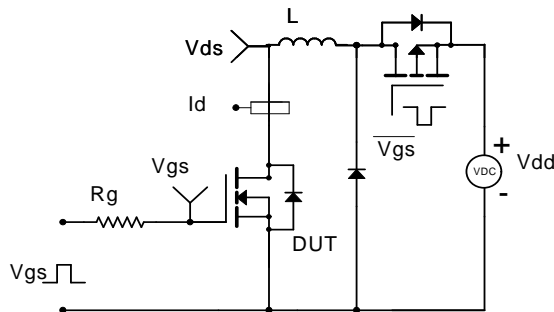
Gate Charge Test Circuit & Waveform



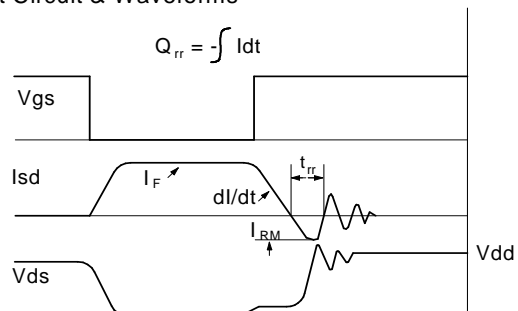
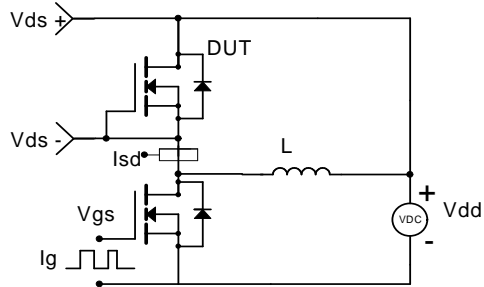
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-60			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-48\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1 -5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1	-2.1	-3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}$, $V_{DS}=-5\text{V}$	-20			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}$, $I_D=-3.2\text{A}$ $T_J=125^\circ\text{C}$		84	105	m Ω
		$V_{GS}=-4.5\text{V}$, $I_D=-2.8\text{A}$		106	135	
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-3.2\text{A}$		9		S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}$, $V_{GS}=0\text{V}$		-0.73	-1	V
I_S	Maximum Body-Diode Continuous Current				-3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=-30\text{V}$, $f=1\text{MHz}$		930	1120	pF
C_{oss}	Output Capacitance			85		pF
C_{rss}	Reverse Transfer Capacitance			35		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		7.2	9	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge (10V)	$V_{GS}=-10\text{V}$, $V_{DS}=-30\text{V}$, $I_D=-3.2\text{A}$		16	20	nC
$Q_g(4.5\text{V})$	Total Gate Charge (4.5V)			8	10	nC
Q_{gs}	Gate Source Charge			2.5		nC
Q_{gd}	Gate Drain Charge			3.2		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=-10\text{V}$, $V_{DS}=-30\text{V}$, $R_L=9.4\Omega$, $R_{GEN}=3\Omega$		8	12	ns
t_r	Turn-On Rise Time			3.8	7.5	ns
$t_{D(off)}$	Turn-Off DelayTime			31.5	48	ns
t_f	Turn-Off Fall Time			7.5	15	ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-3.2\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		27	35	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-3.2\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		32		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any a given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D: The static characteristics in Figures 1 to 6, 12, 14 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

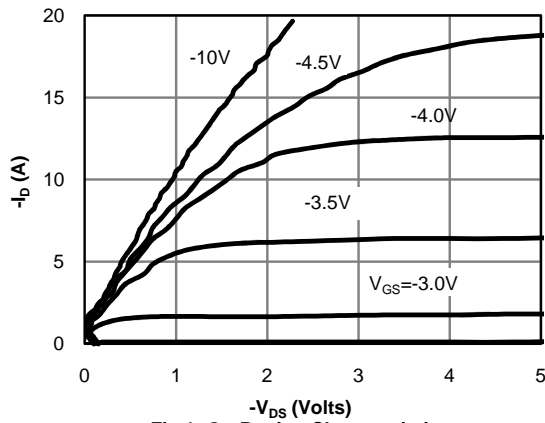


Fig 1: On-Region Characteristics

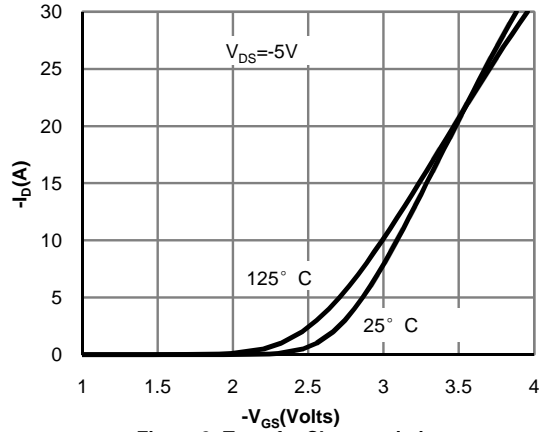


Figure 2: Transfer Characteristics

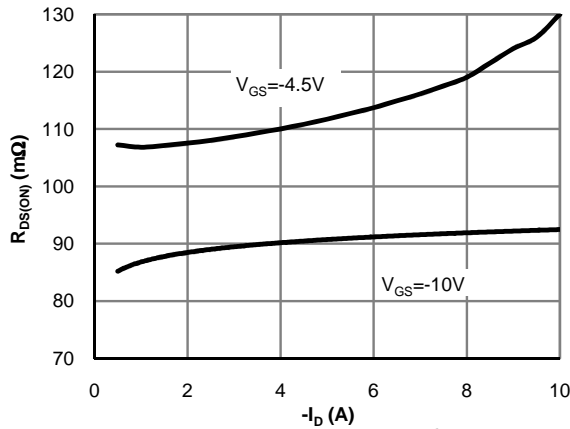


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

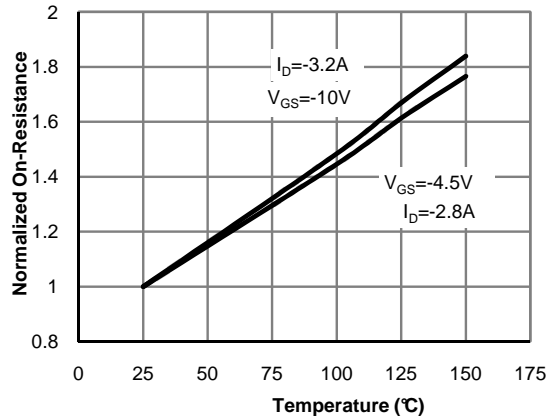


Figure 4: On-Resistance vs. Junction Temperature

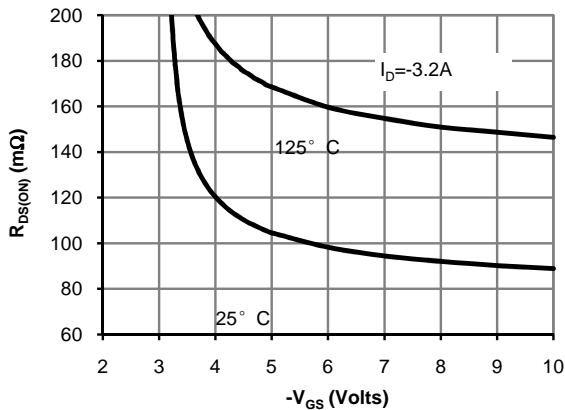


Figure 5: On-Resistance vs. Gate-Source Voltage

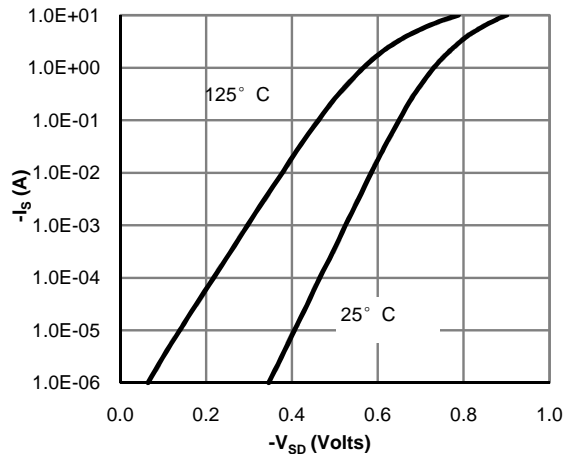


Figure 6: Body-Diode Characteristics

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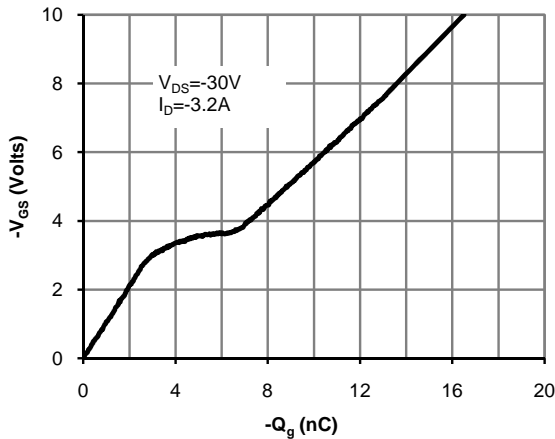


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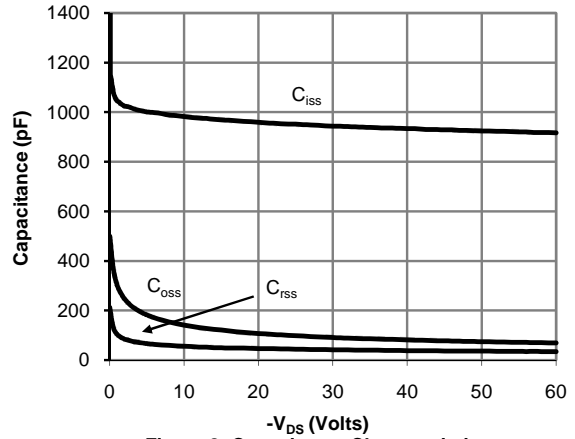


Figure 8: Capacitance Characteristics

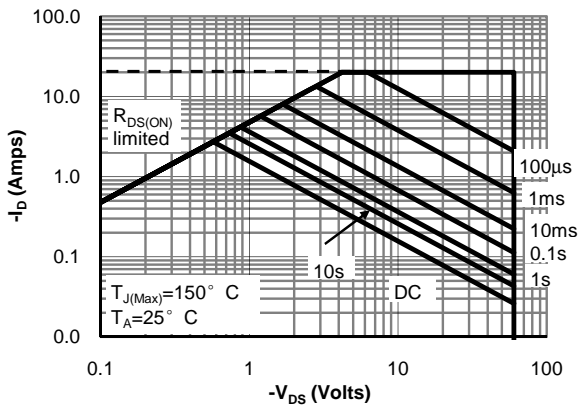


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

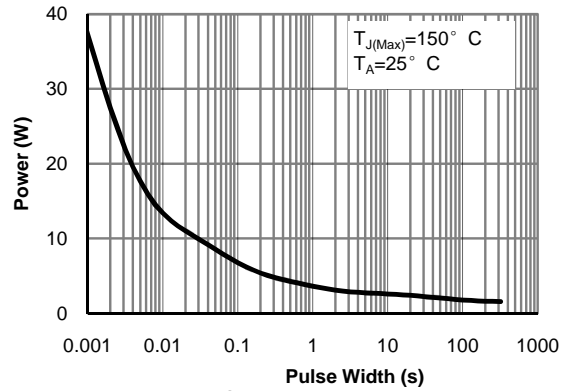


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

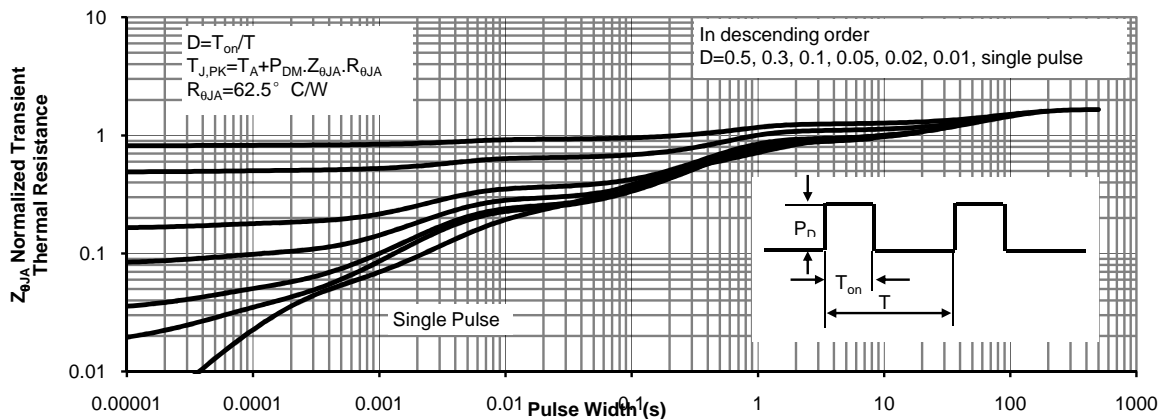
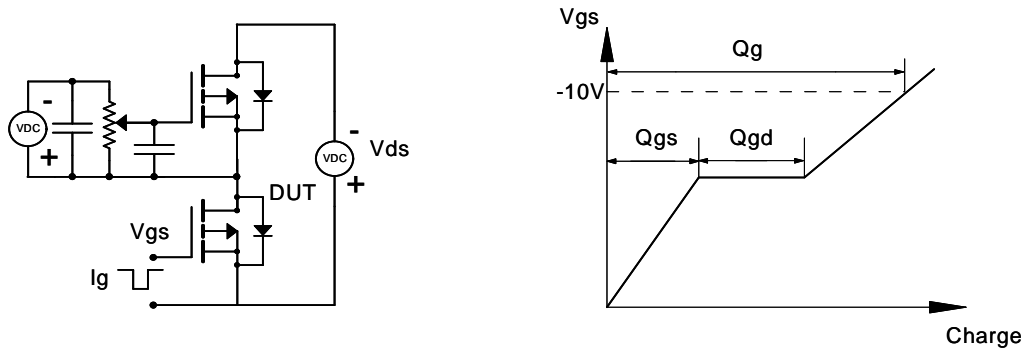
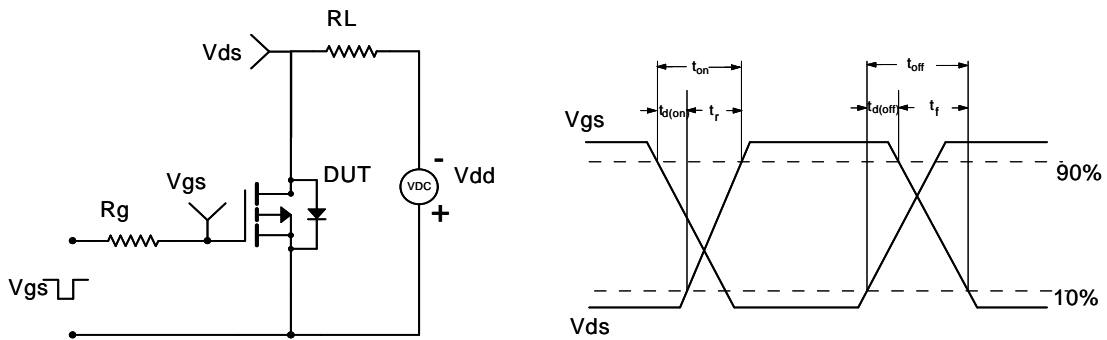


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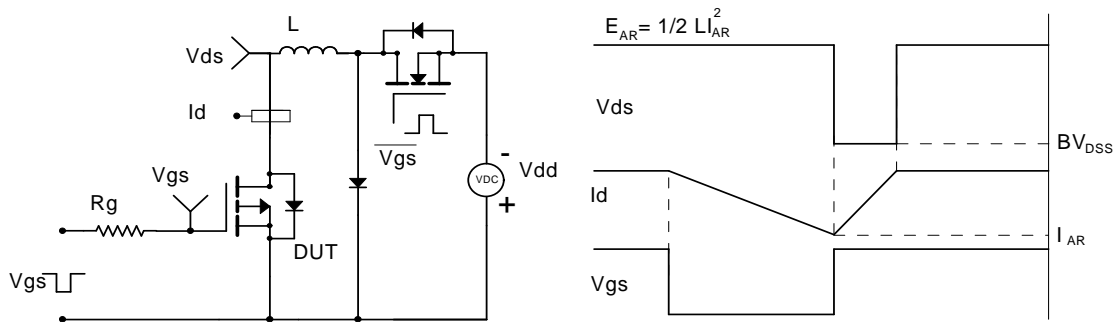
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

