

# IRF7307QPbF

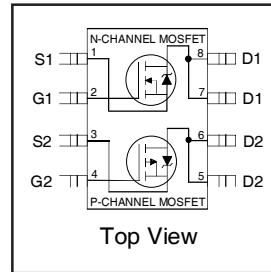
HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dual N and P Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- 150°C Operating Temperature
- Lead-Free

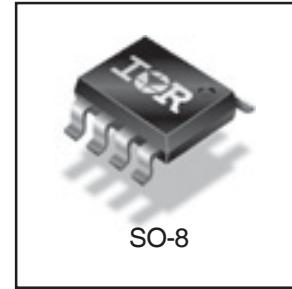
## Description

These HEXFET® Power MOSFET's in a Dual SO-8 package utilize the lastest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of these HEXFET Power MOSFET's are a 150°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.

The efficient SO-8 package provides enhanced thermal characteristics and dual MOSFET die capability making it ideal in a variety of power applications. This dual, surface mount SO-8 can dramatically reduce board space and is also available in Tape & Reel.



	N-Ch	P-Ch
V <sub>DSS</sub>	20V	-20V
R <sub>DS(on)</sub>	0.050Ω	0.090Ω



## Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
I <sub>D</sub> @ T <sub>A</sub> = 25°C	10 Sec. Pulse Drain Current, V <sub>GS</sub> @ 4.5V	5.7	-4.7	A
I <sub>D</sub> @ T <sub>A</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 4.5V	5.2	-4.3	
I <sub>D</sub> @ T <sub>A</sub> = 70°C	Continuous Drain Current, V <sub>GS</sub> @ 4.5V	4.1	-3.4	
I <sub>DM</sub>	Pulsed Drain Current ①	21	-17	
P <sub>D</sub> @T <sub>A</sub> = 25°C	Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 12		V
dV/dt	Peak Diode Recovery dV/dt ②	5.0	-5.0	V/ns
T <sub>J</sub> , T <sub>STG</sub>	Junction and Storage Temperature Range	-55 to + 150		°C

## Thermal Resistance Ratings

	Parameter	Typ.	Max.	Units
R <sub>θJA</sub>	Maximum Junction-to-Ambient④	—	62.5	°C/W

# IRF7307QPbF

International  
Rectifier

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

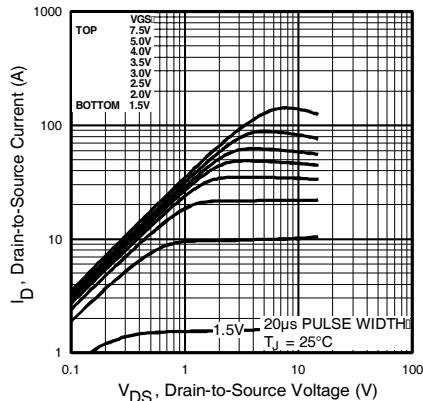
	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	N-Ch	20	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
		P-Ch	-20	—	—		$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.044	—	$^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
		P-Ch	—	-0.012	—		Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{DS(\text{ON})}$	Static Drain-to-Source On-Resistance	N-Ch	—	—	0.050	$\Omega$	$V_{GS} = 4.5\text{V}, I_D = 2.6\text{A}$ ③
		N-Ch	—	—	0.070		$V_{GS} = 2.7\text{V}, I_D = 2.2\text{A}$ ③
		P-Ch	—	—	0.090		$V_{GS} = -4.5\text{V}, I_D = -2.2\text{A}$ ③
		P-Ch	—	—	0.140		$V_{GS} = -2.7\text{V}, I_D = -1.8\text{A}$ ③
$V_{GS(\text{th})}$	Gate Threshold Voltage	N-Ch	0.70	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
		P-Ch	-0.70	—	—		$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
$g_{fs}$	Forward Transconductance	N-Ch	8.30	—	—	S	$V_{DS} = 15\text{V}, I_D = 2.6\text{A}$ ③
		P-Ch	4.00	—	—		$V_{DS} = -15\text{V}, I_D = -2.2\text{A}$ ③
$I_{DSS}$	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	$\mu\text{A}$	$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}$
		P-Ch	—	—	-1.0		$V_{DS} = -16\text{V}, V_{GS} = 0\text{V}$
		N-Ch	—	—	25		$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
		P-Ch	—	—	-25		$V_{DS} = -16\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	N-P	—	—	$\pm 100$		$V_{GS} = \pm 12\text{V}$
$Q_g$	Total Gate Charge	N-Ch	—	—	20	$\text{nC}$	N-Channel $I_D = 2.6\text{A}, V_{DS} = 16\text{V}, V_{GS} = 4.5\text{V}$
		P-Ch	—	—	22		③
$Q_{gs}$	Gate-to-Source Charge	N-Ch	—	—	2.2		P-Channel
		P-Ch	—	—	3.3		$I_D = -2.2\text{A}, V_{DS} = -16\text{V}, V_{GS} = -4.5\text{V}$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	N-Ch	—	—	8.0		
		P-Ch	—	—	9.0		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	9.0	—		N-Channel
		P-Ch	—	8.4	—		$V_{DD} = 10\text{V}, I_D = 2.6\text{A}, R_G = 6.0\Omega, R_D = 3.8\Omega$
$t_r$	Rise Time	N-Ch	—	42	—		③
		P-Ch	—	26	—		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	32	—		P-Channel
		P-Ch	—	51	—		$V_{DD} = -10\text{V}, I_D = -2.2\text{A}, R_G = 6.0\Omega, R_D = 4.5\Omega$
$t_f$	Fall Time	N-Ch	—	51	—		
		P-Ch	—	33	—		
$L_D$	Internal Drain Inductance	N-P	—	4.0	—	$\text{nH}$	Between lead tip and center of die contact
$L_S$	Internal Source Inductance	N-P	—	6.0	—		
$C_{iss}$	Input Capacitance	N-Ch	—	660	—	$\text{pF}$	N-Channel
		P-Ch	—	610	—		$V_{GS} = 0\text{V}, V_{DS} = 15\text{V}, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	N-Ch	—	280	—		③
		P-Ch	—	310	—		P-Channel
$C_{rss}$	Reverse Transfer Capacitance	N-Ch	—	140	—		$V_{GS} = 0\text{V}, V_{DS} = -15\text{V}, f = 1.0\text{MHz}$
		P-Ch	—	170	—		

## Source-Drain Ratings and Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	N-Ch	—	—	2.5	$\text{A}$	
		P-Ch	—	—	-2.5		
$I_{SM}$	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	21		
		P-Ch	—	—	-17		
$V_{SD}$	Diode Forward Voltage	N-Ch	—	—	1.0	$\text{V}$	$T_J = 25^\circ\text{C}, I_S = 1.8\text{A}, V_{GS} = 0\text{V}$ ③
		P-Ch	—	—	-1.0		$T_J = 25^\circ\text{C}, I_S = -1.8\text{A}, V_{GS} = 0\text{V}$ ③
$t_{rr}$	Reverse Recovery Time	N-Ch	—	29	44	$\text{ns}$	N-Channel
		P-Ch	—	56	84		$T_J = 25^\circ\text{C}, I_F = 2.6\text{A}, di/dt = 100\text{A}/\mu\text{s}$
$Q_{rr}$	Reverse Recovery Charge	N-Ch	—	22	33	$\text{nC}$	P-Channel
		P-Ch	—	71	110		$T_J = 25^\circ\text{C}, I_F = -2.2\text{A}, di/dt = 100\text{A}/\mu\text{s}$
$t_{on}$	Forward Turn-On Time	N-P	Intrinsic turn-on time is neglegible (turn-on is dominated by $L_S + L_D$ )				

### Notes:

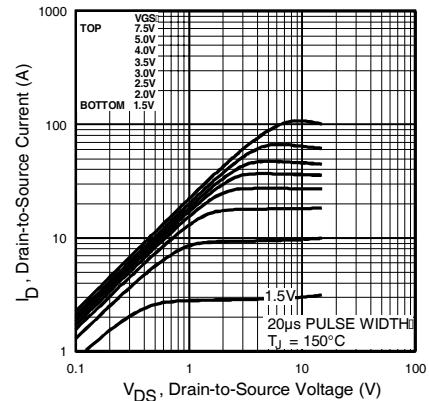
- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 23 )
- ② N-Channel  $I_{SD} \leq 2.6\text{A}$ ,  $di/dt \leq 100\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(\text{BR})\text{DSS}}$ ,  $T_J \leq 150^\circ\text{C}$   
P-Channel  $I_{SD} \leq -2.2\text{A}$ ,  $di/dt \leq 50\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(\text{BR})\text{DSS}}$ ,  $T_J \leq 150^\circ\text{C}$
- ③ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④ Surface mounted on FR-4 board,  $t \leq 10\text{sec}$ .



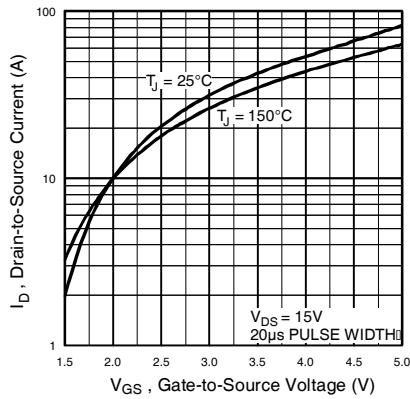
**Fig 1.** Typical Output Characteristics

N-Channel

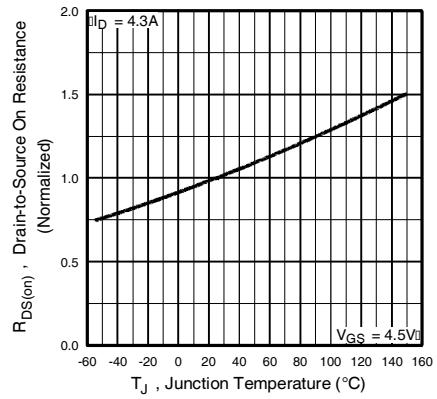
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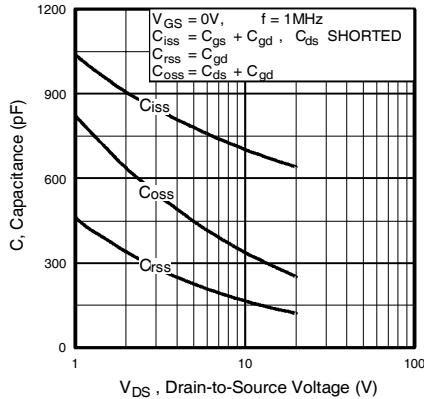
**Fig 2.** Typical Output Characteristics



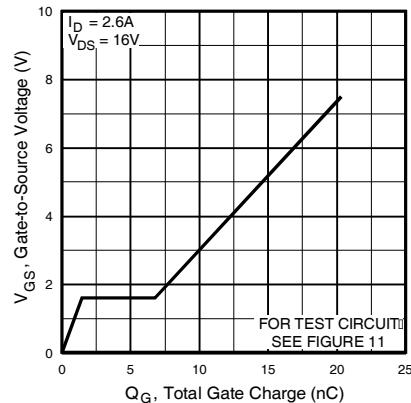
**Fig 3.** Typical Transfer Characteristics



**Fig 4.** Normalized On-Resistance Vs. Temperature



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

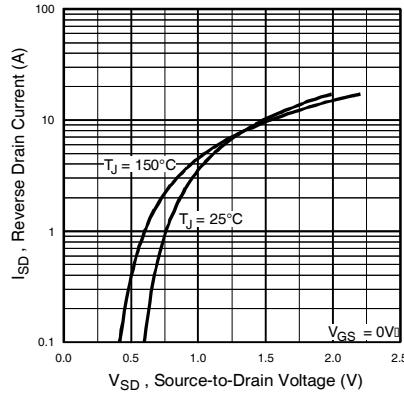


**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

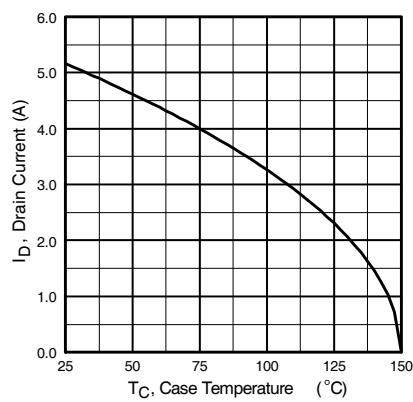
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N-Channel

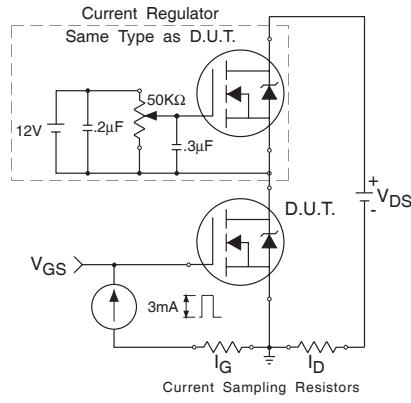
International  
Rectifier



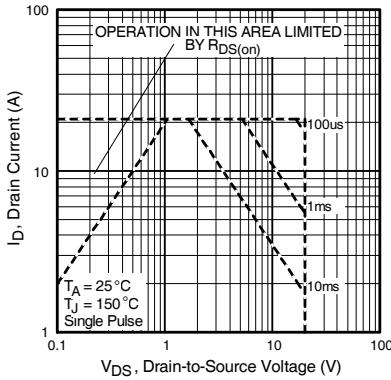
**Fig 7.** Typical Source-Drain Diode Forward Voltage



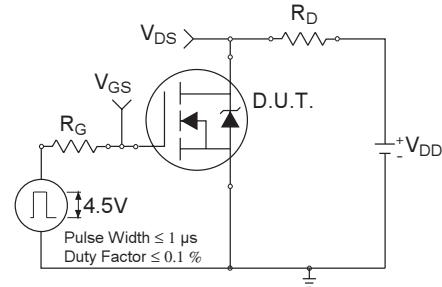
**Fig 9.** Maximum Drain Current Vs. Ambient Temperature



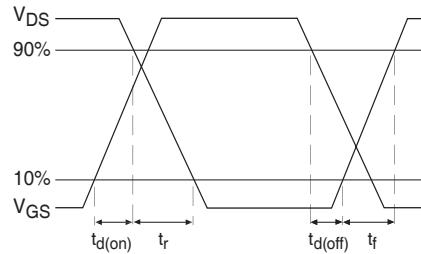
**Fig 11a.** Gate Charge Test Circuit  
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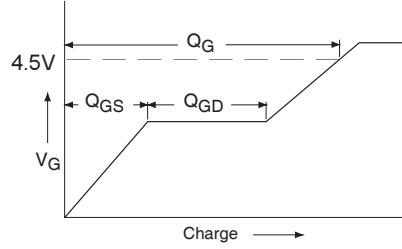
**Fig 8.** Maximum Safe Operating Area



**Fig 10a.** Switching Time Test Circuit

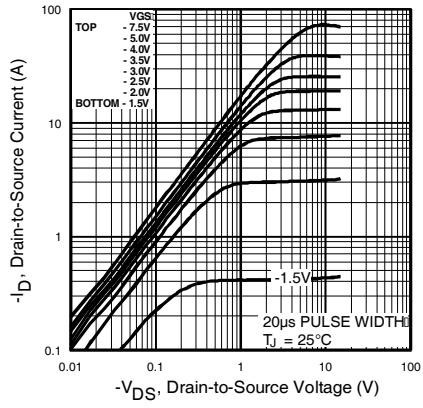


**Fig 10b.** Switching Time Waveforms



**Fig 11b.** Basic Gate Charge Waveform

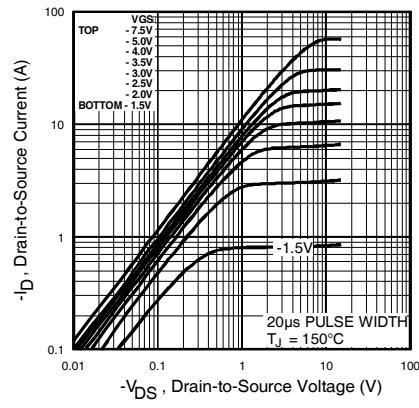
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**IR** Rectifier



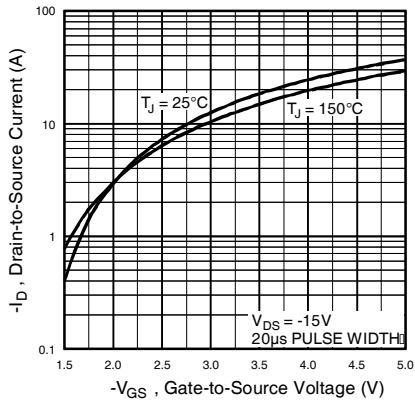
**Fig 12.** Typical Output Characteristics

P-Channel

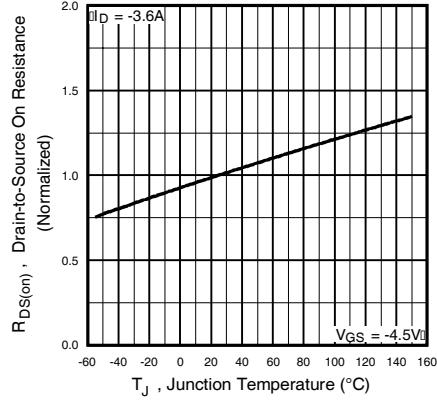
**IRF7307QPBf**



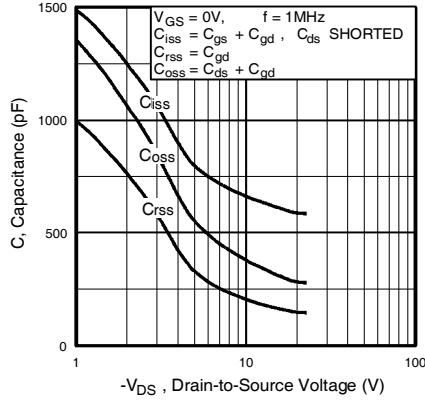
**Fig 13.** Typical Output Characteristics



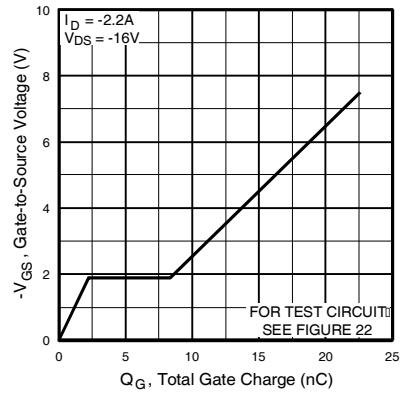
**Fig 14.** Typical Transfer Characteristics



**Fig 15.** Normalized On-Resistance Vs. Temperature



**Fig 16.** Typical Capacitance Vs. Drain-to-Source Voltage

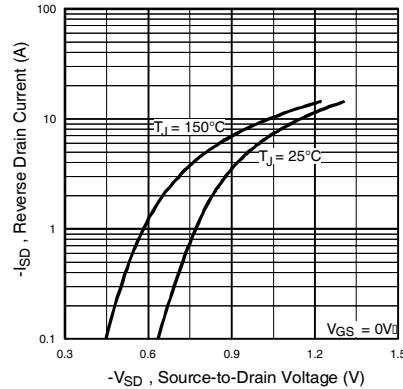


**Fig 17.** Typical Gate Charge Vs. Gate-to-Source Voltage

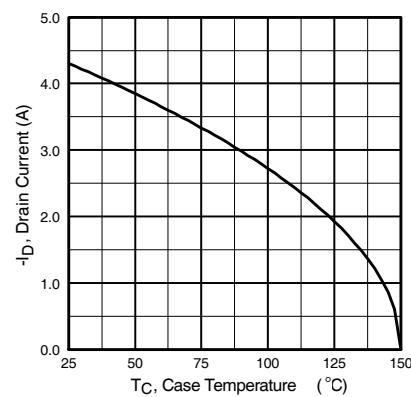
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P-Channel

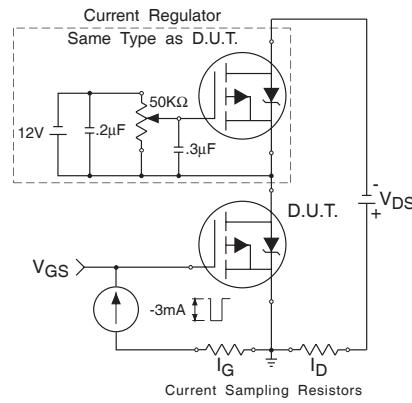
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**Fig 18.** Typical Source-Drain Diode Forward Voltage

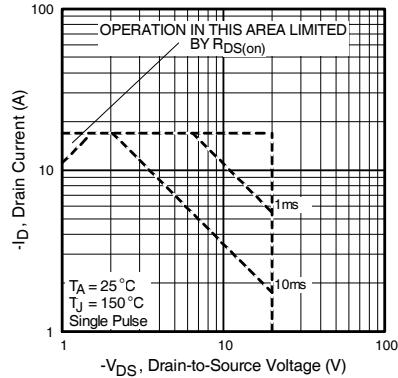


**Fig 20.** Maximum Drain Current Vs. Ambient Temperature

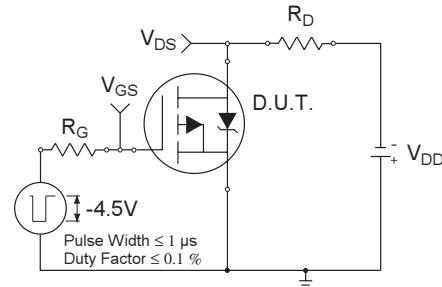


**Fig 22a.** Gate Charge Test Circuit

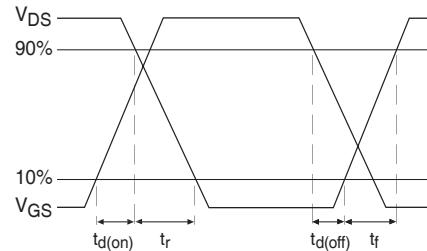
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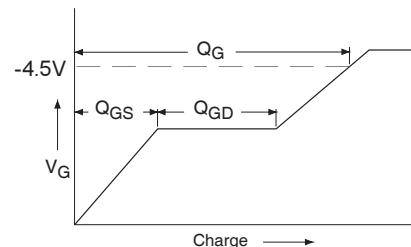
**Fig 19.** Maximum Safe Operating Area



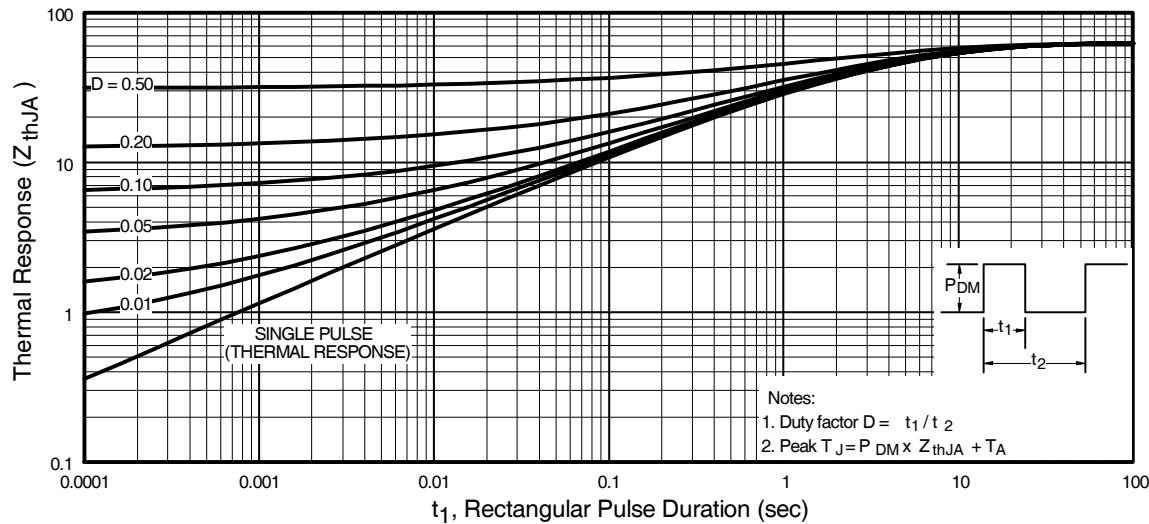
**Fig 21a.** Switching Time Test Circuit



**Fig 21b.** Switching Time Waveforms

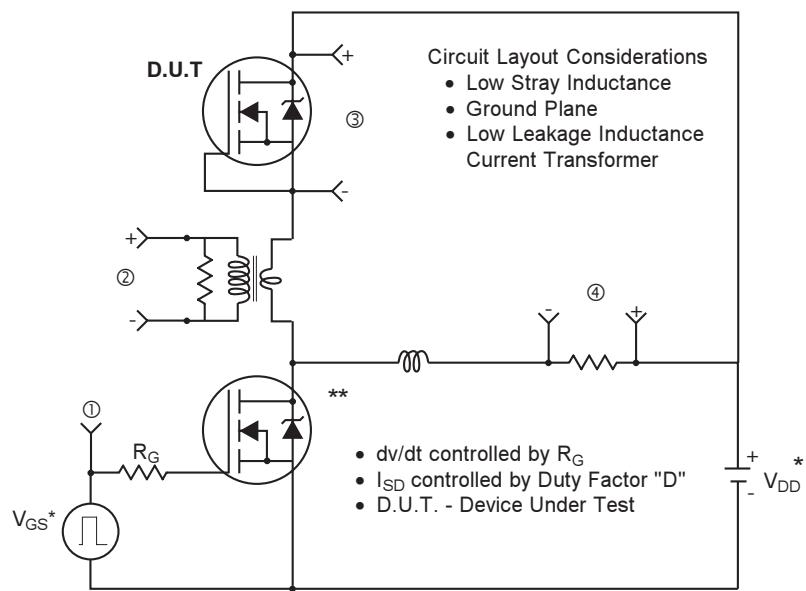


**Fig 22b.** Basic Gate Charge Waveform



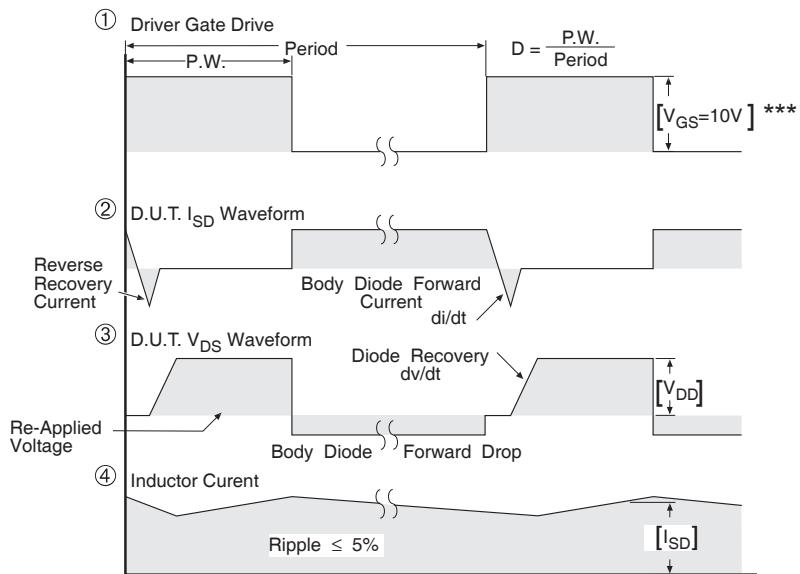
**Fig 23.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

## Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity for P-Channel

\*\* Use P-Channel Driver for P-Channel Measurements



\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

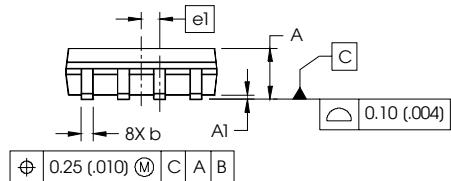
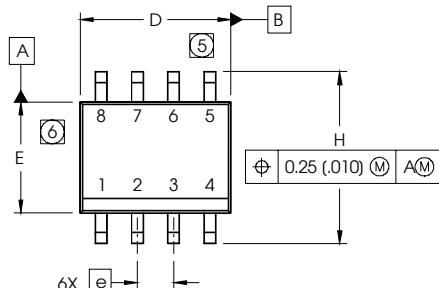
**Fig 24.** For N and P Channel HEXFETs

International  
**IR** Rectifier

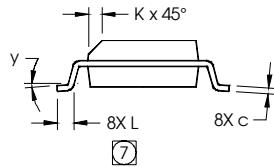
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## SO-8 Package Outline

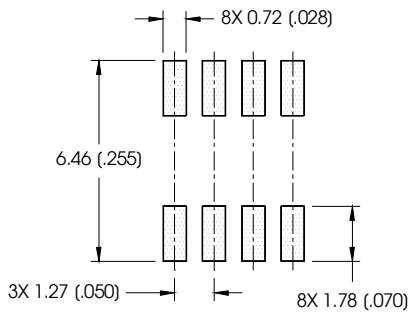
Dimensions are shown in millimeters (inches)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

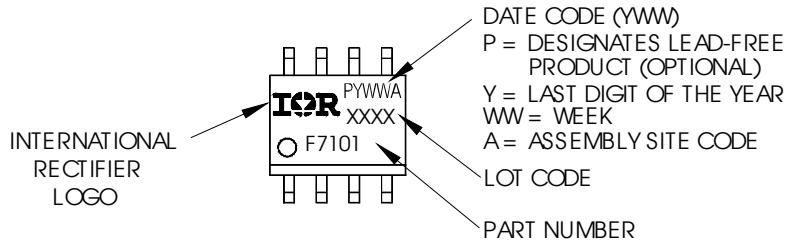


FOOTPRINT



## SO-8 Part Marking

EXAMPLE: THIS IS AN IRF7101 (MOSFET)



Notes:

1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

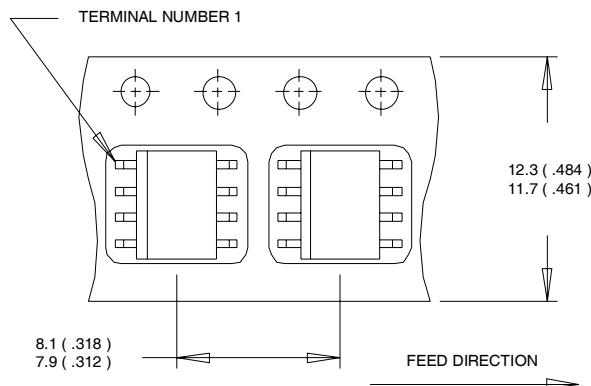
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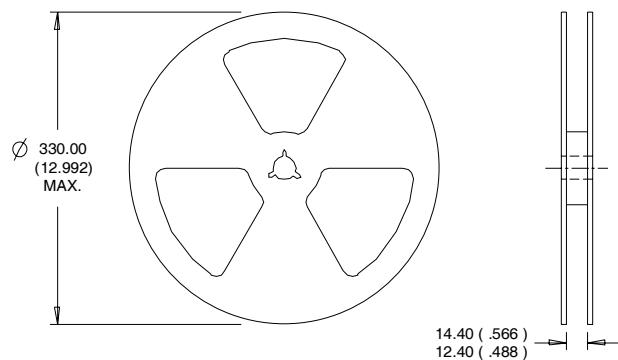
## SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

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