



May 2000

**QFET™**

# FQS4901

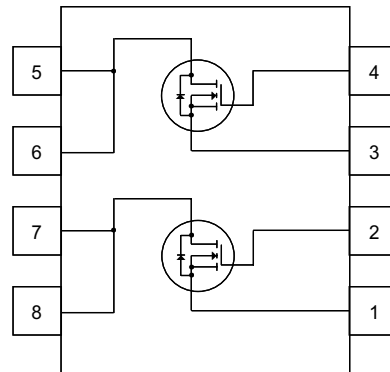
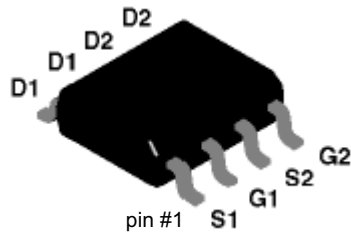
## 400V Dual N-Channel MOSFET

### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, electronic lamp ballast based on half bridge.

### Features

- 0.45A, 400V,  $R_{DS(on)} = 4.2\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 5.8 nC)
- Low Crss ( typical 5.0 pF)
- Fast switching
- Improved dv/dt capability



### Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	FQS4901	Units
V <sub>DSS</sub>	Drain-Source Voltage	400	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>A</sub> = 25°C) - Continuous (T <sub>A</sub> = 70°C)	0.45	A
		0.285	A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	1.8	A
V <sub>GSS</sub>	Gate-Source Voltage	± 25	V
dv/dt	Peak Diode Recovery dv/dt (Note 2)	4.5	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>A</sub> = 25°C) (T <sub>A</sub> = 70°C)	2.0	W
		1.3	W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C

### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	400	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.42	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 320\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

**On Characteristics**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 0.225\text{ A}$	--	3.2	4.2	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 35\text{ V}, I_D = 0.225\text{ A}$ (Note 3)	--	0.283	--	S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	160	210	pF
$C_{oss}$	Output Capacitance		--	30	40	pF
$C_{rss}$	Reverse Transfer Capacitance		--	5	6.5	pF

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 200\text{ V}, I_D = 0.45\text{ A},$ $R_G = 25\ \Omega$	--	5	20	ns	
$t_r$	Turn-On Rise Time		--	20	50	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 3,4)	--	20	50	ns
$t_f$	Turn-Off Fall Time		(Note 3,4)	--	35	80	ns
$Q_g$	Total Gate Charge	$V_{DS} = 320\text{ V}, I_D = 0.45\text{ A},$ $V_{GS} = 10\text{ V}$	--	5.8	7.5	nC	
$Q_{gs}$	Gate-Source Charge		(Note 3,4)	--	0.53	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 3,4)	--	3.22	--	nC

**Drain-Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	0.45	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	1.8	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.45\text{ A}$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 0.45\text{ A},$	--	86	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 3)	--	0.15	--	$\mu\text{C}$

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $I_{SD} \leq 0.45\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
3. Pulse Test : Pulse width  $\leq 300\ \mu\text{s}$ , Duty cycle  $\leq 2\%$
4. Essentially independent of operating temperature

Typical Characteristics

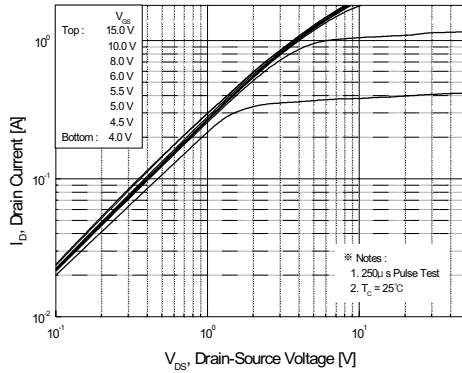


Figure 1. On-Region Characteristics

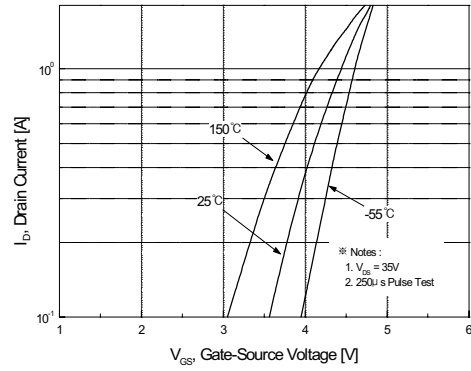


Figure 2. Transfer Characteristics

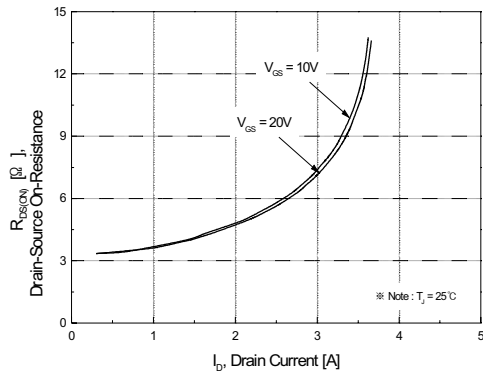


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

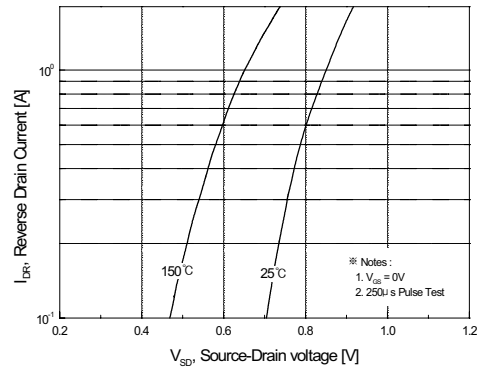


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

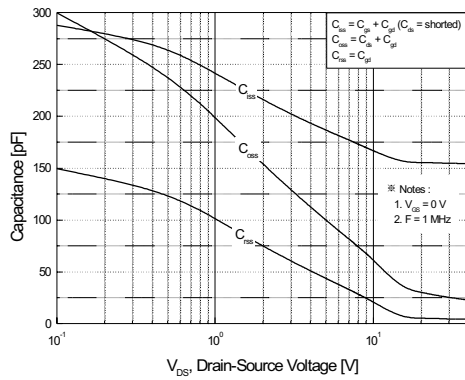


Figure 5. Capacitance Characteristics

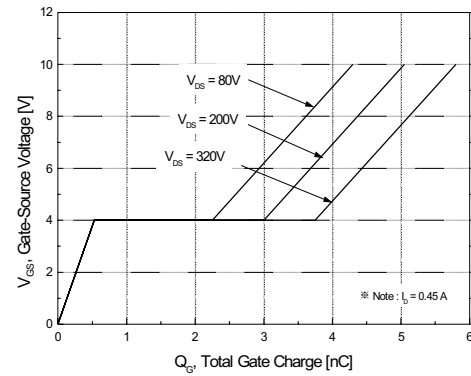
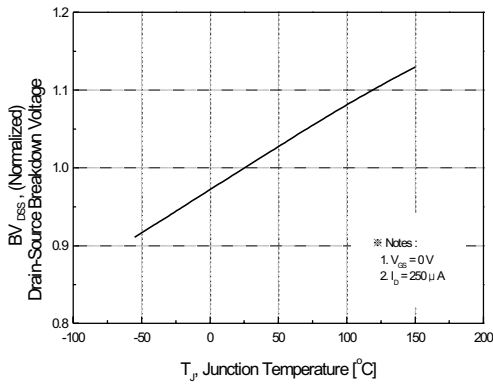
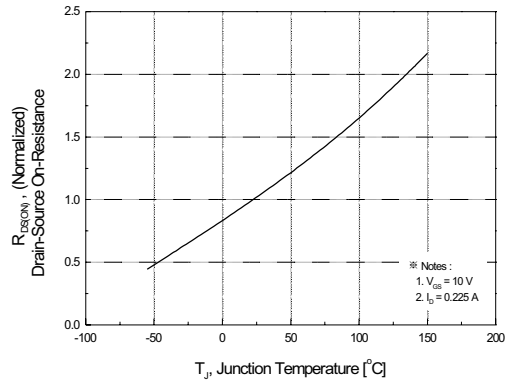


Figure 6. Gate Charge Characteristics

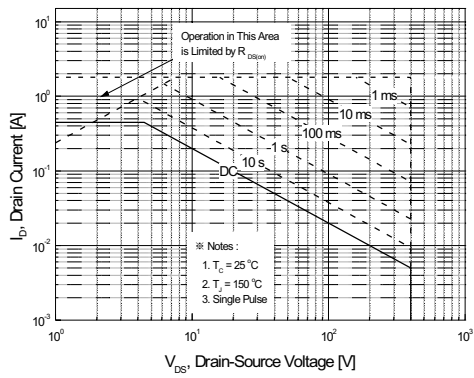
**Typical Characteristics** (Continued)



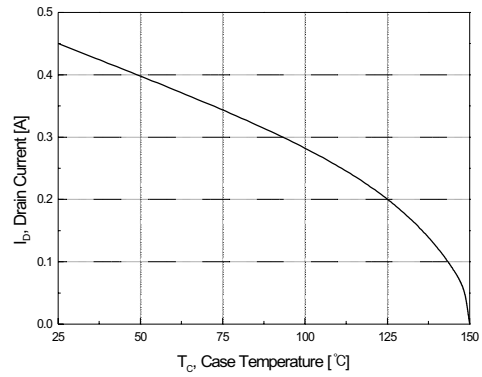
**Figure 7. Breakdown Voltage Variation vs. Temperature**



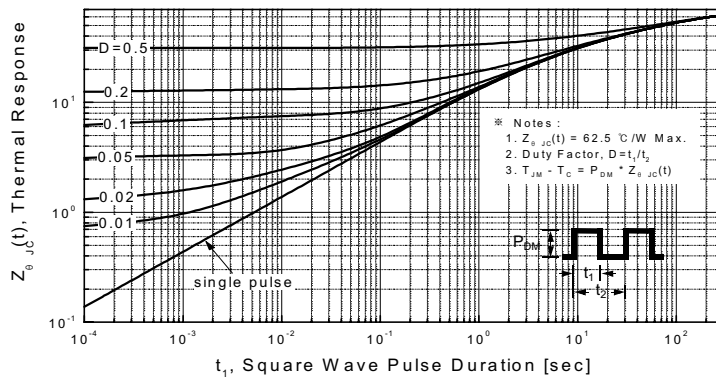
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

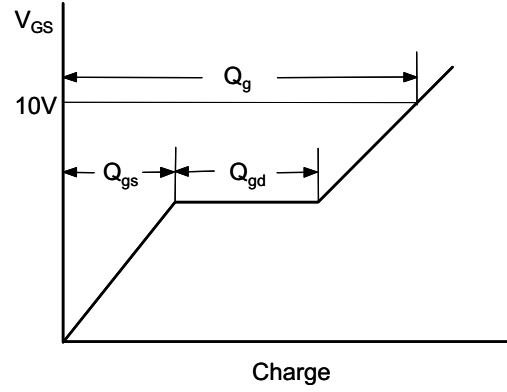
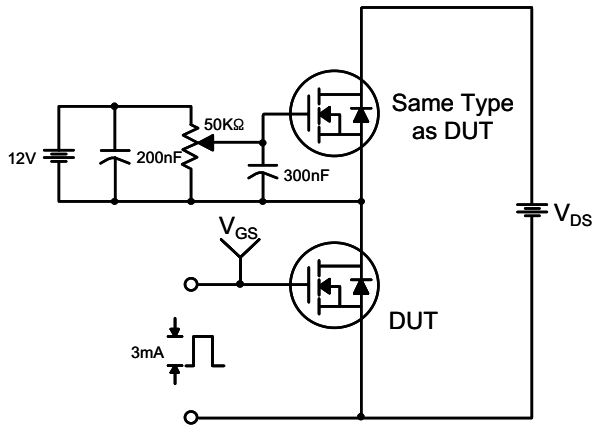


**Figure 10. Maximum Drain Current vs. Case Temperature**

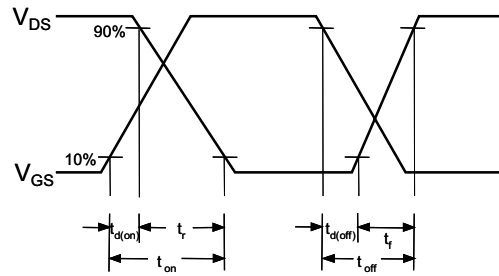
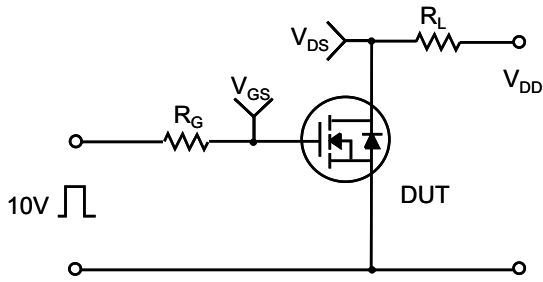


**Figure 11. Transient Thermal Response Curve**

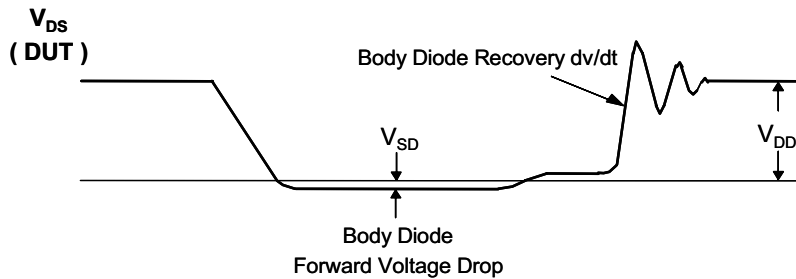
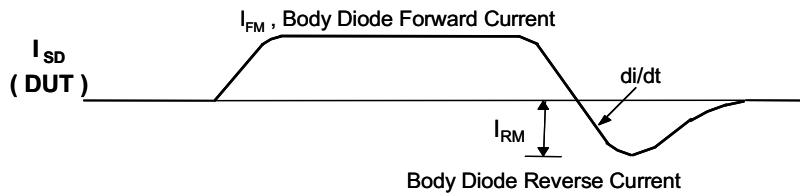
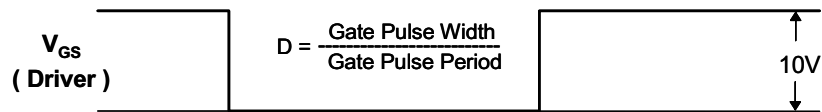
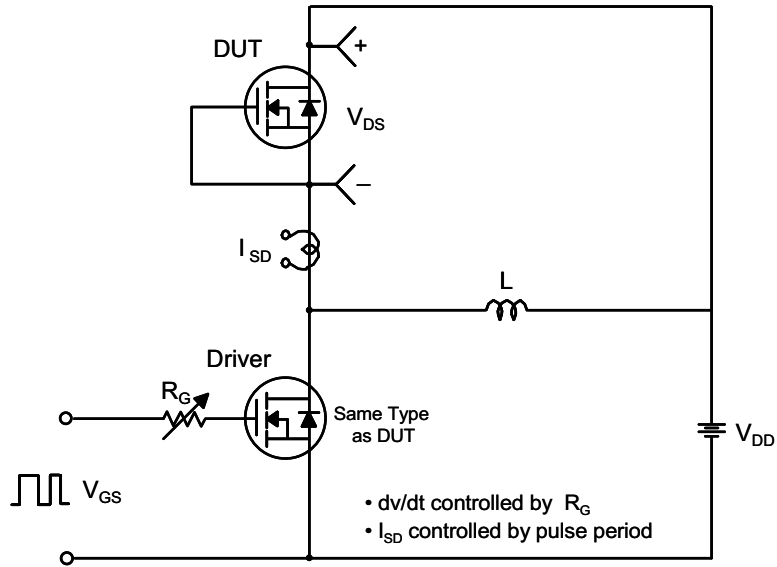
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

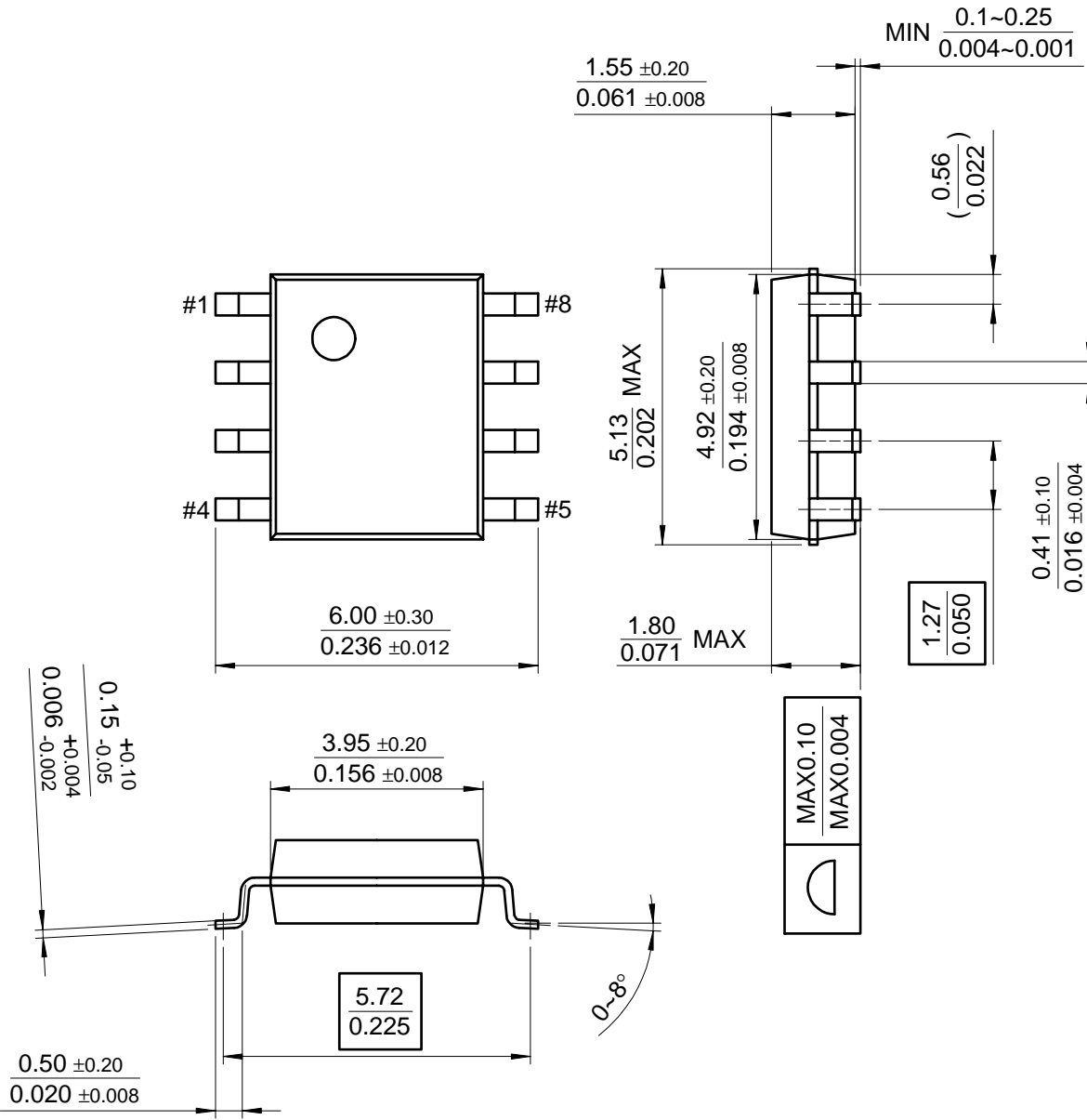


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

8SOP



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