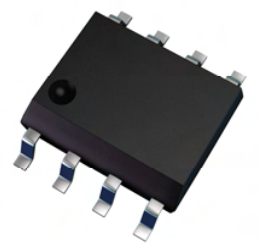
A Product Line of
Diodes Incorporated

ZXMC10A816N8
100V SO8 Complementary Dual enhancement mode MOSFET

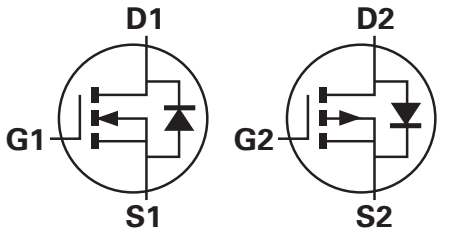
Summary

Device	$V_{(BR)DSS}$ (V)	Q_G (nC)	$R_{DS(on)}$ (Ω)	I_D (A) T_A= 25°C
Q1	100	9.2	0.230 @ V_{GS}= 10V	2.1
			0.300 @ V_{GS}= 4.5V	1.9
Q2	-100	16.5	0.235 @ V_{GS}= -10V	-2.2
			0.320 @ V_{GS}= -4.5V	-1.9



Description

This new generation complementary dual MOSFET features low on-resistance achievable with low gate drive.



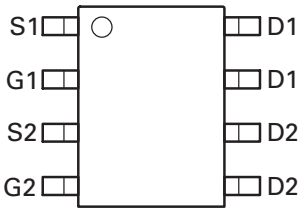
Q1 N-Channel Q2 P-Channel

Features

- 100 V Complementary in SOIC package
- Low on-resistance
- Fast switching speed
- Low voltage (V_{GS} = 4.5 V) gate drive

Applications

- DC motor control
- Backlighting
- Class D Audio Output Stages (<100W)



Top view

Ordering information

Device	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMC10A816N8TC	13	12	2,500

Device marking

ZXMC
10A816

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Absolute maximum ratings

Parameter	Symbol	N-channel Q1	P-channel Q2	Unit
Drain-Source voltage	V_{DSS}	100	-100	V
Gate-Source voltage	V_{GS}	±20	±20	V
Continuous Drain current @ V_{GS}= 10V; T_A=25°C (b)(d) @ V_{GS}= 10V; T_A=70°C (b)(d) @ V_{GS}= 10V; T_A=25°C (a)(d) @ V_{GS}= 10V; T_A=25°C (a)(e) @ V_{GS}= 10V; T_L=25°C (f)(d)	I_D	2.1 1.7 1.7 2.0 2.3	-2.2 -1.8 -1.7 -2.0 -2.4	A
Pulsed Drain current @ V_{GS}= 10V; T_A=25°C (c)(d)	I_{DM}	9.4	-10.5	A
Continuous Source current (Body diode) at T_A=25°C (b)(d)	I_S	3.0	-3.1	A
Pulsed Source current (Body diode) at T_A=25°C (c)(d)	I_{SM}	9.4	-10.5	A
Power dissipation at T_A=25°C (a)(d) Linear derating factor	P_D	1.3 10.0		W mW/°C
Power dissipation at T_A=25°C (a)(e) Linear derating factor	P_D	1.8 14.2		W mW/°C
Power dissipation at T_A=25°C (b)(d) Linear derating factor	P_D	2.1 16.7		W mW/°C
Power dissipation at T_L=25°C (f)(d) Linear derating factor	P_D	2.4 18.9	2.6 20.4	W mW/°C
Operating and storage temperature range	T_j, T_{stg}	-55 to 150		°C

Thermal resistance

Parameter	Symbol	Value		Unit
Junction to ambient (a)(d)	$R_{\theta JA}$	100		°C/W
Junction to ambient (a)(e)	$R_{\theta JA}$	70		°C/W
Junction to ambient (b)(d)	$R_{\theta JA}$	60		°C/W
Junction to lead (f)(d)	$R_{\theta JL}$	53	49	°C/W

NOTES:

(a) For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.

(b) Same as note (a), except the device is measured at t ≤ 10 sec.

(c) Same as note (a), except the device is pulsed with D= 0.02 and pulse width 300 µs. The pulse current is limited by the maximum junction temperature.

(d) For a dual device with one active die.

(e) For a device with two active die running at equal power.

(f) Thermal resistance from junction to solder-point (at the end of the drain lead); the device is operating in a steady-state condition.

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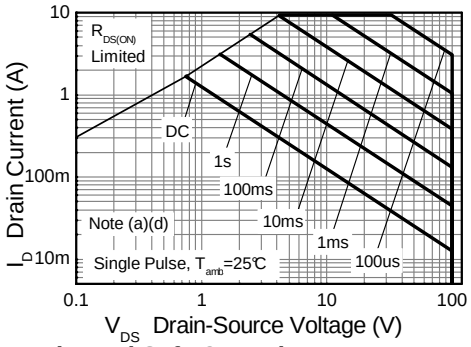
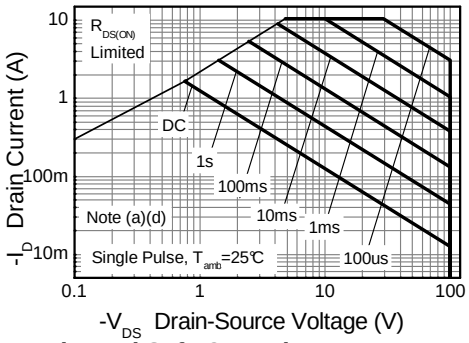
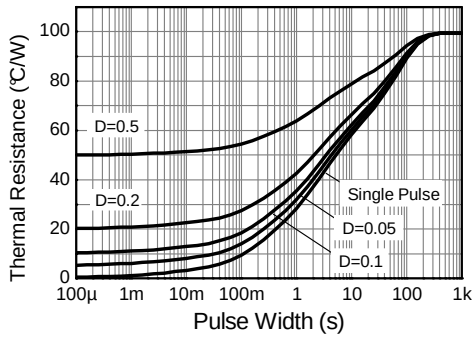
Thermal characteristics



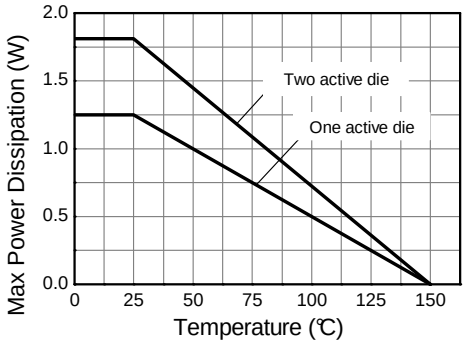
N-channel Safe Operating Area



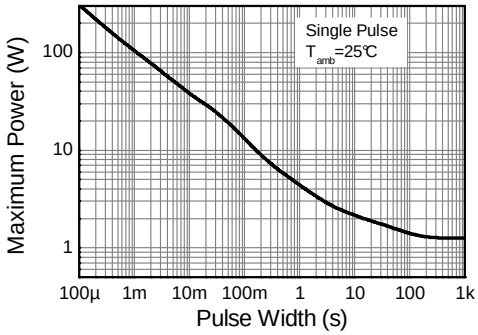
P-channel Safe Operating Area



Transient Thermal Impedance



Derating Curve



Pulse Power Dissipation

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Q1 (N-channel) electrical characteristics (at T_{amb} = 25°C unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-Source breakdown voltage	$V_{(BR)DSS}$	100			V	I_D = 250µA, V_{GS}= 0V
Zero Gate voltage Drain current	I_{DSS}			0.5	µA	V_{DS}= 100V, V_{GS}= 0V
Gate-Body leakage	I_{GSS}			100	nA	V_{GS}= ±20V, V_{DS}= 0V
Gate-Source threshold voltage	$V_{GS(th)}$	1.0		3.0	V	I_D= 250µA, V_{DS}= V_{GS}
Static Drain-Source on-state resistance (a)	$R_{DS(on)}$		0.170 0.210	0.230 0.300	Ω	V_{GS}= 10V, I_D= 1.0A V_{GS}= 4.5V, I_D= 0.5A
Forward Transconductance (a) (c)	g_{fs}		4.8		S	V_{DS}= 15V, I_D= 1.6A
Dynamic						
Capacitance (c)						
Input capacitance	C_{iss}		497		pF	V_{DS}= 50V, V_{GS}= 0V f= 1MHz
Output capacitance	C_{oss}		29		pF	
Reverse transfer capacitance	C_{rss}		18		pF	
Switching (b) (c)						
Turn-on-delay time	$t_{d(on)}$		2.9		ns	V_{DD}= 50V, V_{GS}= 10V I_D= 1.0A $R_G \cong 6.0\Omega$,
Rise time	t_r		2.1		ns	
Turn-off delay time	$t_{d(off)}$		12.1		ns	
Fall time	t_f		5.0		ns	
Gate charge (c)						
Total Gate charge	Q_g		9.2		nC	V_{DS}= 50V, V_{GS}= 10V I_D= 1.6A
Gate-Source charge	Q_{gs}		1.7		nC	
Gate-Drain charge	Q_{gd}		2.5		nC	
Source–Drain diode						
Diode forward voltage (a)	V_{SD}		0.85	0.95	V	I_S= 1.7A, V_{GS}= 0V
Reverse recovery time (c)	t_{rr}		32		ns	I_S= 1.7A, di/dt= 100A/µs
Reverse recovery charge (c)	Q_{rr}		40		nC	

NOTES:
(a) Measured under pulsed conditions. Pulse width ≤ 300µs; duty cycle ≤ 2%.
(b) Switching characteristics are independent of operating junction temperature.
(c) For design aid only, not subject to production testing

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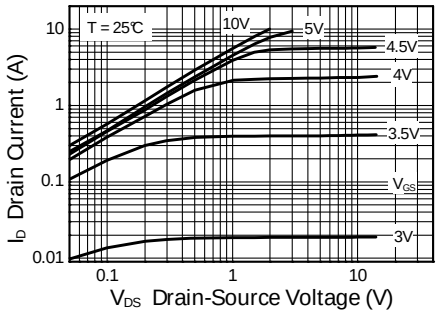
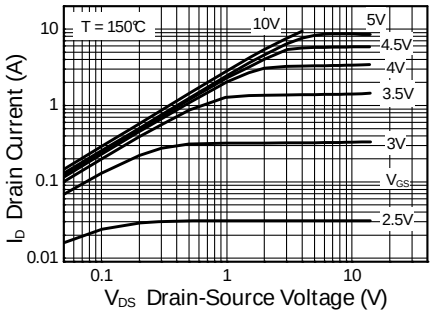
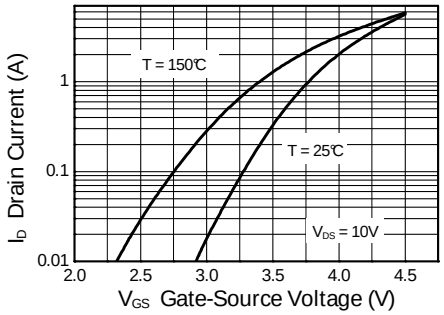
Q1 (N-channel) typical characteristics



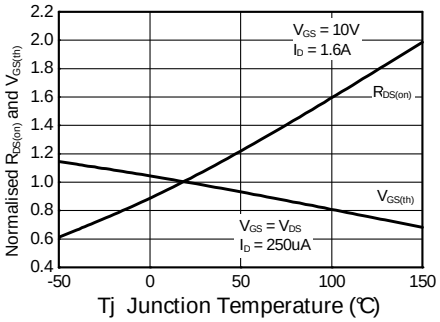
Output Characteristics



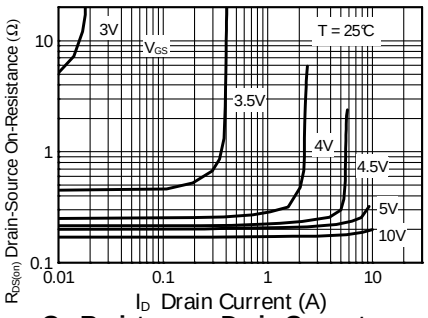
Output Characteristics



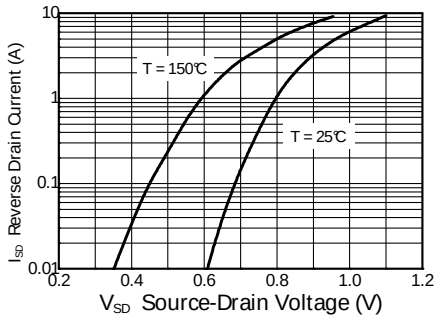
Typical Transfer Characteristics



Normalised Curves v Temperature



On-Resistance v Drain Current



Source-Drain Diode Forward Voltage

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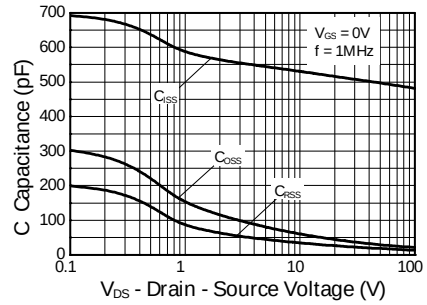
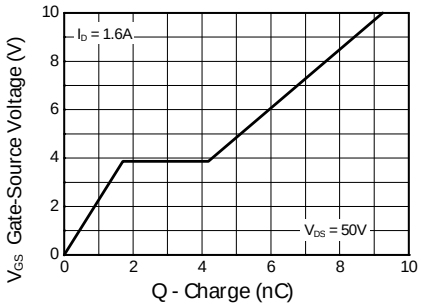
Q1 (N-channel) typical characteristics –continued

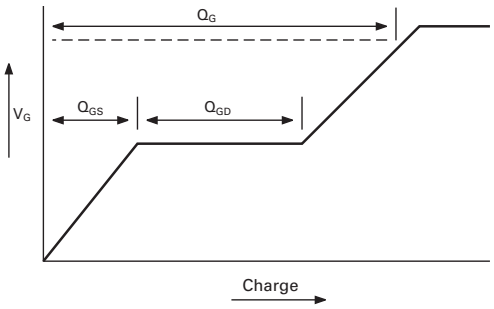


Capacitance v Drain-Source Voltage

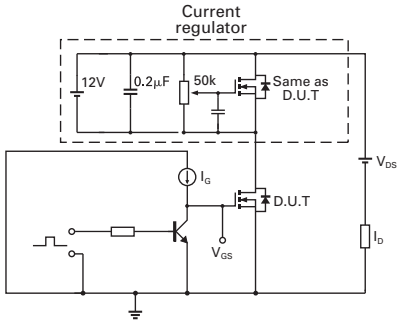


Gate-Source Voltage v Gate Charge

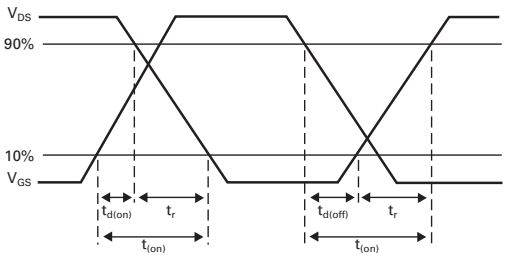
Test circuits



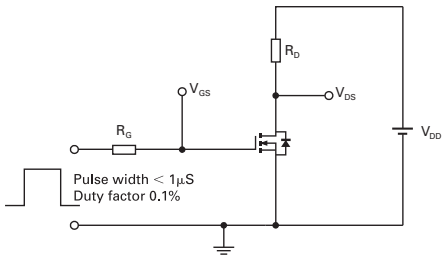
Basic gate charge waveform



Gate charge test circuit



Switching time waveforms



Switching time test circuit

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Q1 (P-channel) electrical characteristics (at T_{amb} = 25°C unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-Source breakdown voltage	$V_{(BR)DSS}$	-100			V	I_D = -250µA, V_{GS}= 0V
Zero Gate voltage Drain current	I_{DSS}			-0.5	µA	V_{DS}= -100V, V_{GS}= 0V
Gate-Body leakage	I_{GSS}			100	nA	V_{GS}= ±20V, V_{DS}= 0V
Gate-Source threshold voltage	$V_{GS(th)}$	-2.0		-4.0	V	I_D= -250µA, V_{DS}= V_{GS}
Static Drain-Source on-state resistance (a)	$R_{DS(on)}$		0.170 0.250	0.235 0.320	Ω	V_{GS}= -10V, I_D= -1.0A V_{GS}= -4.5V, I_D= -0.5A
Forward Transconductance (a) (c)	g_{fs}		4.7		S	V_{DS}= -15V, I_D= -2.1A
Dynamic						
Capacitance (c)						
Input capacitance	C_{iss}		717		pF	V_{DS}= -50V, V_{GS}= 0V f= 1MHz
Output capacitance	C_{oss}		55		pF	
Reverse transfer capacitance	C_{rss}		46		pF	
Switching (b) (c)						
Turn-on-delay time	$t_{d(on)}$		4.3		ns	V_{DD}= -50V, V_{GS}= -10V I_D= -1A $R_G \cong$ 6.0Ω,
Rise time	t_r		5.2		ns	
Turn-off delay time	$t_{d(off)}$		20		ns	
Fall time	t_f		12		ns	
Gate charge (c)						
Total Gate charge	Q_g		16.5		nC	V_{DS}= -50V, V_{GS}= -10V I_D= -2.1A
Gate-Source charge	Q_{gs}		2.5		nC	
Gate-Drain charge	Q_{gd}		5.4		nC	
Source–Drain diode						
Diode forward voltage (a)	V_{SD}		-0.85	-0.95	V	I_S= -1.7A, V_{GS}= 0V
Reverse recovery time (c)	t_{rr}		43		ns	I_S= -1.7A, di/dt= 100A/µs
Reverse recovery charge (c)	Q_{rr}		77		nC	

NOTES:
(a) Measured under pulsed conditions. Pulse width ≤ 300µs; duty cycle ≤ 2%.
(b) Switching characteristics are independent of operating junction temperature.
(c) For design aid only, not subject to production testing

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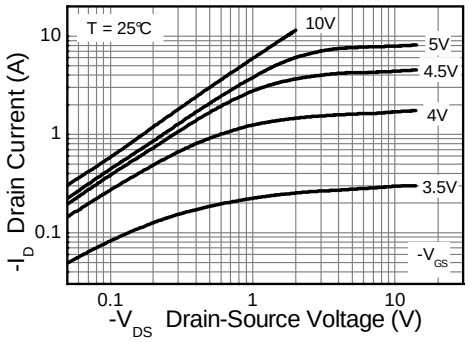
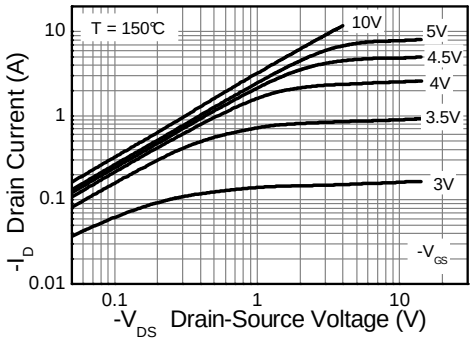
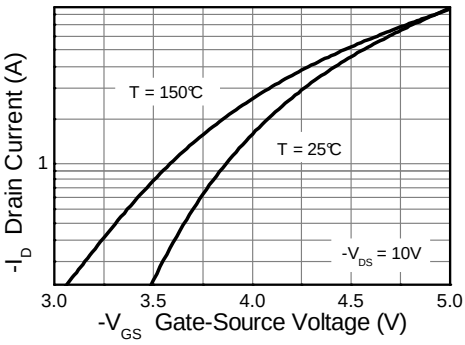
Q2 (P-channel) typical characteristics



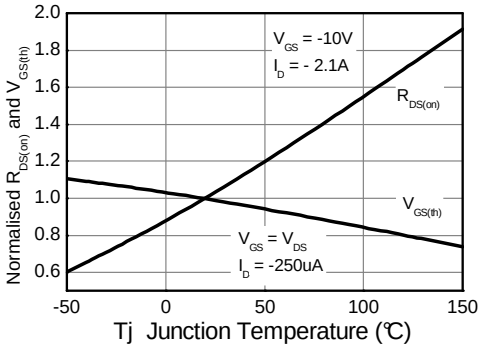
Output Characteristics



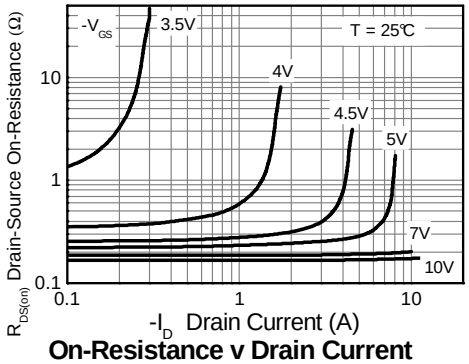
Output Characteristics



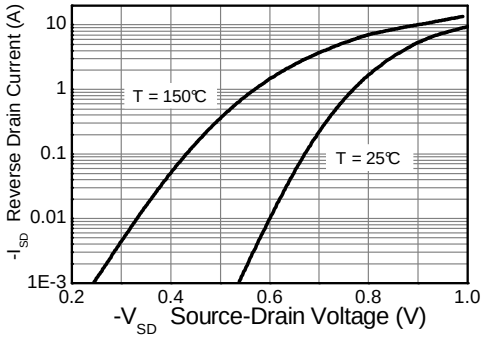
Typical Transfer Characteristics



Normalised Curves v Temperature



On-Resistance v Drain Current



Source-Drain Diode Forward Voltage

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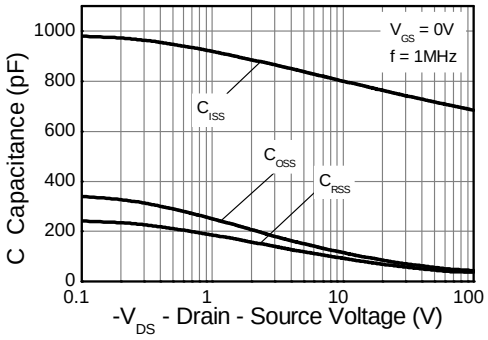
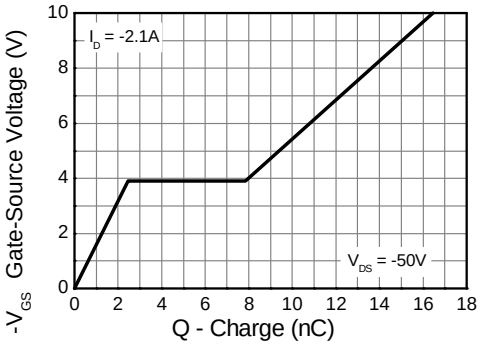
Q2 (P-channel) typical characteristics –continued

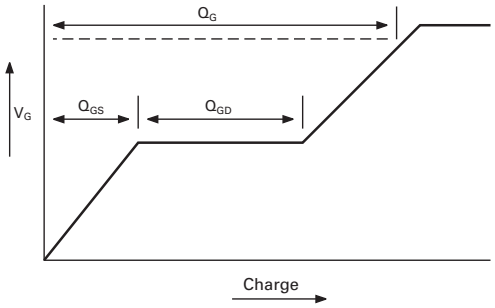


Capacitance v Drain-Source Voltage

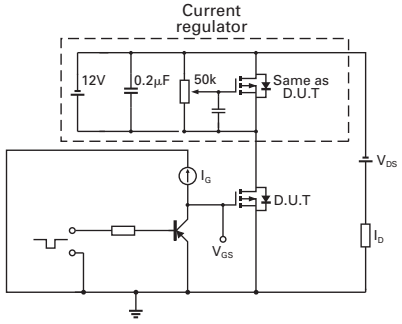


Gate-Source Voltage v Gate Charge

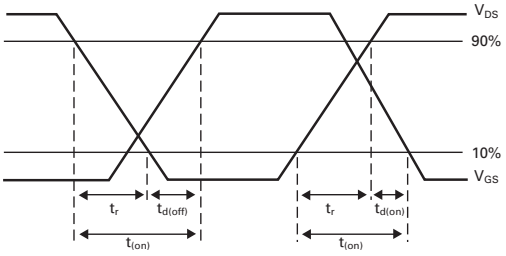
Test circuits



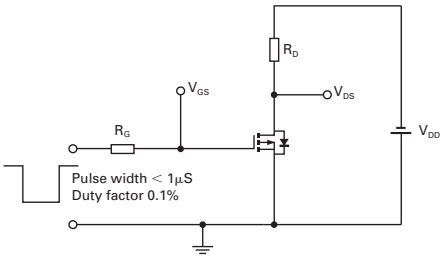
Basic gate charge waveform



Gate charge test circuit



Switching time waveforms



Switching time test circuit

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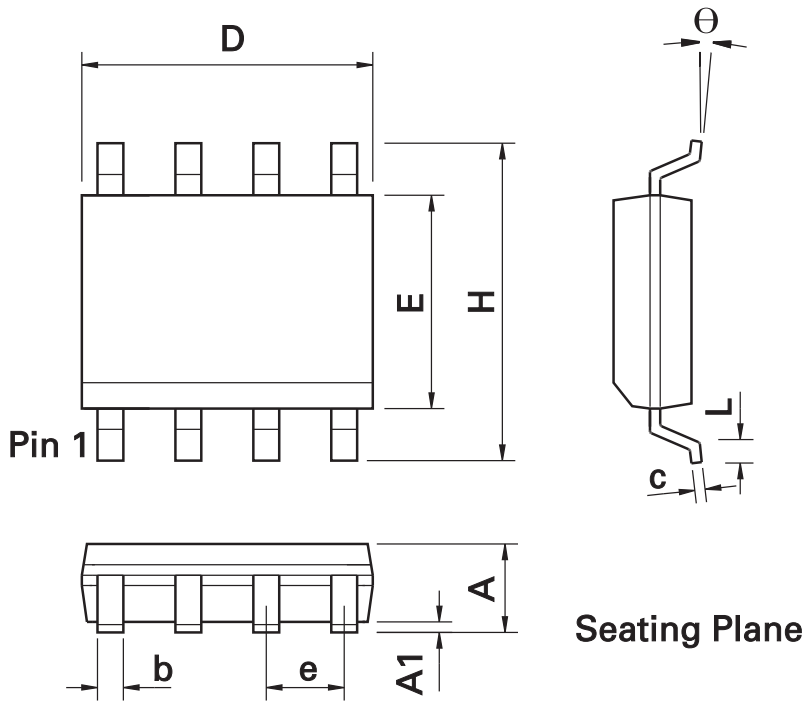
Packaging details - SO8



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	θ	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	-	-	-	-	-
L	0.016	0.050	0.40	1.27	-	-	-	-	-

Note: Controlling dimensions are in inches. Approximate dimensions are provided in millimeters

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Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

   1. are intended to implant into the body, or
   2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

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