FAIRCHILD SEMICONDUCTOR®

May 2010

FDMA2002NZ

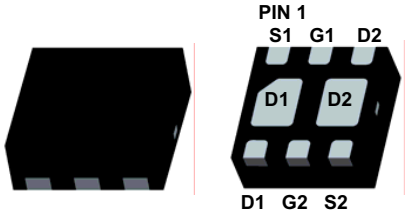
Dual N-Channel PowerTrench® MOSFET

General Description

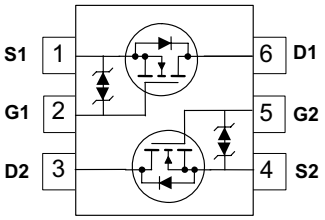
This device is designed specifically as a single package solution for dual switching requirements in cellular handset and other ultra-portable applications. It features two independent N-Channel MOSFETs with low on-state resistance for minimum conduction losses. The MicroFET 2x2 offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Features

- 2.9 A, 30 V $R_{DS(ON)}$ = 123 mΩ @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 140 mΩ @ V_{GS} = 3.0 V
  $R_{DS(ON)}$ = 163 mΩ @ V_{GS} = 2.5 V
- Low profile – 0.8 mm maximum – in the new package MicroFET 2x2 mm
- HBM ESD protection level = 1.8kV (Note 3)
- RoHS Compliant
- Free from halogenated compounds and antimony oxides



MicroFET 2x2



Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain-Source Voltage		30	V
V_{GS}	Gate-Source Voltage		±12	V
I_D	Drain Current – Continuous (T_C = 25°C, V_{GS} = 4.5V)		2.9	A
	– Continuous (T_C = 25°C, V_{GS} = 2.5V)		2.7	
	– Pulsed		10	
P_D	Power Dissipation for Single Operation	(Note 1a)	1.5	W
	Power Dissipation for Single Operation	(Note 1b)	0.65	
T_J, T_{STG}	Operating and Storage Temperature		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	83 (Single Operation)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	193 (Single Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1c)	68 (Dual Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1d)	145 (Dual Operation)	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
002	FDMA2002NZ	7''	8mm	3000 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		25		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate–Body Leakage Current	V_{GS} = ± 12 V, V_{DS} = 0 V			±10	μA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.4	1.0	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		–3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 4.5V, I_D = 2.9A		75	123	mΩ
		V_{GS} = 3.0V, I_D = 2.7A		84	140	
		V_{GS} = 2.5V, I_D = 2.5A		92	163	
		V_{GS} = 4.5V, I_D = 2.9A, T_C = 85°C		95	166	
		V_{GS} = 3.0V, I_D = 2.7A, T_C = 150°C		138	203	
		V_{GS} = 2.5V, I_D = 2.5A, T_C = 150°C		150	268	
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		190	220	pF
C_{oss}	Output Capacitance			30	40	pF
C_{rss}	Reverse Transfer Capacitance			20	30	pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		6	12	ns
t_r	Turn–On Rise Time			8	16	ns
$t_{d(off)}$	Turn–Off Delay Time			12	21	ns
t_f	Turn–Off Fall Time			2	10	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 2.9 A, V_{GS} = 4.5 V		2.4	3.0	nC
Q_{gs}	Gate–Source Charge			0.35		nC
Q_{gd}	Gate–Drain Charge			0.75		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Source–Drain Diode Forward Current				2.9	A
V_{SD}	Source–Drain Diode Forward Voltage	I_S = 2.0 A		0.9	1.2	V
		I_S = 1.1 A		0.8	1.2	
t_{rr}	Diode Reverse Recovery Time	I_F = 2.9 A, dI_F/dt = 100 A/μs		10		ns
Q_{rr}	Diode Reverse Recovery Charge			2		nC

Notes:

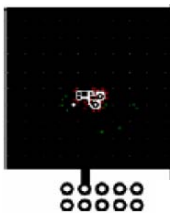
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

   (a) $R_{\theta JA}$ = 86 °C/W when mounted on a 1 in^2 pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For single operation.

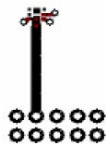
   (b) $R_{\theta JA}$ = 173 °C/W when mounted on a minimum pad of 2 oz copper. For single operation.

   (c) $R_{\theta JA}$ = 69 °C/W when mounted on a 1 in^2 pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For dual operation.

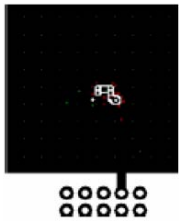
   (d) $R_{\theta JA}$ = 151 °C/W when mounted on a minimum pad of 2 oz copper. For dual operation.



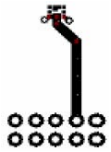
a)86 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b)173 °C/W when mounted on a minimum pad of 2 oz copper.



c)69 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



d)151 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test : Pulse Width < 300 us, Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics

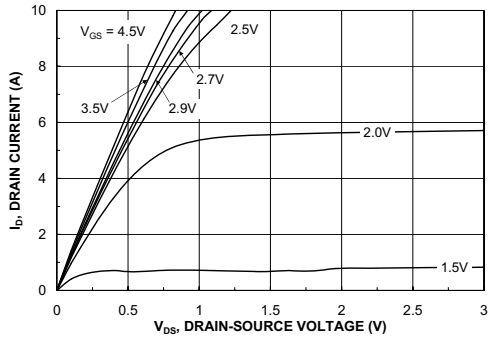


Figure 1. On-Region Characteristics.

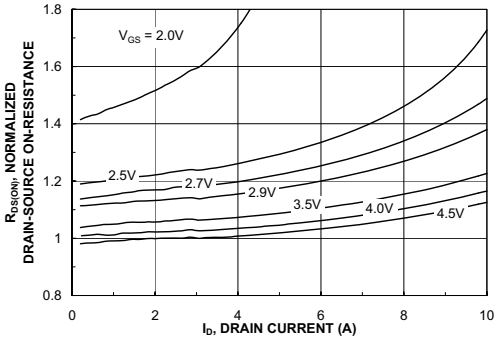


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

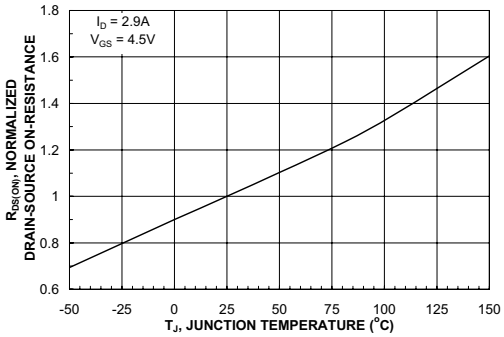


Figure 3. On-Resistance Variation with Temperature.

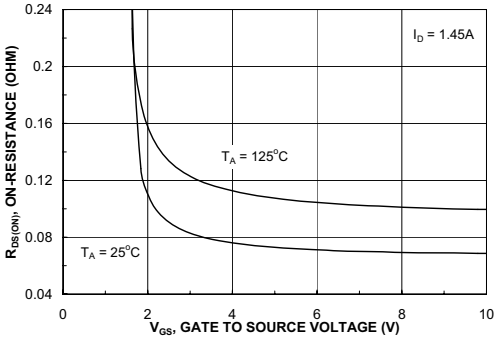


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

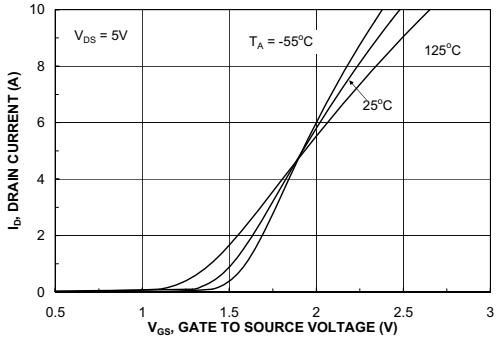


Figure 5. Transfer Characteristics.

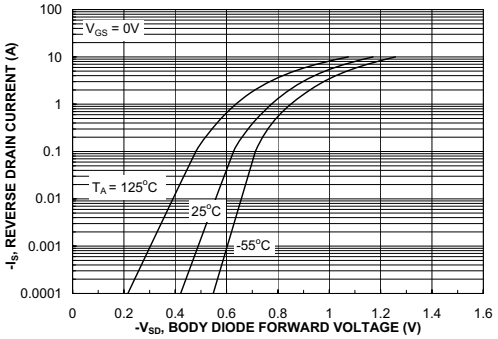
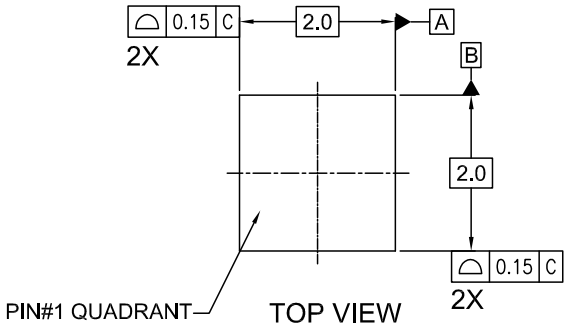
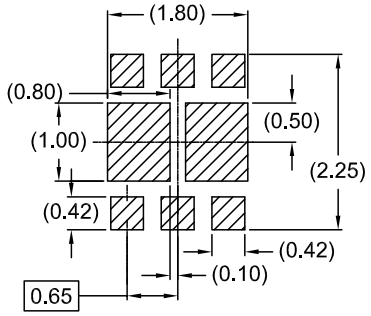


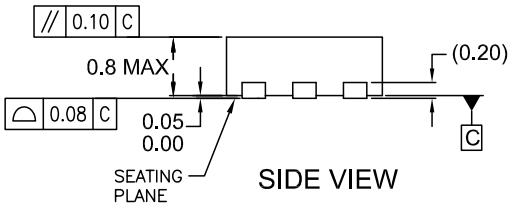
Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

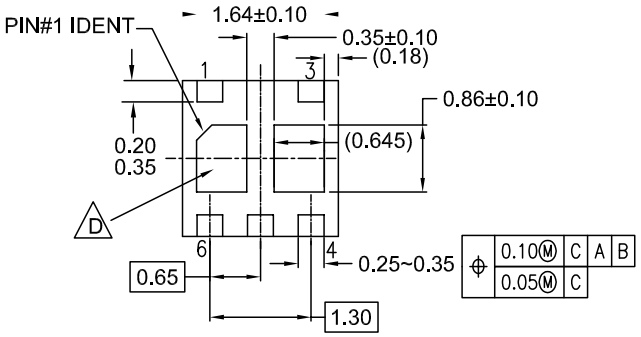
Dimensional Outline and Pad Layout





RECOMMENDED LAND PATTERN





BOTTOM VIEW

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION VCCC EXCEPT AS NOTED.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. NON-JEDEC DUAL DAP

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