July 2000



FDC6327C

Dual N & P-Channel 2.5V Specified PowerTrench[™] MOSFET

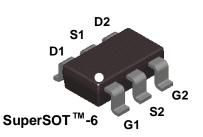
General Description

These N & P-Channel 2.5V specified MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO-8 and TSSOP-8 packages are impractical.

Applications

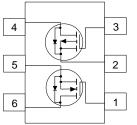
- DC/DC converter
- Load switch
- Motor driving



Features

• N-Channel 2.7A, 20V. $R_{DS(on)} = 0.08\Omega @ V_{GS} = 4.5V$ $R_{DS(on)} = 0.12\Omega @ V_{GS} = 2.5V$

- P-Channel -1.6A, -20V.R $_{\rm DS(on)}$ = 0.17 Ω @ V $_{\rm GS}$ = -4.5V $R_{DS(on)}$ = 0.25 Ω @ V_{GS} = -2.5V
- · Fast switching speed.
- · Low gate charge.
- High performance trench technology for extremely low R_{DS(ON)}.
- SuperSOT[™]-6 package: small footprint (72% smaller than SO-8); low profile (1mm thick).



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter N-Channel P-Channel Units					
V _{DSS}	Drain-Source Voltage		20	-20	V	
V _{GSS}	Gate-Source Voltage		<u>+</u> 8	<u>+</u> 8	V	
ID	Drain Current - Continuous	(Note 1a)	2.7	-1.9	А	
	- Pulsed		8	-8	1	
PD	Power Dissipation	(Note 1a)	0.9	96	W	
		(Note 1b)	0.	9	1	
		(Note 1c)	0.	7	1	
T _J , T _{stg}	Operating and Storage Junction Temperatu	re Range	-55 to	+150	۰C	
Therma	I Characteristics					
R _{θJA}	Thermal Resistance, Junction-to-Ambient	(Note 1a)	13	30	∘C/W	
R _{θJC}	Thermal Resistance, Junction-to-Case	(Note 1)	6	0	∘C/W	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.327	FDC6327C	7"	8mm	3000

©1999 Fairchild Semiconductor Corporation

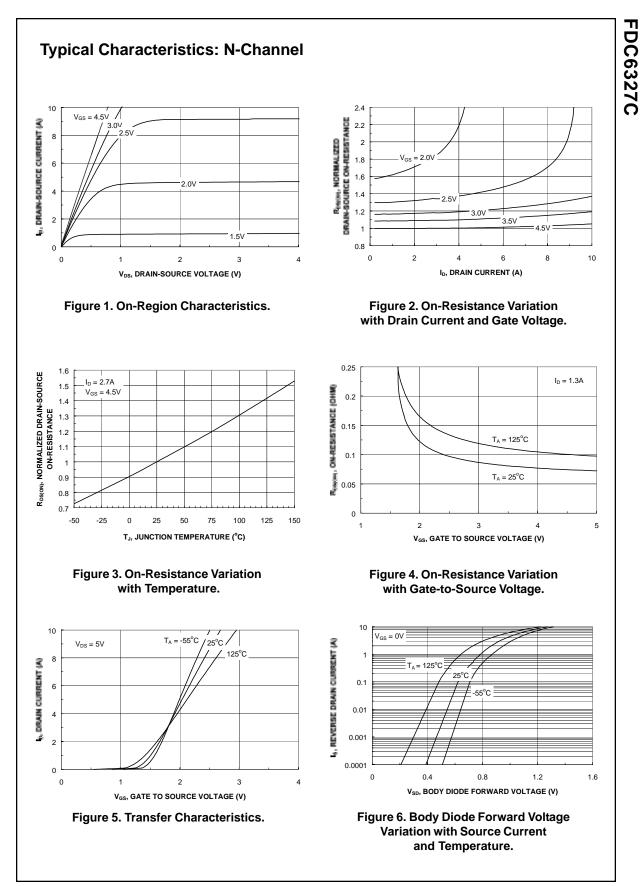
Symbol	Parameter	Test Conditions	Туре	Min	Тур	Мах	Units
Off Cha	restariation						
BV _{DSS}	acteristics	V 0.V I 250 A	N-Ch	20			V
DVDSS	Voltage	$V_{GS} = 0 V, I_D = 250 \mu A$ $V_{GS} = 0 V, I_D = -250 \mu A$	P-Ch	-20			v
ABVDSS	Breakdown Voltage	$I_D = 250 \mu\text{A}$, Referenced to 25°C	N-Ch	20	12		mV/∘C
Δ <u>DVUSS</u> ΔTJ	Temperature Coefficient	$I_D = 250 \ \mu$ A, Referenced to 25°C	P-Ch		-19		1117/-0
	Zero Gate Voltage Drain	$V_{DS} = 16 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	N-Ch		10	1	μA
055	Current	$V_{DS} = -16 V, V_{GS} = 0 V$	P-Ch			-1	μ
I _{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 8 V, V_{DS} = 0 V$	All			100	nA
I _{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -8 V, V_{DS} = 0 V$	All			-100	nA
On Char V _{GS(th)}	acteristics (Note 2) Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	N-Ch	0.4	0.9	1.5	V
00(11)		$V_{DS} = V_{GS}, I_D = -250 \mu A$	P-Ch	-0.4	-0.9	-1.5	
AVGS(th)	Gate Threshold Voltage	$I_D = 250 \mu A$, Referenced to $25 \circ C$	N-Ch		-2.1		mV/∘C
ΔT_J	Temperature Coefficient	$I_D = -250 \mu A$, Referenced to $25 \circ C$	P-Ch		2.3		
R _{DS(on)}	Static Drain-Source	$V_{GS} = 4.5 \text{ V}, I_{D} = 2.7 \text{ A}$	N-Ch		0.069	0.08	Ω
	On-Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 2.7 \text{ A}, T_J = 125 \circ \text{C}$	N-Ch		0.094	0.13	
		$V_{GS} = 2.5 \text{ V}, I_D = 2.2 \text{ A}$	N-Ch		0.093	0.12	
		$V_{GS} = -4.5 \text{ V}, \text{ I}_{D} = -1.6 \text{ A}$	P-Ch		0.141	0.17	
		$V_{GS} = -4.5 \text{ V}, I_D = -1.6 \text{ A}, T_J = 125 \circ \text{C}$	P-Ch		0.203	0.27	
		$V_{GS} = -2.5 \text{ V}, I_D = -1.3 \text{ A}$	P-Ch		0.205	0.25	
I _{D(on)}	On-State Drain Current	$V_{GS} = 4.5 V, V_{DS} = 5 V$	N-Ch	8			A
~		$V_{GS} = -4.5 \text{ V}, V_{DS} = -5 \text{ V}$	P-Ch	-8	77		<u> </u>
g fs	Forward Transconductance	$V_{DS} = 5 V, I_D = 2.7 A$ $V_{DS} = -5 V, I_D = -1.9 A$	N-Ch P-Ch		7.7 4.5		S
		$IV_{DS} = -3V, ID = -1.3 A$			4.5	<u> </u>	1
	Characteristics	1	1				1
C _{iss}	Input Capacitance	N-Channel $V_{DS} = 10 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ f} = 1.0 \text{ MHz}$	N-Ch P-Ch		325 315		pF
Coss	Output Capacitance		N-Ch		75		pF

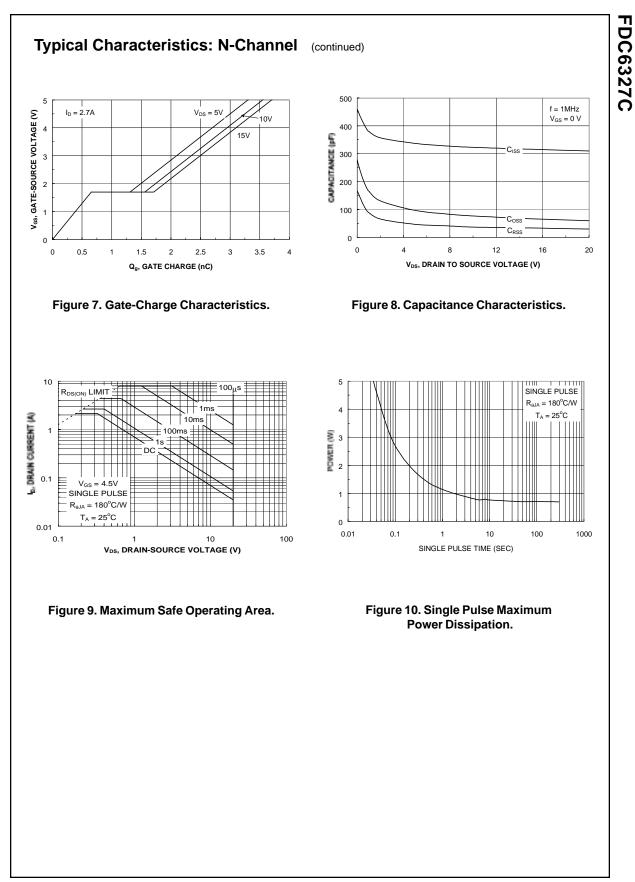
Uiss	Input Capacitance	N-Channel	N-Ch	325	рг
		$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	P-Ch	315	
Coss	Output Capacitance		N-Ch	75	pF
		P-Channel	P-Ch	65	· .
Crss	Reverse Transfer Capacitance	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	N-Ch	35	pF
			P-Ch	24	-

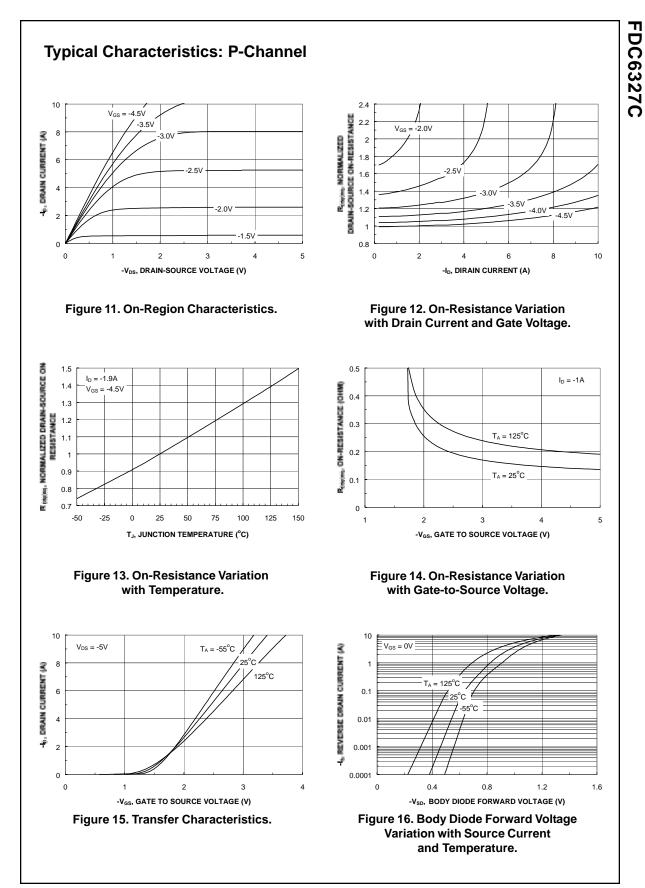
FDC6327C

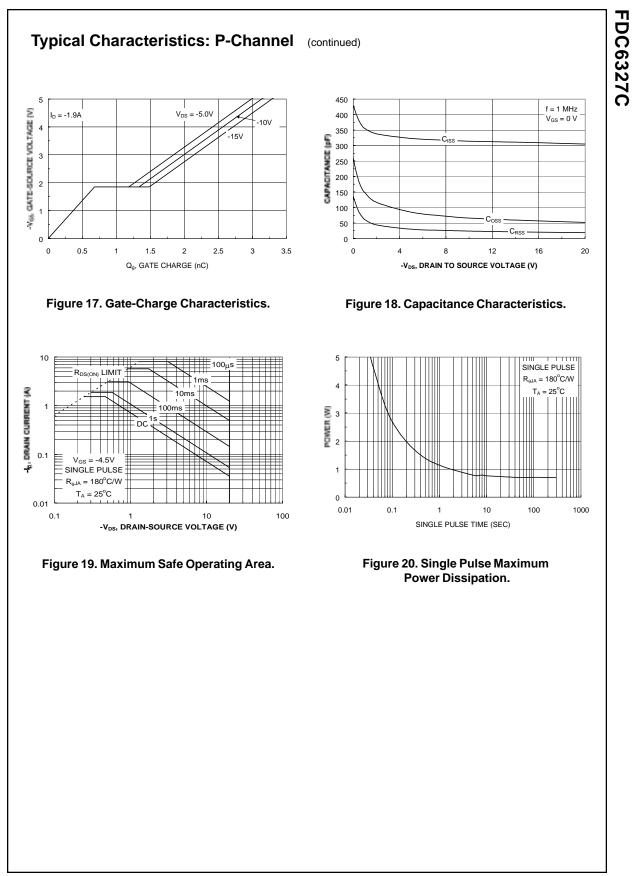
FDC6327C

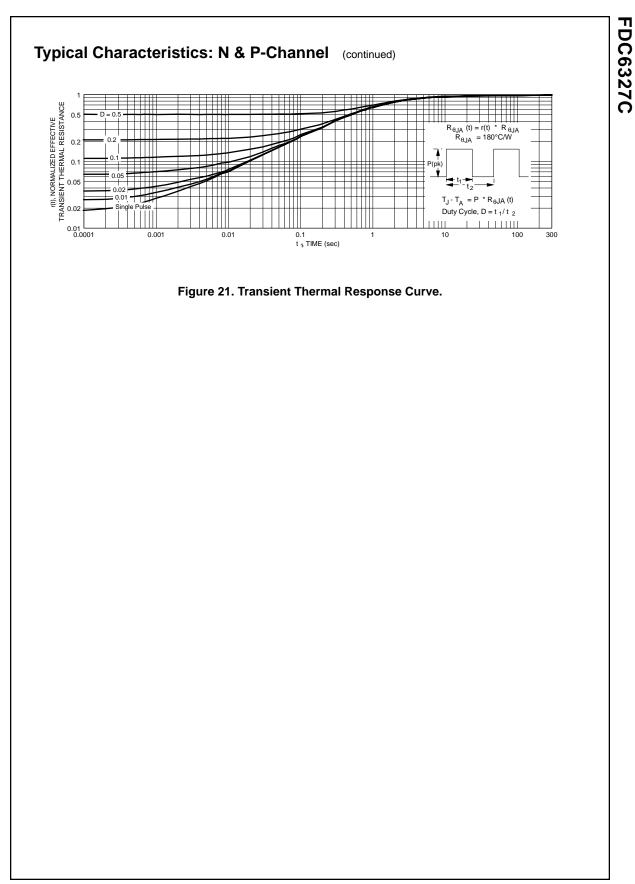
VodeVode10 V, ID1 A, VGSP-Ch714trTurn-On Rise TimeVGS4.5V, RGEN6 Ω N-Ch918nstd(off)Turn-Off Delay TimeP-ChannelVDD-10 V, ID-1 A, VDDN-Ch1222nstd(off)Turn-Off Fall TimeVGS-4.5 V, RGEN6 Ω N-Ch1425N-ChQgTotal Gate ChargeN-ChannelVDS-4.5 V, RGENN-Ch3.254.5nCQgsGate-Source ChargeN-ChannelVDS10 V, ID-1.9 A, VGS-4.5 VN-Ch0.65nCQgdGate-Drain ChargeVDS-10 V, ID-1.9 A, VGS-4.5 VN-Ch0.65nCDrain-Source Diode Characteristics and Maximum RatingsIsMaximum Continuous Drain-Source Diode ForwardVGS0.8 AN-Ch0.761.2VVSDDrain-Source Diode ForwardVGS0.8 A(Note 2)N-Ch0.761.2VVGS0.13 Qg0.761.2VVGS0.761.2VVVoltageVGS0.7 IS0.8 A(Note 2)N-Ch0.761.2VVotes:: R ₈₄ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
$t_{d(on)}$ Turn-On Delay TimeN-ChannelN-ChannelN-Ch515ns $V_{DD} = 10 V$, $I_D = 1 A$, $V_{GS} = 4.5V$, $R_{GEN} = 6 \Omega$ N-Ch918ns $t_{d(off)}$ Turn-On Rise TimeP-ChannelN-Ch1222ns $t_{d(off)}$ Turn-Off Fall TimeP-ChannelN-Ch1222ns $V_{DD} = -10 V$, $I_D = -1 A$, $V_{DD} = -10 V$, $I_D = -1 A$, $V_{DS} = -10 V$, $I_D = -1 A$, $P-Ch$ N-Ch1425 t_r Turn-Off Fall TimeV_GS = -4.5 V, $R_{GEN} = 6 \Omega$ N-Ch39ns Q_g Total Gate ChargeN-Channel $V_{DS} = 10 V$, $I_D = 2.7 A$, $V_{GS} = 4.5 V$ N-Ch3.254.5nC Q_{gs} Gate-Source ChargeP-ChannelN-Ch0.665nCP-Ch0.665nC Q_{gd} Gate-Drain Charge $V_{nS} = -10 V$, $I_D = -1.9 A$, $V_{GS} = -4.5 V$ N-Ch0.65nC $D_{rain-Source Diode Characteristics and Maximum RatingsIsMaximum Continuous Drain-Source Diode Forward CurrentN-Ch0.761.2VV_{SD}Drain-Source Diode ForwardV_{GS} = 0 V, I_S = -0.8 A (Note 2)N-Ch0.761.2VV_{SD}Drain-Source Diode ForwardV_{GS} = 0 V, I_S = -0.8 A (Note 2)N-Ch0.761.2VV_{SD}Drain-Source Diode ForwardV_{GS} = 0 V, I_S = -0.8 A (Note 2)N-Ch0.761.2VV_{SD}Drain-Meined by design while R_{0A} is determined by the user'$	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Switchir	ng Characteristics (Note	2)					
tr Turn-On Rise Time $V_{GS} = 4.5V$, $R_{GEN} = 6 \Omega$ N-Ch 9 18 ns $t_{d(off)}$ Turn-Off Delay Time P-Channel N-Ch 14 25 N-Ch 16 14 25 N-Ch 16 16 16 16 16 16 16 16 16 16 16 <td>Rr Turn-On Rise Time $V_{GS} = 4.5V$, $R_{GEN} = 6 \Omega$ N-Ch 9 18 ns Rd(df) Turn-Off Delay Time P-Channel N-Ch 12 22 ns Rd(df) Turn-Off Delay Time V_{GS} = -10 V, I_D = -1 A, N-Ch 14 25 ns Rd Turn-Off Fall Time V_{GS} = -4.5 V, R_{GEN} = 6 Ω N-Ch 14 25 ns Qag Total Gate Charge N-Channel V_{DS} = 10 V, I_D = 2.7 A, V_{GS} = 4.5 V N-Ch 3 9 ns Qag Gate-Source Charge P-Ch 14 25 nc N-Ch 3.8 9 ns Qag Gate-Drain Charge N-Channel N-Ch 0.65 nC P-Ch 2.85 4.0 N-Ch 0.68 nc N-Ch 0.68 nc N-Ch 0.68 nc N-Ch 0.68 nc N-Ch 0.68 N-Ch N-Ch</td> <td></td> <td>-</td> <td>N-Channel</td> <td>_</td> <td></td> <td></td> <td></td> <td>ns</td>	Rr Turn-On Rise Time $V_{GS} = 4.5V$, $R_{GEN} = 6 \Omega$ N-Ch 9 18 ns Rd(df) Turn-Off Delay Time P-Channel N-Ch 12 22 ns Rd(df) Turn-Off Delay Time V _{GS} = -10 V, I _D = -1 A, N-Ch 14 25 ns Rd Turn-Off Fall Time V _{GS} = -4.5 V, R _{GEN} = 6 Ω N-Ch 14 25 ns Qag Total Gate Charge N-Channel V _{DS} = 10 V, I _D = 2.7 A, V _{GS} = 4.5 V N-Ch 3 9 ns Qag Gate-Source Charge P-Ch 14 25 nc N-Ch 3.8 9 ns Qag Gate-Drain Charge N-Channel N-Ch 0.65 nC P-Ch 2.85 4.0 N-Ch 0.68 nc N-Ch 0.68 nc N-Ch 0.68 nc N-Ch 0.68 nc N-Ch 0.68 N-Ch		-	N-Channel	_				ns
d(off)Turn-Off Delay TimeP-ChannelN-Ch1222ns t_{bb} Turn-Off Fall Time V_{bb} = -10 V, I_{b} = -1 A,N-Ch1425N-Ch Ω_{g} Total Gate ChargeN-Channel V_{cs} = 0.0N-Ch3.9ns Ω_{gs} Gate-Source ChargeN-Channel V_{bs} 10 V, I_{b} = 2.7 A, V_{Gs} 9-Ch2.854.0 Ω_{gs} Gate-Source ChargeN-Channel V_{bs} 10 V, I_{b} = 2.7 A, V_{Gs} 9-Ch2.854.0 Ω_{gd} Gate-Drain Charge V_{bs} = 10 V, I_{b} = 1.9 A, V_{Gs} = -4.5 VN-Ch0.65nC Ω_{gd} Gate-Drain Charge V_{bs} = 10 V, I_{b} = -1.9 A, V_{Gs} = -4.5 VN-Ch0.66nC D_{rain} -Source Diode Characteristics and Maximum RatingssMaximum Continuous Drain-Source Diode Forward CurrentN-Ch0.761.2V V_{Sb} Drain-Source Diode Forward V_{Gs} 0.7 I_{b}-0.79-1.2VVoltage V_{ds} 0.7 I_{b} 0.8 A (Note 2)N-Ch0.761.2V V_{ab} is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pinsR _{Auc} is quaranteed by design while R _{buh} is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energically.a) 130 "C/W when mounted on a 0.125 in" pad of 2 oz. copper. <t< td=""><td>$\begin{array}{c c c c c c c c c c c c c c c c c c c$</td><td>r</td><td>Turn-On Rise Time</td><td></td><td>N-Ch</td><td></td><td>9</td><td>18</td><td>ns</td></t<>	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	r	Turn-On Rise Time		N-Ch		9	18	ns
Image: stress of the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins N=Ch 3 9 ns R_{auc} Total Gate Charge N=Channel N=Ch 3 3 9 ns Q_{gs} Gate-Source Charge N=Channel N=Ch 3 2.85 4.0 N=Ch Q_{gs} Gate-Drain Charge P=Channel N=Ch 0.65 nC Q_{gd} Gate-Drain Charge N=S N=Ch 0.65 nC Q_{gd} Gate-Drain Charge N=S N=Ch 0.65 nC Q_{gd} Gate-Drain Charge N=S N=Ch 0.65 nC D_{gd} Gate-Drain Charge V_S N=S N=Ch 0.65 nC Q_{gd} Gate-Drain Charge V_S N=S N=Ch 0.68 nC S Maximum Continuous Drain-Source Diode Forward Current N=Ch 0.65 0.76 1.2 V S_{SD} Drain-Source Diode Forward V_{GS} 0 N=S 0.76 1.2 V	Image: second secon	d(off)	Turn-Off Delay Time		N-Ch		12	22	ns
Ω_{gg} Total Gate Charge N-Channel N-Channel N-Ch 3.25 4.5 nC Ω_{gg} Gate-Source Charge P-Channel P-Channel N-Ch 2.85 4.0 nC Ω_{gd} Gate-Drain Charge P-Channel N-Ch 0.68 nC Ω_{gd} Gate-Drain Charge V _{DS} = -10 V, I _D = -1.9 A, V _{GS} = -4.5V N-Ch 0.65 nC Drain-Source Diode Characteristics and Maximum Ratings Maximum Continuous Drain-Source Diode Forward Current N-Ch 0.8 A V_{SD} Drain-Source Diode Forward $V_{GS} = 0$ V, $I_S = 0.8$ A (Note 2) N-Ch 0.76 1.2 V V_{SD} Drain-Source Diode Forward $V_{GS} = 0$ V, $I_S = -0.8$ A (Note 2) N-Ch 0.76 1.2 V $V_{GS} = 0$ V, $I_S = -0.8$ A (Note 2) N-Ch 0.76 1.2 V $V_{GS} = 0$ V, $I_S = -0.8$ A (Note 2) N-Ch 0.79 -1.2 V $v_{GS} = 0$ V, $I_S = -0.8$ A (Note 2) N-Ch 0.79 -1.2 V 0.65 0.79 -1.2 V $v_{GS} = 0$ $V_{GS} = 0$ $V_{$	Q_g Total Gate Charge N-Channel N-Channel N-Ch 3.25 4.5 nC Q_{gs} Gate-Source Charge P-Channel P-Channel N-Ch 3.25 4.0 nC Q_{gd} Gate-Drain Charge N-Ch annel N-Ch 0.65 nC P_{ch} 0.65 nC 0.68 nC Q_{gd} Gate-Drain Charge N-Ch annel 0.68 nC P_{ch} 0.68 nC 0.68 nC P_{ch} 0.68 nC 0.68 nC Q_{gd} Gate-Drain Charge $V_{sp} = -1.9 \text{ A}, V_{GS} = -4.5 \text{ V}$ $N-Ch$ 0.68 nC $Drain-Source Diode Characteristics and Maximum Ratings N-Ch 0.68 A -0.8 A V_{SD} Drain-Source Diode Forward V_{GS} = 0 \text{ V}, I_S = 0.8 \text{ A} (Note 2) N-Ch 0.76 1.2 V Voltage O V, I_S = 0.8 \text{ A} (Note 2) P-Ch 0.76 1.2 V V_{as} is guaranteed by design while R_{atA} is determined by the user's board design. Both devices are assumed to be operating and s$	f	Turn-Off Fall Time		N-Ch		3	9	ns
Ω_{gs} Gate-Source Charge P-Channel N-Ch 0.65 nC Ω_{gd} Gate-Drain Charge P-Channel N-Ch 0.65 nC Ω_{gd} Gate-Drain Charge P-Channel N-Ch 0.65 nC Drain-Source Diode Characteristics and Maximum Ratings N-Ch 0.90 nC s Maximum Continuous Drain-Source Diode Forward Current N-Ch 0.76 0.8 A V_{SD} Drain-Source Diode Forward $V_{GS} = 0$ V, $I_S = 0.8$ A (Note 2) N-Ch 0.76 1.2 V Voltage Voltage V _{GS} = 0 V, $I_S = 0.8$ A (Note 2) N-Ch 0.76 1.2 V $V_{GS} = 0$ V, $I_S = 0.8$ A (Note 2) N-Ch 0.76 1.2 V Voltage 0 V, $I_S = 0.8$ A (Note 2) P-Ch 0.79 -1.2 V $N=Ch$ 0.76 1.2 V $V_{GS} = 0$ V, $I_S = 0.8$ A (Note 2) N-Ch 0.76 1.2 V $N=0$ 0.90 0.76 0.76 0.2 0.76 0.76 0.79 0.79 0.79 0.79 0.79	Ω_{gg} Gate-Source Charge P-Channel N-Ch 0.65 nC Ω_{gd} Gate-Drain Charge P-Channel N-Ch 0.65 nC Ω_{gd} Gate-Drain Charge P-Channel N-Ch 0.65 nC Drain-Source Diode Characteristics and Maximum Ratings N-Ch 0.65 nC s Maximum Continuous Drain-Source Diode Forward Current N-Ch 0.76 1.2 V Vsp Drain-Source Diode Forward V_{GS} = 0 V, I_S = 0.8 A (Note 2) N-Ch 0.76 1.2 V Vsp Drain-Source Diode Forward V_{GS} = 0 V, I_S = 0.8 A (Note 2) N-Ch 0.76 1.2 V Voltage OV, I_S = 0.8 A (Note 2) N-Ch 0.76 1.2 V R_{add} is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R R_{add} is guaranteed by design while R_{adA} is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energe equally. $M_{add} = 0.205$ $M_{add} = 0.205$ $M_{add} = 0.205$ $M_{add} = 0.2005$ $M_{add} = 0.2005$ $M_{add} = 0.2005$ M_{a	Qg	Total Gate Charge		N-Ch		3.25	4.5	nC
D_{gd} Gate-Drain Charge $V_{DS} = -10 \text{ V}, I_D = -1.9 \text{ A}, V_{GS} = -4.5 \text{ V}$ $N-Ch$ 0.90 0.90 nC Drain-Source Diode Characteristics and Maximum Ratings N-Ch 0.8 A S Maximum Continuous Drain-Source Diode Forward Current N-Ch 0.8 A V_{SD} Drain-Source Diode Forward $V_{GS} = 0 \text{ V}, I_S = 0.8 \text{ A}$ (Note 2) N-Ch 0.76 1.2 V V_{SD} Drain-Source Diode Forward $V_{GS} = 0 \text{ V}, I_S = 0.8 \text{ A}$ (Note 2) N-Ch 0.76 1.2 V otest: R _{9.0} is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins $R_{9.4}$ is guaranteed by design while $R_{9.4}$ is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally. $M_{equally}$ $M_{equally$	Ω_{gd} Gate-Drain Charge $V_{DS} = -10 \text{ V}, I_D = -1.9 \text{ A}, V_{GS} = -4.5 \text{V}$ $N-Ch$ 0.00 nC Drain-Source Diode Characteristics and Maximum Ratings Maximum Continuous Drain-Source Diode Forward Current N-Ch 0.8 A S Maximum Continuous Drain-Source Diode Forward VGS $N-Ch$ 0.76 1.2 V Vsp Drain-Source Diode Forward VGS $V_{GS} = 0 \text{ V}, I_S = 0.8 \text{ A}$ $(Note 2)$ $N-Ch$ 0.76 1.2 V Vsp Drain-Source Diode Forward VGS $V_{GS} = 0 \text{ V}, I_S = 0.8 \text{ A}$ $(Note 2)$ $N-Ch$ 0.76 1.2 V Vsp Drain-Source Diode Forward VGS $V_{GS} = 0 \text{ V}, I_S = -0.8 \text{ A}$ $(Note 2)$ $N-Ch$ 0.76 1.2 V Voltage $V_{VGS} = 0 \text{ V}, I_S = -0.8 \text{ A}$ $(Note 2)$ $P-Ch$ 0.76 1.2 V Revelop is guaranteed by design while Rule is a case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{P,C}$ 0.76 0.12 0.007 0.007 0.007 0.007 0.007 0.007 0.007 0.007 0.0007 <	Q _{gs}	Gate-Source Charge		N-Ch		0.65	4.0	nC
Drain-Source Diode Characteristics and Maximum Ratings s Maximum Continuous Drain-Source Diode Forward Current N-Ch 0.8 A Vsp Drain-Source Diode Forward VGS = 0 V, IS = 0.8 A (Note 2) N-Ch 0.76 1.2 V otest Red is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins Red is guaranteed by design while Red is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally. Image: the number of the index on a 0.125 in ² pad of 2 oz. copper. b) 140 °C/W when mounted on a 0.005 in ² pad of 2 oz. copper. c) 180 °C/W when mounted on a 0.0015 in ² pad of 2 oz. copper.	Drain-Source Diode Characteristics and Maximum Ratings s Maximum Continuous Drain-Source Diode Forward Current N-Ch 0.8 A V _{SD} Drain-Source Diode Forward V _{GS} = 0 V, I _S = 0.8 A (Note 2) N-Ch 0.76 1.2 V Voltage V _{GS} = 0 V, I _S = -0.8 A (Note 2) P-Ch -0.79 -1.2 V otes: R _{elA} is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R _{elA} is guaranteed by design while R _{elA} is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energically. Image: a subject of the distingt of the distipated on a 0.005 in ² pad of 2 oz. copper. a) 130 °C/W when mounted on a 0.125 in ² pad of 2 oz. copper. b) 140 °C/W when mounted on a 0.005 in ² pad of 2 oz. copper. c) 180 °C/W when mounted on a 0.0015 in ² pad of 2 oz. copper. Scale 1 : 1 on letter size paper Scale 1 : 1 on letter size paper b) 140 °C/W when mounted on a 0.005 in ² pad of 2 oz. copper. c) 180 °C/W when mounted on a 0.0015 in ² pad of 2 oz. copper.	Q _{gd}	Gate-Drain Charge		N-Ch		0.90		nC
s Maximum Continuous Drain-Source Diode Forward Current N-Ch 0.8 A V _{SD} Drain-Source Diode Forward V _{GS} = 0 V, I _S = 0.8 A (Note 2) N-Ch 0.76 1.2 V V _{SD} Drain-Source Diode Forward V _{GS} = 0 V, I _S = -0.8 A (Note 2) N-Ch 0.76 1.2 V otes: R _{0JA} is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins R _{0JC} is guaranteed by design while R _{0JA} is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally. Image: the sum of the junction to case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins R _{0JA} is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally. Image: the sum of the junction to a 0.125 in ² pad of 2 oz. copper. Image: the sum of the operating and sharing the dissipated heat energy equally.	s Maximum Continuous Drain-Source Diode Forward Current N-Ch 0.8 A Vsb Drain-Source Diode Forward V _{GS} = 0 V, I _S = 0.8 A (Note 2) N-Ch 0.76 1.2 V Vsb Voltage V _{GS} = 0 V, I _S = 0.8 A (Note 2) N-Ch 0.776 1.2 V voltage V _{GS} = 0 V, I _S = -0.8 A (Note 2) N-Ch 0.79 -1.2 V otes: Reux is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Reux is guaranteed by design while Reux is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally. Image: the sum of the junction and 0.125 in² pad of 2 oz. copper. a) 130 °C/W when mounted on a 0.0125 in² pad of 2 oz. copper. b) 140 °C/W when mounted on a 0.005 in² pad of 2 oz. copper. c) 180 °C/W when mounted on a 0.0015 in² pad of 2 oz. copper. Scale 1 : 1 on letter size paper Scale 1 : 1 on letter size paper b) 140 °C/W when mounted on a 0.125 in² c) 180 °C/W when mounted on a 0.0015 in²				1 011		0.00	1	
VSD Drain-Source Diode Forward VGS = 0 V, IS = 0.8 Å (Note 2) N-Ch 0.76 1.2 V otes: : R _{0JA} is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins R _{0JC} is guaranteed by design while R _{0JA} is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally. Image: the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins R _{0JC} is guaranteed by design while R _{0JA} is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally. Control of the drain pins R _{0JC} is guaranteed by design while R _{0JA} is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally. Image: the sum of the junction to case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins R _{0JC} is guaranteed by design while R _{0JA} is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally. Image: the sum of the junction to case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins R _{0JC} is guaranteed by design while R _{0JA} is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equality. Image: the surface of the drain pins R _{0JA} is determined by the u	VSD Drain-Source Diode Forward $V_{GS} = 0 V$, $I_S = 0.8 A$ (Note 2) N-Ch 0.76 1.2 V otes: Re _{0.14} is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Re _{0.16} is guaranteed by design while Re _{0.14} is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally. a) 130 °C/W when mounted on a 0.125 in ² pad of 2 oz. copper. b) 140 °C/W when mounted on a 0.005 in ² pad of 2 oz. copper. c) 180 °C/W when mounted on a 0.0015 in ² pad of 2 oz. copper. Scale 1 : 1 on letter size paper Scale 1 : 1 on letter size paper Image: Comparison of the size paper Image: Comparison of the size paper Image: Comparison of the size paper			-					Α
otes: : R _{BJA} is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins R _{BJA} is guaranteed by design while R _{BJA} is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally. a) 130 °C/W when mounted on a 0.125 in ² pad of 2 oz. copper. b) 140 °C/W when mounted on a 0.005 in ² pad of 2 oz. copper.	otes: :: R _{0,JA} is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R _{0,LC} is guaranteed by design while R _{0,JA} is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally. Image: a structure of the distribution	V _{SD}			N-Ch			1.2	V
600			a) 130 °C/W when mounted on a 0.125 in ²	mounted on a 0.005 in ² pad of 2 oz. copper.	Q		moun	ted on a 0.0	











TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACExTM BottomlessTM CoolFETTM CROSSVOLTTM DOMETM E²CMOSTM EnSignaTM FACT T^M FACT Quiet SeriesTM FAST[®]

FASTr[™] GlobalOptoisolator[™] GTO[™] HiSeC[™] ISOPLANAR[™] MICROWIRE[™] OPTOLOGIC[™] OPTOPLANAR[™] POP[™] PowerTrench[®] QFET[™] QS[™] QT Optoelectronics[™] Quiet Series[™] SuperSOT[™]-3 SuperSOT[™]-6 SuperSOT[™]-8 SyncFET[™] TinyLogic[™] UHC[™] VCX™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user. 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.
		that has been discontinued by Fairchild semicond