Re-Configurable 6 Output PECL Oscillator

Series CCE6RE

Electrical Characteristics

	Description	Conditions	Min	Typ	Max	Unit
Ioh	Output High Current	Voh = (L)Vdd - 0.5, (L)Vdd = 3.3 V	12	24		mA
Iol	Output Low Current	Vol = .5, (L)Vdd = 3.3 V	12	24		mA
Vih	High Level Input Voltage	CMOS levels, % of Vdd	0.7			V
Vil	Low-Level Input Voltage	CMOS levels, % of Vdd			0.3	V
Iih	Input High Current	Vin = AVdd - 0.3 V		<1	10	µA
Iil	Input Low Current	Vin = + 0.3 V		<1	10	µA
Ioz	Output Leakage Current	tri-state outputs			10	µA
Idd	Total Power Supply Current	Example 1: 1 PECL output @155.52 MHz 1 CMOS output @19.44 MHz 1 CMOS output @38.88 MHz 1 CMOS output @77.76 MHz 1 CMOS output @12 MHz Example 2: 1 PECL output @400 MHz 1 CMOS output @106.25 MHz 1 CMOS output @200 MHz 1 CMOS output @100 MHz 1 CMOS output @12 MHz		29 59		mA mA
Idds	Shutdown Power Supply Curr	Shutdown active		5	20	µA

Output Clock Switching Characteristics

	Description	Conditions	Min	Typ	Max	Unit
1/t1	Output Frequency	Clock output limit, CMOS, Commercial Clock output limit, PECL, Commercial	0.2 100		200 400	MHz MHz
t3	Rising Edge Slew Rate	Output clock rise time, 20% – 80% Vdd	0.75	1.4		nS
t4	Falling Edge Slew Rate	Output clock fall time, 20% – 80% Vdd	0.75	1.4		nS
t5	Output tri-state timing after SD/OE switches	Time for output to enter/leave tri-state mode		150	300	nS
t6	Clock Jitter measured at Vdd/2	Peak-to-Peak period jitter, CLK outputs		200		pS
v7	P+/P- Crossing Point	Crossing point ref. to Vdd/2, bal res. net	-0.2	0	0.2	V
	Frequency Switch Time	Change time		2	4	ms

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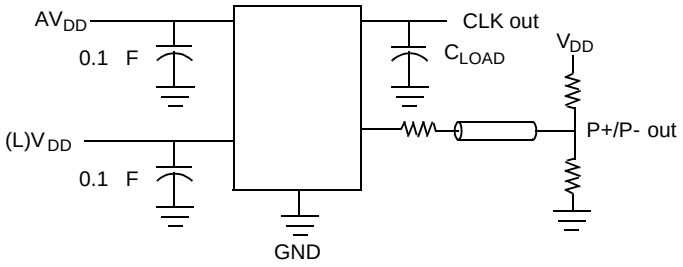
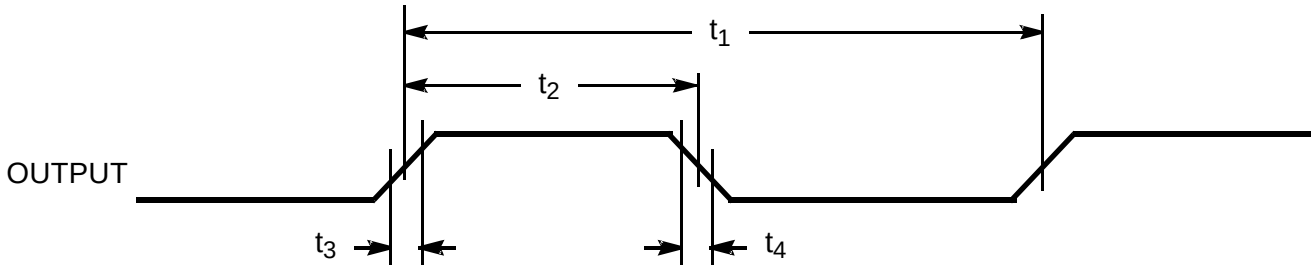
Rev: M-090414-14

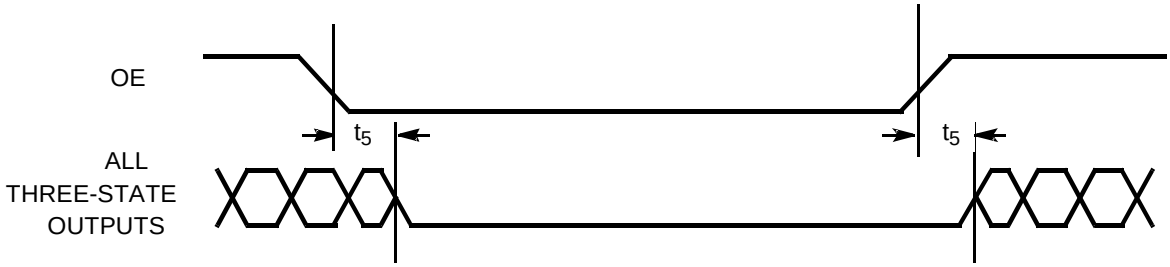
TEST CIRCUIT



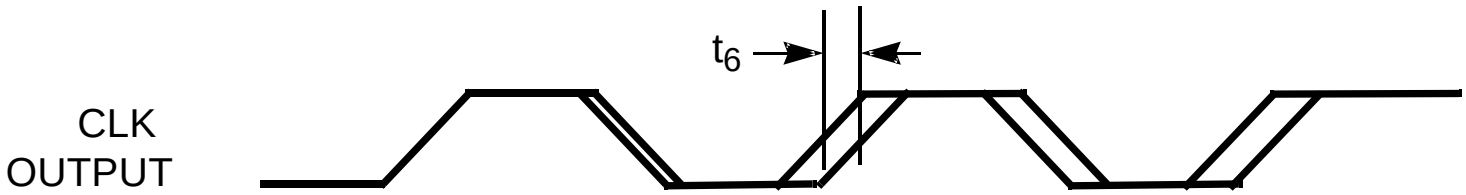
ALL OUTPUTS, DUTY CYCLE, RISE/FALL TIME



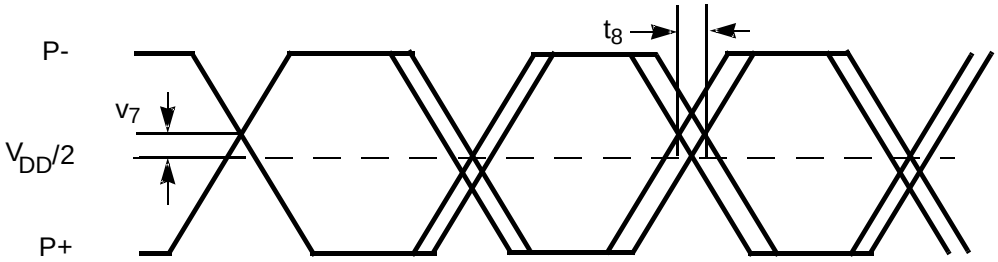
OUTPUT TRI-STATE TIMING



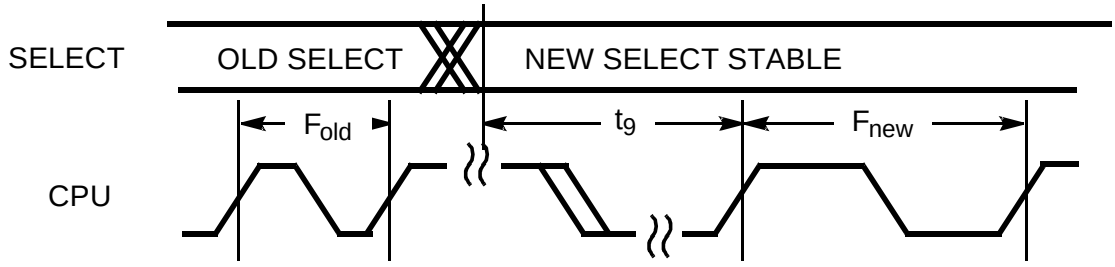
CLK OUTPUT JITTER



P+/P- CROSSING POINT AND JITTER



CPU FREQUENCY CHANGE



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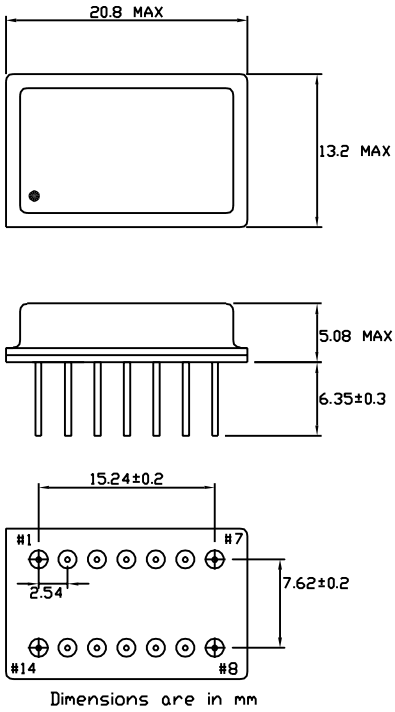
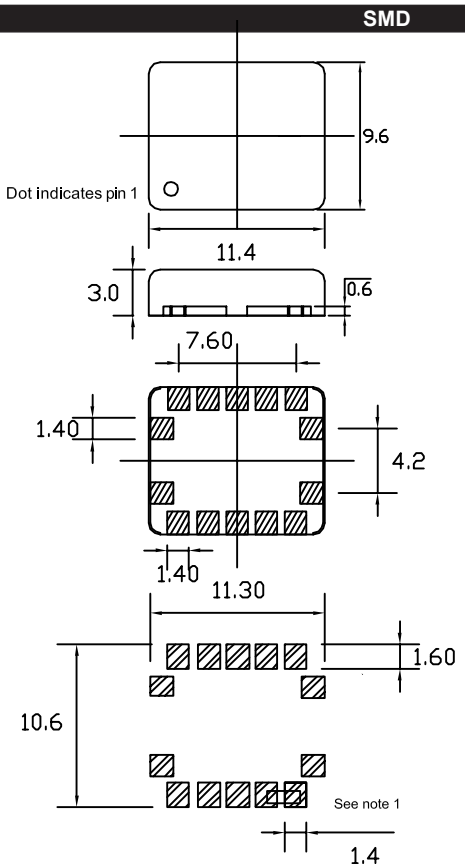
DIP



PIN FUNCTION
PIN 1 OE (CONNECT TO VDD)
PIN 2 SUSPEND (CONNECT TO GND)
PIN 3 VDD
PIN 4 CLK C OUTPUT
PIN 5 CONNECT TO PIN 6
PIN 6 CONNECT TO PIN 5
PIN 7 GND
PIN 8 12 MHz REF CLOCK OUTPUT
PIN 9 PECL - OUTPUT
PIN10 PECL + OUTPUT
PIN 11 SDAT
PIN 12 SCLK
PIN 13 CLK A OUTPUT
PIN 14 CLK B OUTPUT

SMD



PIN FUNCTION
PIN 1 FACTORY USE (MAKE NO CONNECTION)
PIN 2 OE
PIN 3 VDD
PIN 4 CLK C OUTPUT
PIN 5 CONNECT TO PIN 6
PIN 6 CONNECT TO PIN 5
PIN 7 GND
PIN 8 12 MHz REF CLOCK OUTPUT
PIN 9 PECL - OUTPUT
PIN10 PECL + OUTPUT
PIN 11 SCLK
PIN 12 SDAT
PIN 13 CLK A OUTPUT
PIN 14 CLK B OUTPUT

Dimensions in mm
Recommended solder pad layout

Note1:
For proper operation pin 5 must be connected to pin 6

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Flash Programmability:

Non-Volatile programming enables easy customization, ultrafast turnaround, performance tweaking, design timing margin testing, inventory control, lower part count, and more secure product supply. In addition, any part in the family can also be programmed multiple times, which reduces programming errors and provides an easy upgrade path for existing designs.

Feature of the I²C-bus:

- Only two bus lines are required; a serial data line (SDA) and a serial clock line (SCL)
- Each device connected to the bus is software addressable by a unique address and simple master/slave relationship exist at all times; master can operate as a master- transmitter or as master-receivers
- It's a true multi-master bus including collision detection and arbitration to prevent data corruption if two or more master simultaneously initiate data transfer
- Serial 8-bit oriented, bidirectional data transfers can be made at up to 100 Kbit/s in the standard mode, up to 400 kbit/s in the fast-mode, or up to 3.4 Mbit/s in the High-speed mode

Designer Benefits:

I²C bus compatible In Circuit Reconfigurable Oscillator "ICRO" allow a system design to rapidly progress directly from a functional block diagram to a prototype. Moreover, since they 'clip' directly onto the I²C bus without any additional external interfacing, they allow a prototype system to be modified or upgraded simply by 'clipping' or 'unclipping' ICRO to or from the bus.

Here are some of the feature of I²C- bus compatible ICRO which are particularly attractive to designer

- Functional blocks on the block diagram correspond with the actual ICRO designs proceed rapidly from block diagram to final schematic
- No need to design bus interfaces because the I²C-bus interface is already integrated on the ICRO
- Integrated addressing and data-transfer protocol allow systems to be completely software-defined
- The same ICRO types can often be used in many different applications
- Design-time reduces as designers quickly become familiar with the frequently used functional book represented by I²C-bus compatible and ICRO
- ICRO can be added to or remove from system without affecting any other circuits on the bus

In addition to these advantages, the CMOS ICRO in the I²C-bus compatible range offer designers special feature which are particularly attractive for portable equipment and battery-backed systems.

They All Have:

- Extremely low current consumption
- High Noise immunity
- Wide operating temperature range

Manufacturer Benefits

I²C-bus compatible ICRO don't only assist designer, they also give a wider range of benefits to the equipment manufacturer because:

- The simple 2-wire serial I²C bus minimizes interconnections so ICRO have fewer pins and there are not so many PCB tracks; result- smaller and less expensive PCBs
- The completely integrated I²C-bus protocol eliminates the need for address decoders and other 'glue logic'
- The multi-master capability of the I²C-bus allows rapid testing and alignment of end-user equipment via external connections to an assembly line
- I²C-bus handbook, I²C Website: www.semiconductors.philips.com/I2C