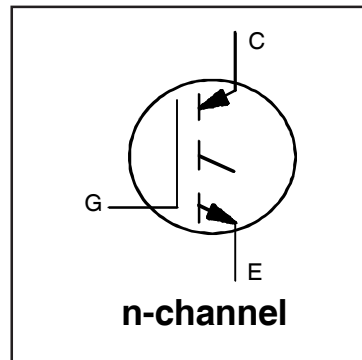


**IRG7PH46UPbF**  
**IRG7PH46U-EP**

**INSULATED GATE BIPOLAR TRANSISTOR**

**Features**

- Low  $V_{CE(ON)}$  trench IGBT technology
- Low switching losses
- Maximum junction temperature 175 °C
- Square RBSOA
- 100% of the parts tested for  $I_{LM}$
- Positive  $V_{CE(ON)}$  temperature co-efficient
- Tight parameter distribution
- Lead-Free



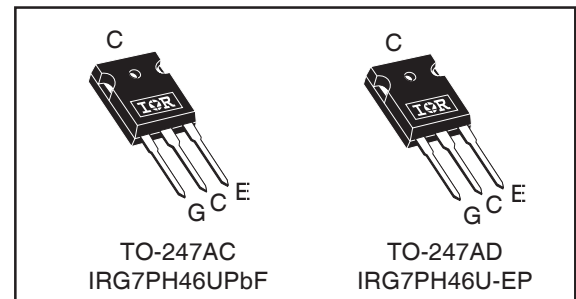
$V_{CES} = 1200V$
$I_C = 75A, T_C = 100^\circ C$
$T_{J(max)} = 175^\circ C$
$V_{CE(on)} \text{ typ.} = 1.7V$

**Benefits**

- High efficiency in a wide range of applications
- Suitable for a wide range of switching frequencies due to low  $V_{CE(ON)}$  and low switching losses
- Rugged transient performance for increased reliability
- Excellent current sharing in parallel operation

**Applications**

- U.P.S
- Welding
- Solar inverter
- Induction heating



<b>G</b>	<b>C</b>	<b>E</b>
Gate	Collector	Emitter

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{CES}$	Collector-to-Emitter Voltage	1200	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current (Silicon Limited)	130 <sup>Ⓞ</sup>	A
$I_C @ T_C = 100^\circ C$	Continuous Collector Current (Silicon Limited)	75	
$I_{NOMINAL}$	Nominal Current	40	
$I_{CM}$	Pulse Collector Current, $V_{GE} = 15V$	120	
$I_{LM}$	Clamped Inductive Load Current, $V_{GE} = 20V$ ①	160	
$V_{GE}$	Continuous Gate-to-Emitter Voltage	±30	V
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	469	W
$P_D @ T_C = 100^\circ C$	Maximum Power Dissipation	234	
$T_J$	Operating Junction and	-55 to +175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 sec.		
	Mounting Torque, 6-32 or M3 Screw	10 lbf-in (1.1 N-m)	

**Thermal Resistance**

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$ (IGBT)	Thermal Resistance Junction-to-Case-(each IGBT) TO-247AC ④	—	—	0.32	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink (flat, greased surface) ④	—	0.24	—	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (typical socket mount)	—	40	—	

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

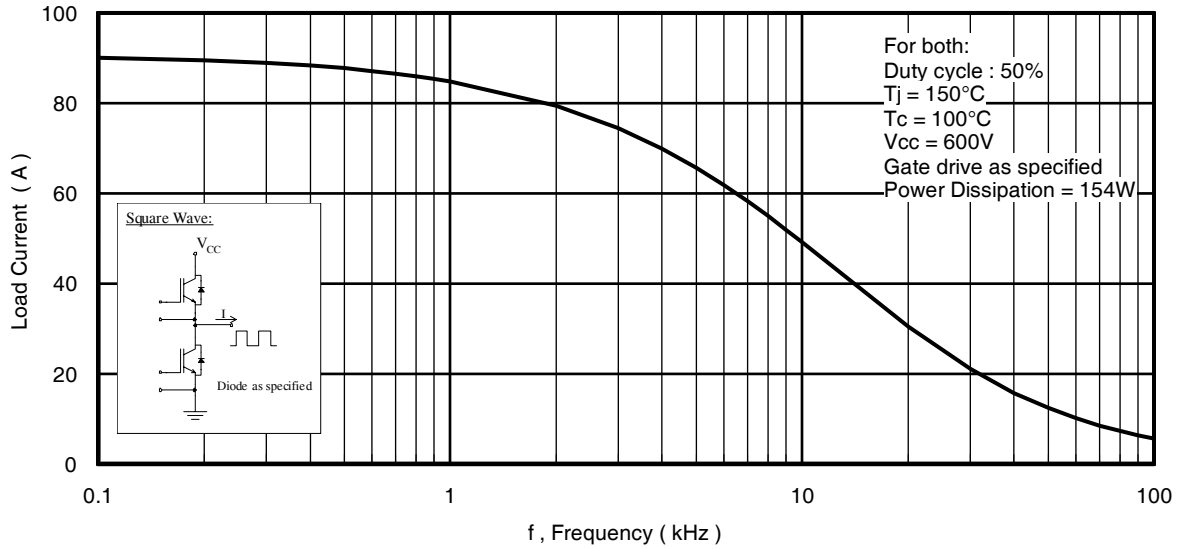
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	$V_{GE} = 0V, I_C = 100\mu A$ ③
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	1.2	—	V/°C	$V_{GE} = 0V, I_C = 1mA$ (25°C-150°C) ③
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.7	2.0	V	$I_C = 40A, V_{GE} = 15V, T_J = 25^\circ\text{C}$ ②
		—	2.0	—		$I_C = 40A, V_{GE} = 15V, T_J = 150^\circ\text{C}$ ②
		—	2.1	—		$I_C = 40A, V_{GE} = 15V, T_J = 175^\circ\text{C}$ ②
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0	V	$V_{CE} = V_{GE}, I_C = 1.6mA$
$\Delta V_{GE(th)}/\Delta T_J$	Threshold Voltage temp. coefficient	—	-15	—	mV/°C	$V_{CE} = V_{GE}, I_C = 1.6mA$ (25°C - 175°C)
$g_{fe}$	Forward Transconductance	—	60	—	S	$V_{CE} = 50V, I_C = 40A, PW = 20\mu s$
$I_{CES}$	Collector-to-Emitter Leakage Current	—	1	100	$\mu A$	$V_{GE} = 0V, V_{CE} = 1200V$
		—	1170	—		$V_{GE} = 0V, V_{CE} = 1200V, T_J = 175^\circ\text{C}$
$I_{GES}$	Gate-to-Emitter Leakage Current	—	—	$\pm 200$	nA	$V_{GE} = \pm 30V$

## Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

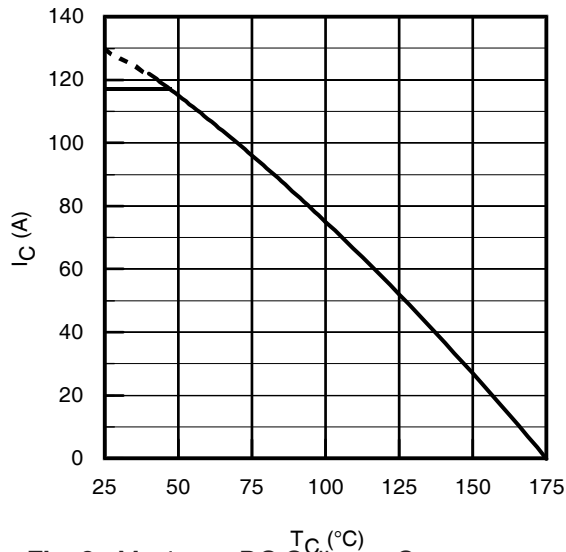
	Parameter	Min.	Typ.	Max.	Units	Conditions
$Q_g$	Total Gate Charge (turn-on)	—	220	320	nC	$I_C = 40A$ ② $V_{GE} = 15V$ $V_{CC} = 600V$
$Q_{ge}$	Gate-to-Emitter Charge (turn-on)	—	30	50		
$Q_{gc}$	Gate-to-Collector Charge (turn-on)	—	85	130		
$E_{on}$	Turn-On Switching Loss	—	2560	3460	$\mu J$	$I_C = 40A, V_{CC} = 600V, V_{GE} = 15V$ ② $R_G = 10\Omega, L = 200\mu H, T_J = 25^\circ\text{C}$ Energy losses include tail & diode reverse recovery
$E_{off}$	Turn-Off Switching Loss	—	1780	2660		
$E_{total}$	Total Switching Loss	—	4340	6120		
$t_{d(on)}$	Turn-On delay time	—	45	65	ns	Diode clamp the same as IRG7PH46UDPbF
$t_r$	Rise time	—	40	55		
$t_{d(off)}$	Turn-Off delay time	—	410	445		
$t_f$	Fall time	—	45	65		
$E_{on}$	Turn-On Switching Loss	—	3950	—	$\mu J$	$I_C = 40A, V_{CC} = 600V, V_{GE} = 15V$ ② $R_G = 10\Omega, L = 200\mu H, T_J = 175^\circ\text{C}$ Energy losses include tail & diode reverse recovery
$E_{off}$	Turn-Off Switching Loss	—	3020	—		
$E_{total}$	Total Switching Loss	—	6970	—		
$t_{d(on)}$	Turn-On delay time	—	40	—	ns	Diode clamp the same as IRG7PH46UDPbF
$t_r$	Rise time	—	40	—		
$t_{d(off)}$	Turn-Off delay time	—	480	—		
$t_f$	Fall time	—	220	—		
$C_{ies}$	Input Capacitance	—	4820	—	pF	$V_{GE} = 0V$ $V_{CC} = 30V$ $f = 1.0MHz$
$C_{oes}$	Output Capacitance	—	150	—		
$C_{res}$	Reverse Transfer Capacitance	—	110	—		
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				$I_C = 160A$ $V_{CC} = 960V, V_p = 1200V$ $R_g = 10\Omega, V_{GE} = +20V \text{ to } 0V, T_J = 175^\circ\text{C}$

### Notes:

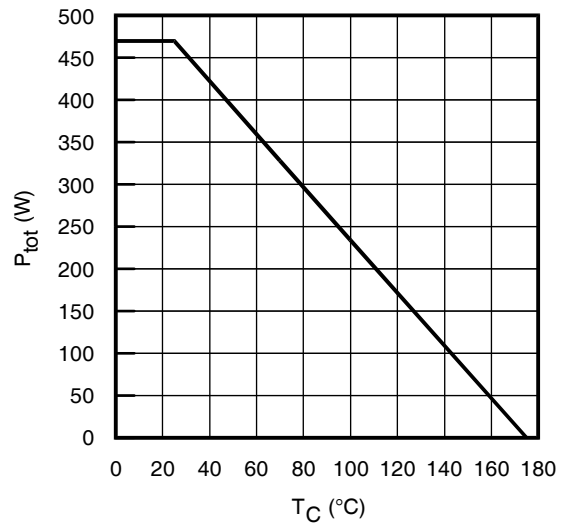
- ①  $V_{CC} = 80\% (V_{CES}), V_{GE} = 20V, L = 25\mu H, R_G = 50\Omega$
- ② Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- ③ Refer to AN-1086 for guidelines for measuring  $V_{(BR)CES}$  safely.
- ④  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑤ Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 117A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.



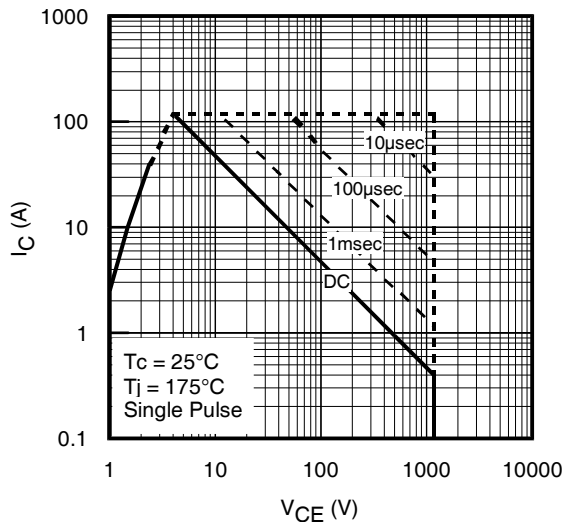
**Fig. 1 - Typical Load Current vs. Frequency**  
(Load Current =  $I_{RMS}$  of fundamental)



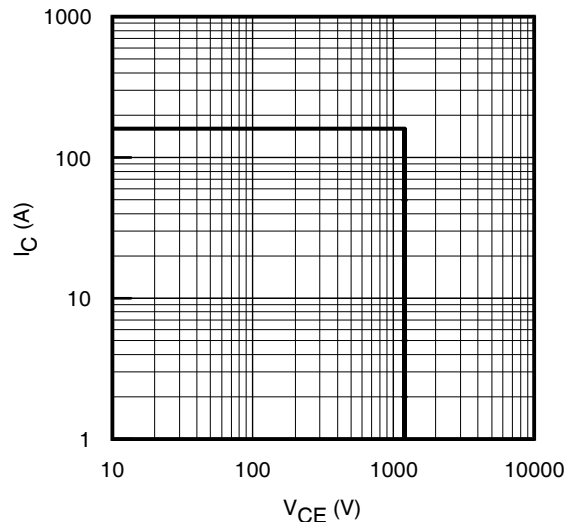
**Fig. 2 - Maximum DC Collector Current vs. Case Temperature**



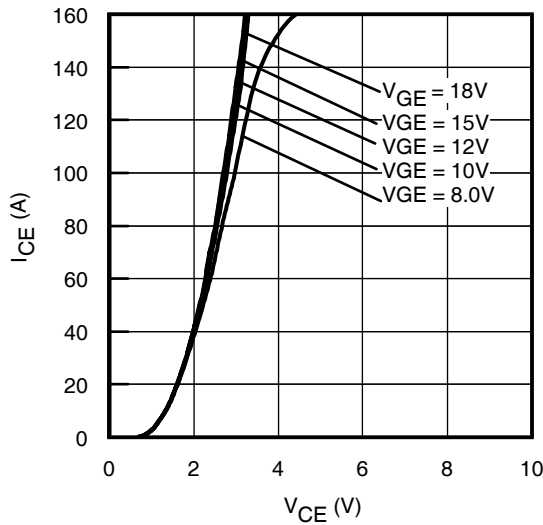
**Fig. 3 - Power Dissipation vs. Case Temperature**



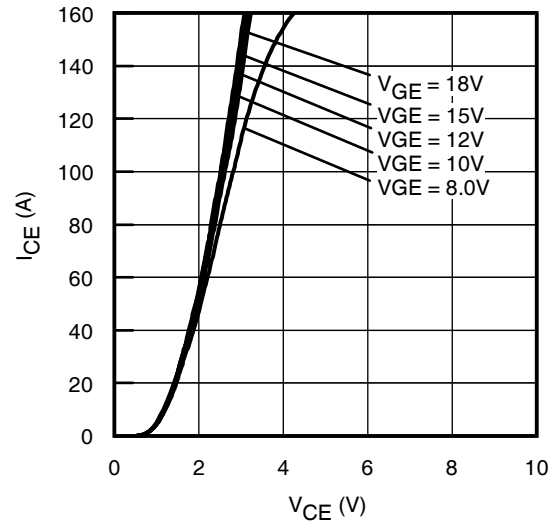
**Fig. 4 - Forward SOA**  
 $T_C = 25^\circ\text{C}$ ,  $T_J \leq 175^\circ\text{C}$ ;  $V_{GE} = 15\text{V}$



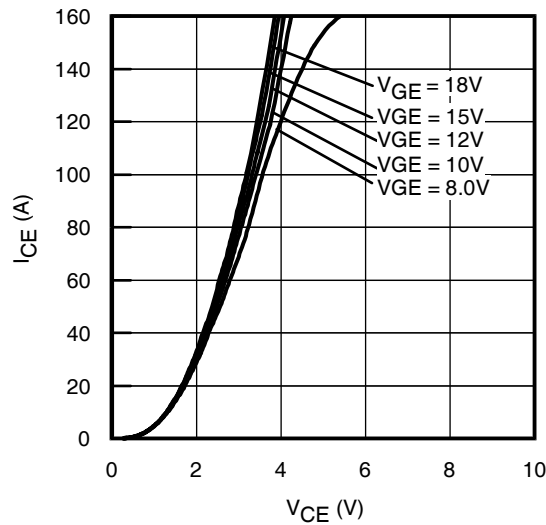
**Fig. 5 - Reverse Bias SOA**  
 $T_J = 175^\circ\text{C}$ ;  $V_{GE} = 20\text{V}$



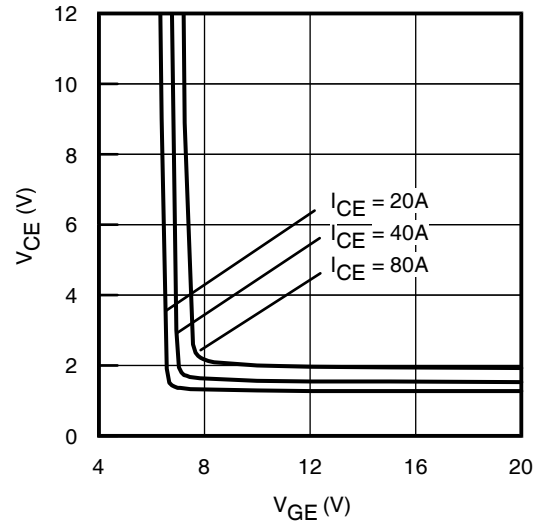
**Fig. 6** - Typ. IGBT Output Characteristics  
 $T_J = -40^\circ\text{C}$ ;  $t_p = 20\mu\text{s}$



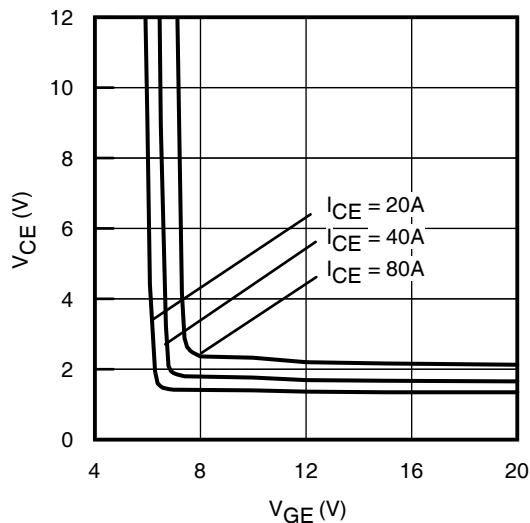
**Fig. 7** - Typ. IGBT Output Characteristics  
 $T_J = 25^\circ\text{C}$ ;  $t_p = 20\mu\text{s}$



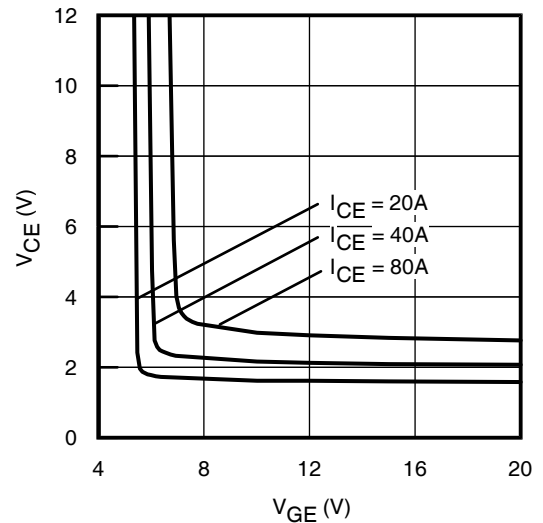
**Fig. 8** - Typ. IGBT Output Characteristics  
 $T_J = 175^\circ\text{C}$ ;  $t_p = 20\mu\text{s}$



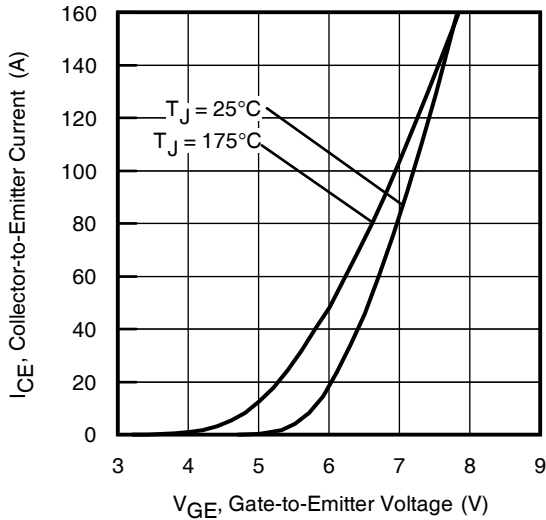
**Fig. 9** - Typical  $V_{CE}$  vs.  $V_{GE}$   
 $T_J = -40^\circ\text{C}$



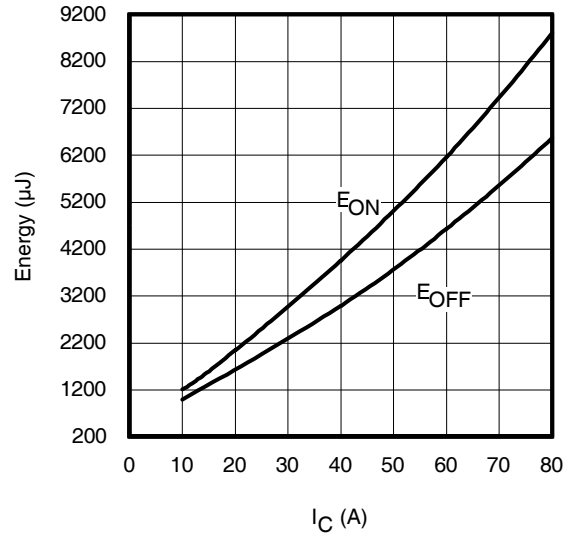
**Fig. 10** - Typical  $V_{CE}$  vs.  $V_{GE}$   
 $T_J = 25^\circ\text{C}$



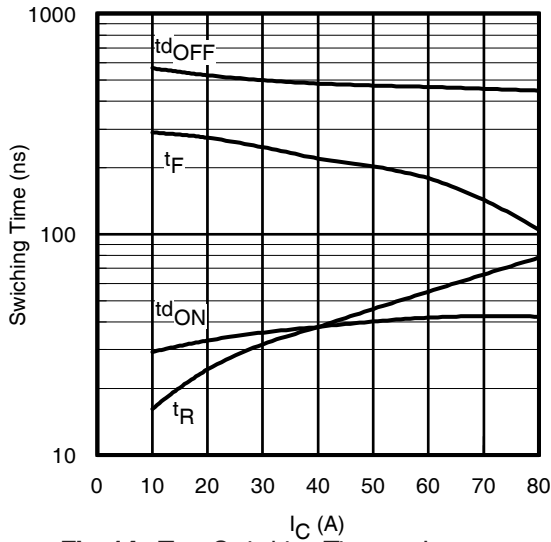
**Fig. 11** - Typical  $V_{CE}$  vs.  $V_{GE}$   
 $T_J = 175^\circ\text{C}$



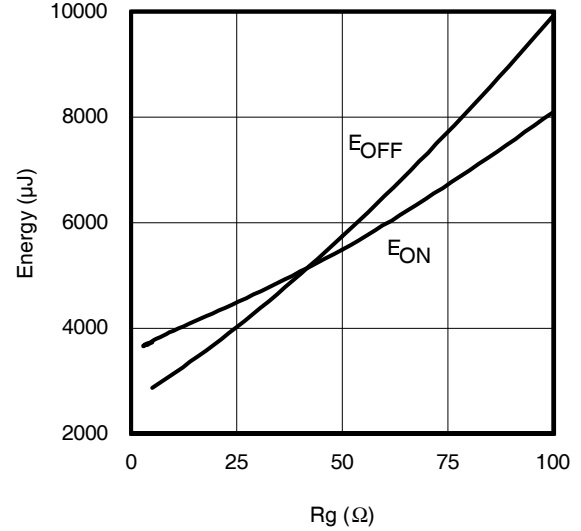
**Fig. 12** - Typ. Transfer Characteristics  
 $V_{CE} = 50V$ ;  $t_p = 20\mu s$



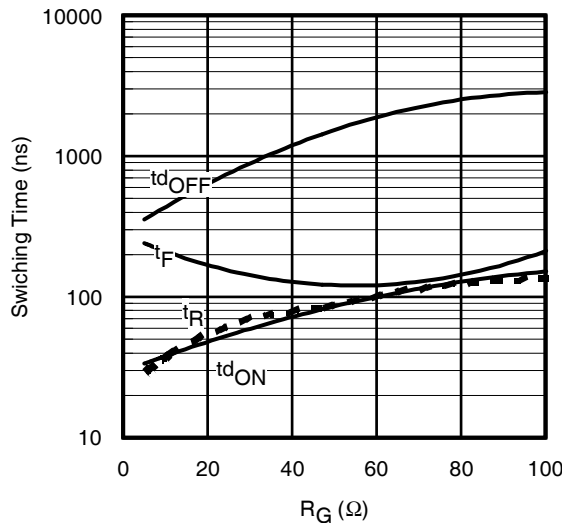
**Fig. 13** - Typ. Energy Loss vs.  $I_C$   
 $T_J = 175^\circ C$ ;  $L = 200\mu H$ ;  $V_{CE} = 600V$ ,  $R_G = 10\Omega$ ;  $V_{GE} = 15V$



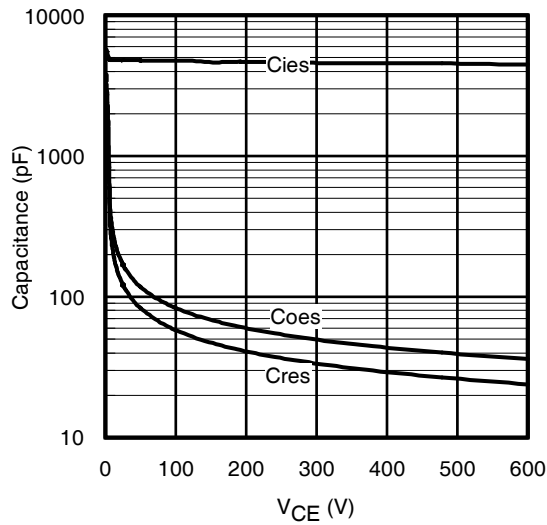
**Fig. 14** - Typ. Switching Time vs.  $I_C$   
 $T_J = 175^\circ C$ ;  $L = 200\mu H$ ;  $V_{CE} = 600V$ ,  $R_G = 10\Omega$ ;  $V_{GE} = 15V$



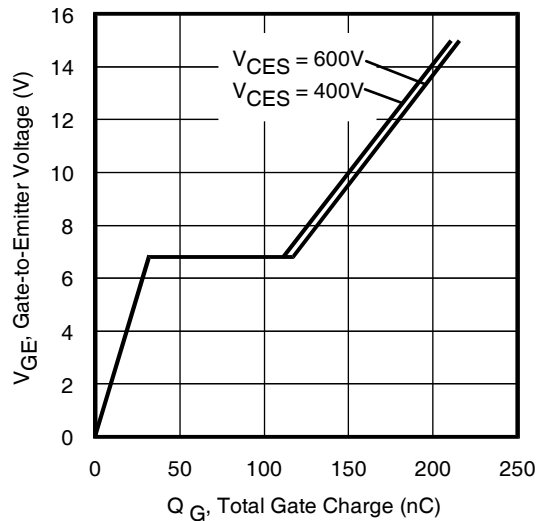
**Fig. 15** - Typ. Energy Loss vs.  $R_G$   
 $T_J = 175^\circ C$ ;  $L = 200\mu H$ ;  $V_{CE} = 600V$ ,  $I_{CE} = 40A$ ;  $V_{GE} = 15V$



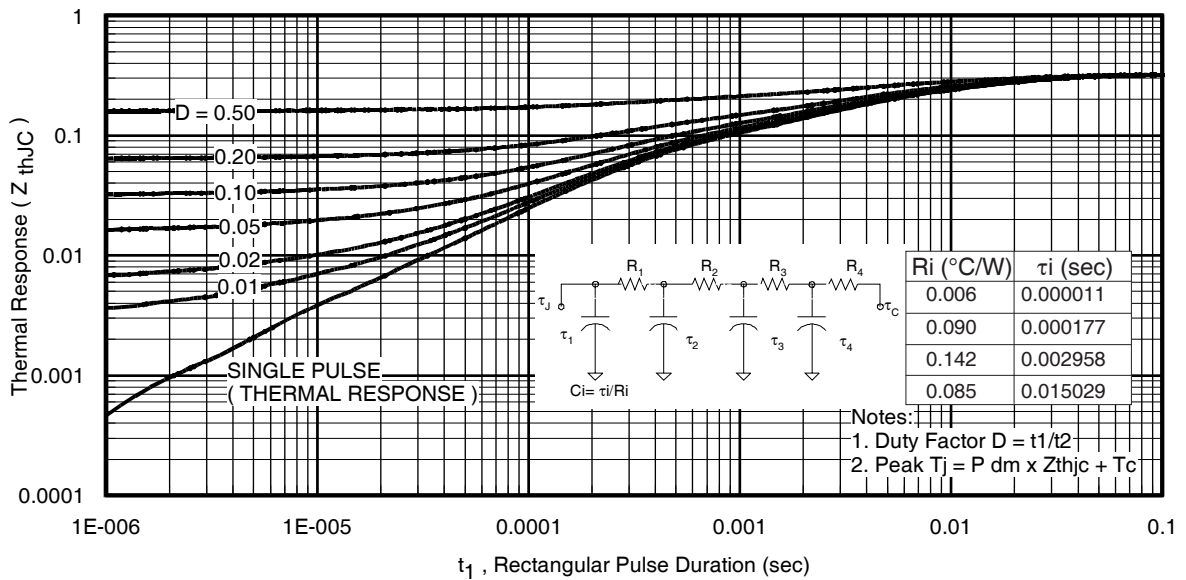
**Fig. 16** - Typ. Switching Time vs.  $R_G$   
 $T_J = 175^\circ C$ ;  $L = 200\mu H$ ;  $V_{CE} = 600V$ ,  $I_{CE} = 40A$ ;  $V_{GE} = 15V$



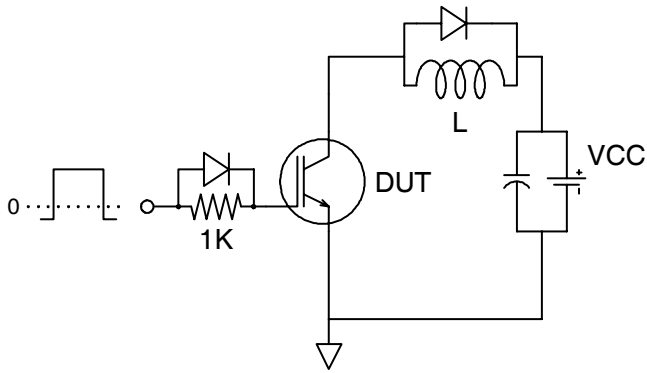
**Fig. 17 - Typ. Capacitance vs.  $V_{CE}$**   
 $V_{GE} = 0V$ ;  $f = 1MHz$



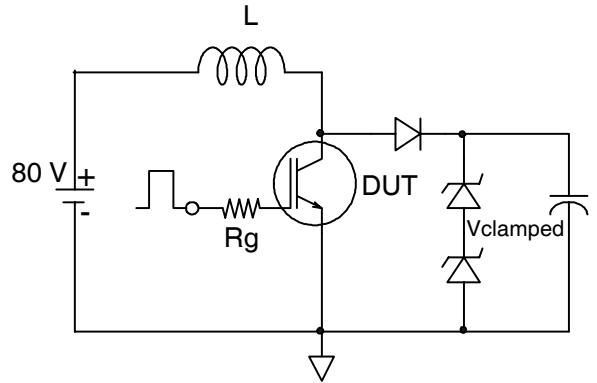
**Fig. 18- Typical Gate Charge vs.  $V_{GE}$**   
 $I_{CE} = 40A$ ;  $L = 2.4mH$



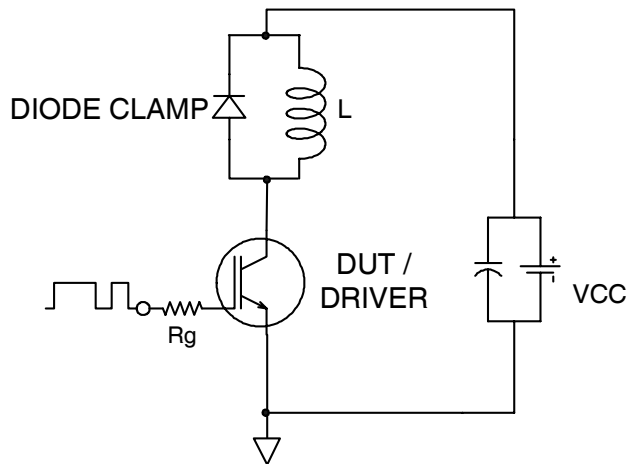
**Fig. 19. Maximum Transient Thermal Impedance, Junction-to-Case (IGBT) TO-247AC**



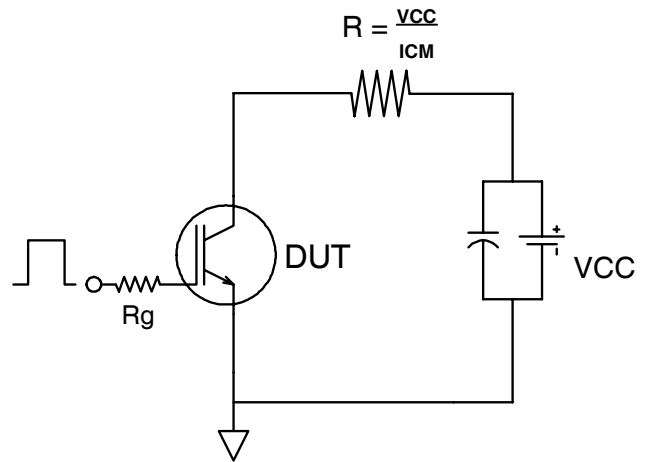
**Fig.C.T.1** - Gate Charge Circuit (turn-off)



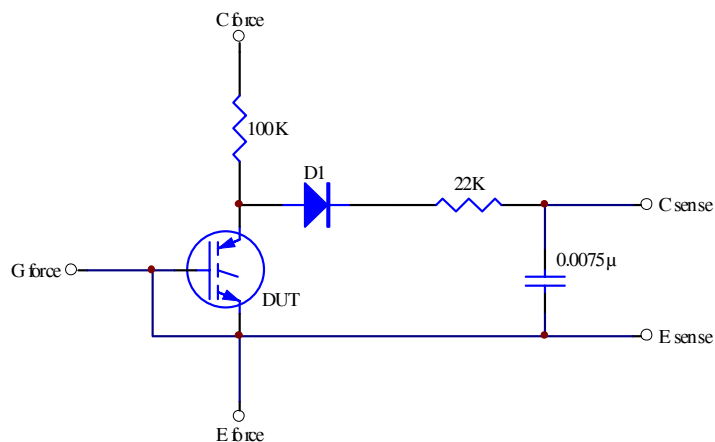
**Fig.C.T.2** - RBSOA Circuit



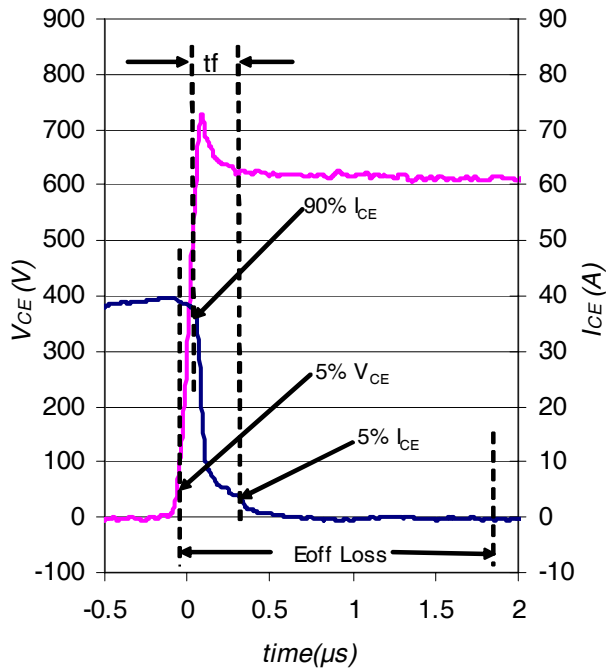
**Fig.C.T.3** - Switching Loss Circuit



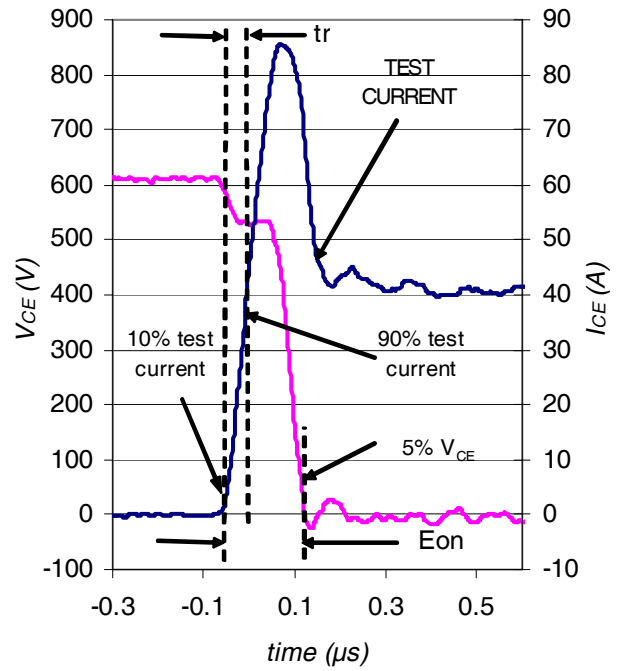
**Fig.C.T.4** - Resistive Load Circuit



**Fig.C.T.5** - BVCES Filter Circuit



**Fig. WF1** - Typ. Turn-off Loss Waveform  
@  $T_J = 175^\circ C$  using Fig. CT.4

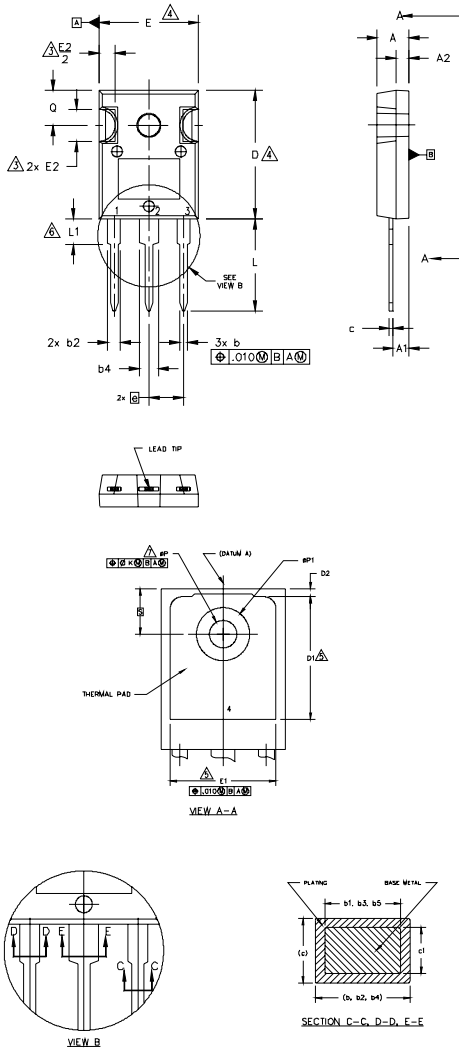


**Fig. WF2** - Typ. Turn-on Loss Waveform  
@  $T_J = 175^\circ C$  using Fig. CT.4



## TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
  2. DIMENSIONS ARE SHOWN IN INCHES.
  3. CONTOUR OF SLOT OPTIONAL.
  4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
  6. LEAD FINISH UNCONTROLLED IN L1.
  7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
- B. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

**LEAD ASSIGNMENTS**

**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

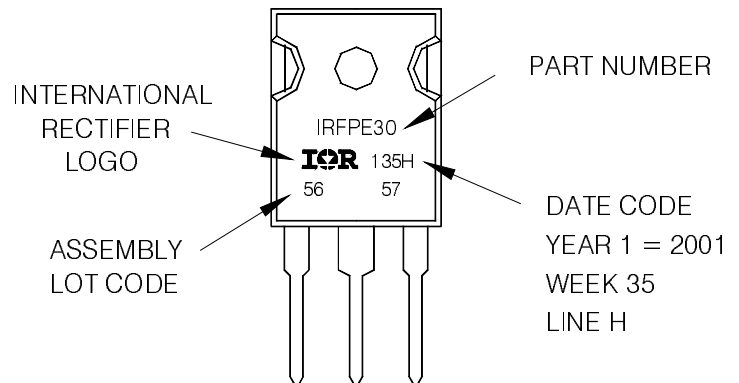
**DIODES**

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

## TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30  
WITH ASSEMBLY  
LOT CODE 5657  
ASSEMBLED ON WW 35, 2001  
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position  
indicates "Lead-Free"

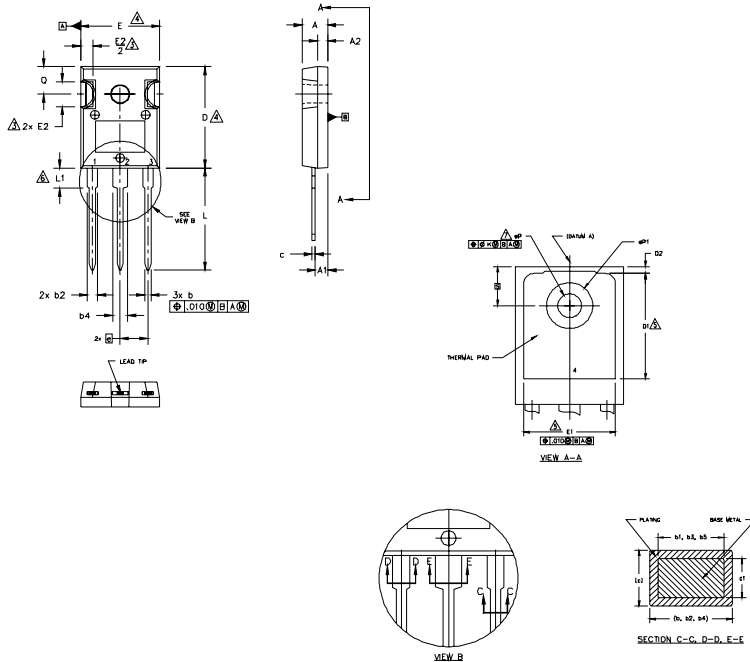


TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## TO-247AD Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.  
CONTOUR OF SLOT OPTIONAL.
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
5. LEAD FINISH UNCONTROLLED IN L1.
6.  $\phi P$  TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AD.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
$\phi k$	.010		0.25		
L	.780	.827	19.57	21.00	
L1	.146	.169	3.71	4.29	
$\phi P$	.140	.144	3.56	3.66	
$\phi P1$	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

**LEAD ASSIGNMENTS**

**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

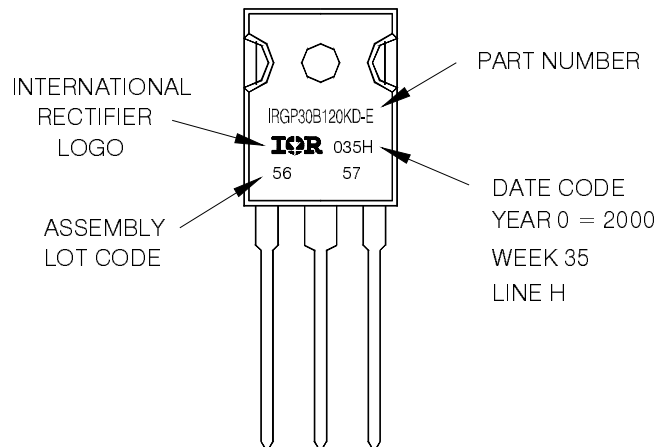
**DIODES**

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

## TO-247AD Part Marking Information

EXAMPLE: THIS IS AN IRGP30B120KD-E  
WITH ASSEMBLY  
LOT CODE 5657  
ASSEMBLED ON WW 35, 2000  
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position  
indicates "Lead-Free"



TO-247AD package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.  
This product has been designed and qualified for Industrial market.  
Qualification Standards can be found on IR's Web site.