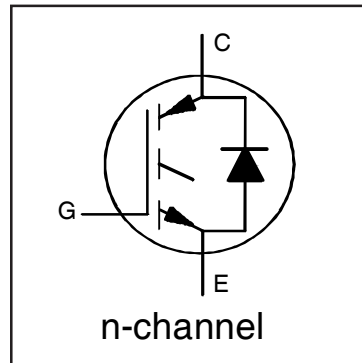


**INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRA-LOW VF DIODE
 FOR INDUCTION HEATING AND SOFT SWITCHING APPLICATIONS**

**IRG7PH42UD1PbF
 IRG7PH42UD1-EP**

Features

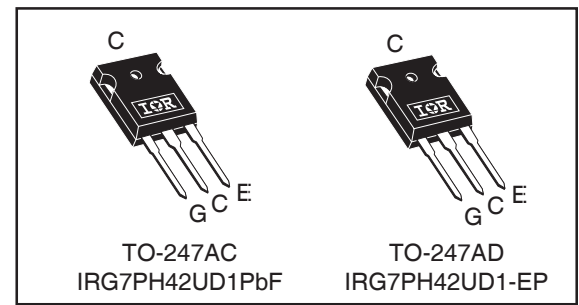
- Low $V_{CE(ON)}$ trench IGBT technology
- Low switching losses
- Square RBSOA
- Ultra-low V_F Diode
- 1300Vpk repetitive transient capacity
- 100% of the parts tested for I_{LM} ①
- Positive $V_{CE(ON)}$ temperature co-efficient
- Tight parameter distribution
- Lead free package



$V_{CES} = 1200V$
$I_{NOMINAL} = 30A$
$T_{J(max)} = 150^{\circ}C$
$V_{CE(on)}$ typ. = 1.7V

Benefits

- Device optimized for induction heating and soft switching applications
- High Efficiency due to Low $V_{CE(on)}$, low switching losses and Ultra-low V_F
- Rugged transient performance for increased reliability
- Excellent current sharing in parallel operation
- Low EMI



G	C	E
Gate	Collector	Emitter

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
$I_C @ T_C = 25^{\circ}C$	Continuous Collector Current	85 ^②	A
$I_C @ T_C = 100^{\circ}C$	Continuous Collector Current	45	
$I_{NOMINAL}$	Nominal Current	30	
I_{CM}	Pulse Collector Current, $V_{GE}=15V$ ⑥	90	
I_{LM}	Clamped Inductive Load Current, $V_{GE}=20V$ ①	120	
$I_F @ T_C = 25^{\circ}C$	Diode Continuous Forward Current	70	
$I_F @ T_C = 100^{\circ}C$	Diode Continuous Forward Current	35	
I_{FRM}	Diode Repetitive Peak Forward Current ②	120	
V_{GE}	Continuous Gate-to-Emitter Voltage	± 30	V
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	313	W
$P_D @ T_C = 100^{\circ}C$	Maximum Power Dissipation	125	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	$^{\circ}C$
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw	10 lbf-in (1.1 N·m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$ (IGBT)	Thermal Resistance Junction-to-Case-(each IGBT) ④	—	—	0.4	$^{\circ}C/W$
$R_{\theta JC}$ (Diode)	Thermal Resistance Junction-to-Case-(each Diode) ④	—	—	1.05	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink (flat, greased surface)	—	0.24	—	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (typical socket mount)	—	40	—	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	$V_{GE} = 0V, I_C = 100\mu\text{A}$ ③
$V_{CES(Transient)}$	Repetitive Transient Collector-to-Emitter Voltage	—	—	1300	V	$V_{GE} = 0V, T_J = 75^\circ\text{C}, PW \leq 10\mu\text{s}$ ③
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	1.2	—	V/°C	$V_{GE} = 0V, I_C = 2.0\text{mA}$ (25°C-150°C)
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.7	2.0	V	$I_C = 30A, V_{GE} = 15V, T_J = 25^\circ\text{C}$
		—	2.0	—		$I_C = 30A, V_{GE} = 15V, T_J = 150^\circ\text{C}$
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0	V	$V_{CE} = V_{GE}, I_C = 1.0\text{mA}$
g_{fe}	Forward Transconductance	—	32	—	S	$V_{CE} = 50V, I_C = 30A, PW = 80\mu\text{s}$
I_{CES}	Collector-to-Emitter Leakage Current	—	1.0	100	μA	$V_{GE} = 0V, V_{CE} = 1200V$
		—	230	—		$V_{GE} = 0V, V_{CE} = 1200V, T_J = 150^\circ\text{C}$
V_{FM}	Diode Forward Voltage Drop	—	1.15	1.30	V	$I_F = 30A$
		—	1.10	—		$I_F = 30A, T_J = 150^\circ\text{C}$
I_{GES}	Gate-to-Emitter Leakage Current	—	—	± 100	nA	$V_{GE} = \pm 30V$

Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	180	270	nC	$I_C = 30A$ $V_{GE} = 15V$ $V_{CC} = 600V$
Q_{ge}	Gate-to-Emitter Charge (turn-on)	—	24	36		
Q_{gc}	Gate-to-Collector Charge (turn-on)	—	70	110		
E_{off}	Turn-Off Switching Loss	—	1210	1450	μJ	$I_C = 30A, V_{CC} = 600V, V_{GE} = 15V$ $R_G = 10\Omega, L = 200\mu\text{H}, T_J = 25^\circ\text{C}$ Energy losses include tail
$t_{d(off)}$	Turn-Off delay time	—	270	290	ns	$I_C = 30A, V_{CC} = 600V, V_{GE} = 15V$ $R_G = 10\Omega, L = 200\mu\text{H}, T_J = 25^\circ\text{C}$
t_f	Fall time	—	35	43		
E_{off}	Turn-Off Switching Loss	—	1936	—	μJ	$I_C = 30A, V_{CC} = 600V, V_{GE} = 15V$ $R_G = 10\Omega, L = 200\mu\text{H}, T_J = 150^\circ\text{C}$ Energy losses include tail
$t_{d(off)}$	Turn-Off delay time	—	300	—	ns	$I_C = 30A, V_{CC} = 600V, V_{GE} = 15V$ $R_G = 10\Omega, L = 200\mu\text{H}, T_J = 150^\circ\text{C}$
t_f	Fall time	—	160	—		
C_{ies}	Input Capacitance	—	3390	—	pF	$V_{GE} = 0V$ $V_{CC} = 30V$ $f = 1.0\text{MHz}$
C_{oes}	Output Capacitance	—	130	—		
C_{res}	Reverse Transfer Capacitance	—	83	—		
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				$T_J = 150^\circ\text{C}, I_C = 120A$ $V_{CC} = 960V, V_p = 1200V$ $R_g = 10\Omega, V_{GE} = +20V \text{ to } 0V$

Notes:

- ① $V_{CC} = 80\% (V_{CES}), V_{GE} = 20V, L = 22\mu\text{H}, R_G = 10\Omega$.
- ② Pulse width limited by max. junction temperature.
- ③ Refer to AN-1086 for guidelines for measuring $V_{(BR)CES}$ safely.
- ④ R_θ is measured at T_J of approximately 90°C .
- ⑤ Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 78A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- ⑥ Rating for Hard Switching conditions. Rating is higher in Soft Switching conditions.

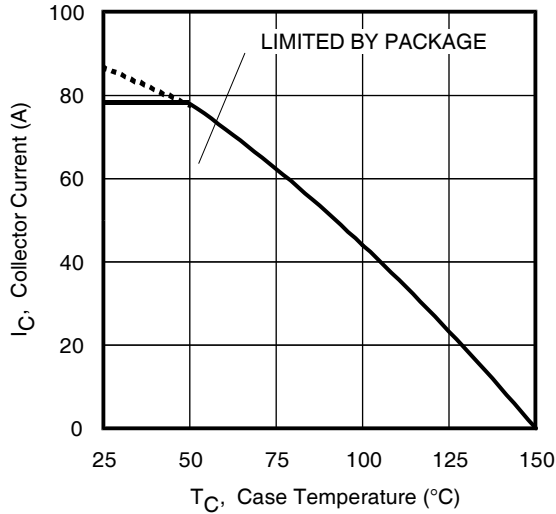


Fig. 1 - Maximum DC Collector Current vs. Case Temperature

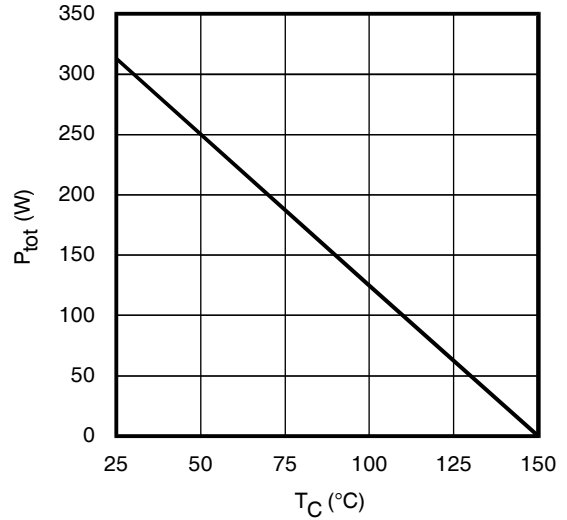


Fig. 2 - Power Dissipation vs. Case Temperature

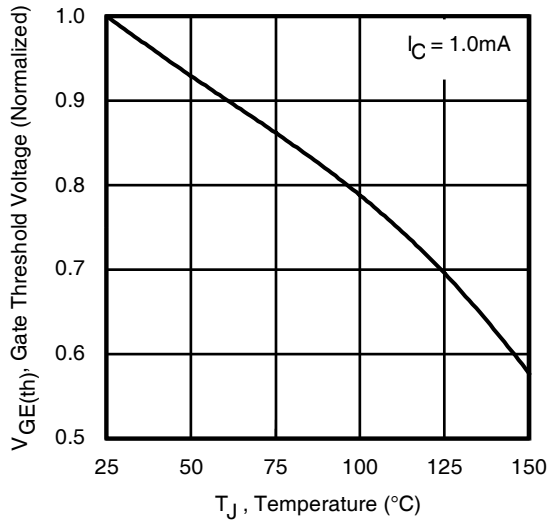


Fig. 3 - Typical Gate Threshold Voltage (Normalized) vs. Junction Temperature

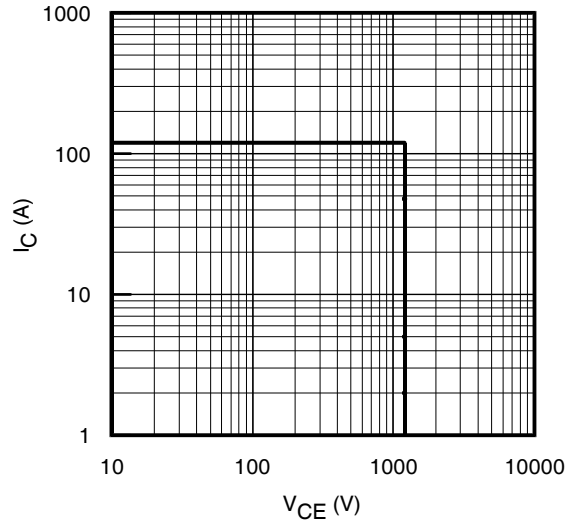


Fig. 4 - Reverse Bias SOA
 $T_J = 150^\circ\text{C}; V_{GE} = 20\text{V}$

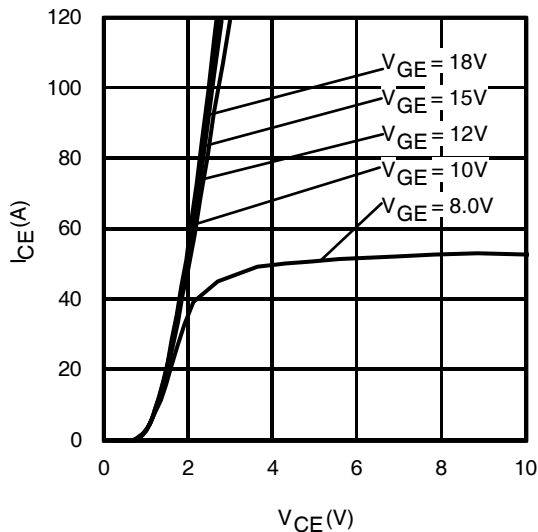


Fig. 5 - Typ. IGBT Output Characteristics
 $T_J = -40^\circ\text{C}; t_p = 80\mu\text{s}$

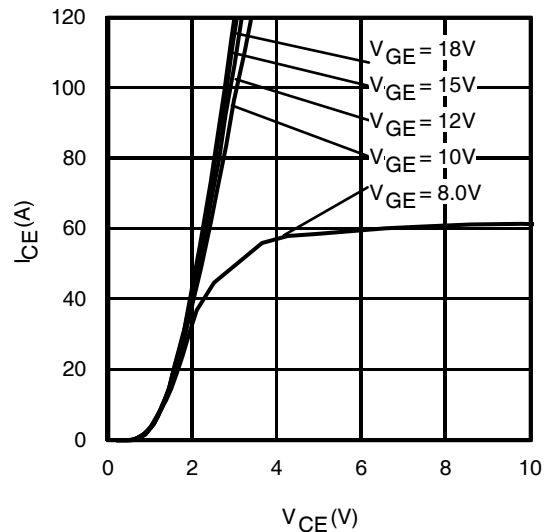


Fig. 6 - Typ. IGBT Output Characteristics
 $T_J = 25^\circ\text{C}; t_p = 80\mu\text{s}$

IRG7PH42UD1PbF/IRG7PH42UD1-EP

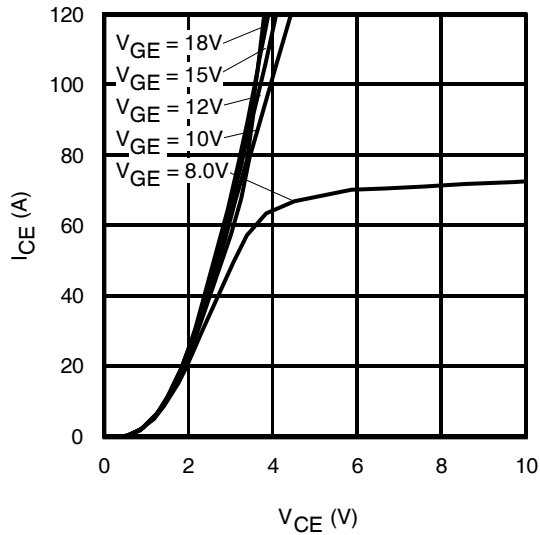


Fig. 7 - Typ. IGBT Output Characteristics
 $T_J = 150^\circ\text{C}$; $t_p = 80\mu\text{s}$

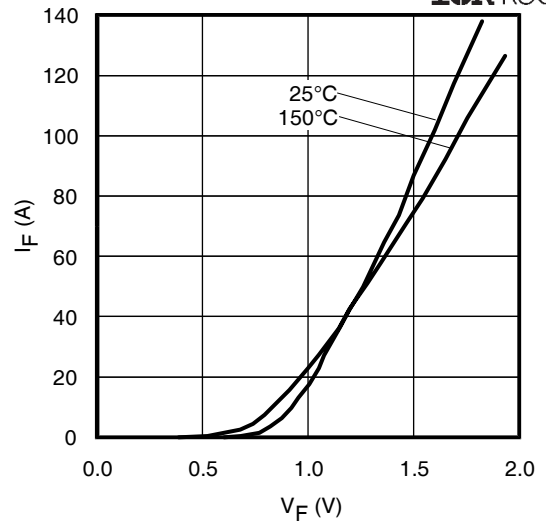


Fig. 8 - Typ. Diode Forward Voltage Drop Characteristics

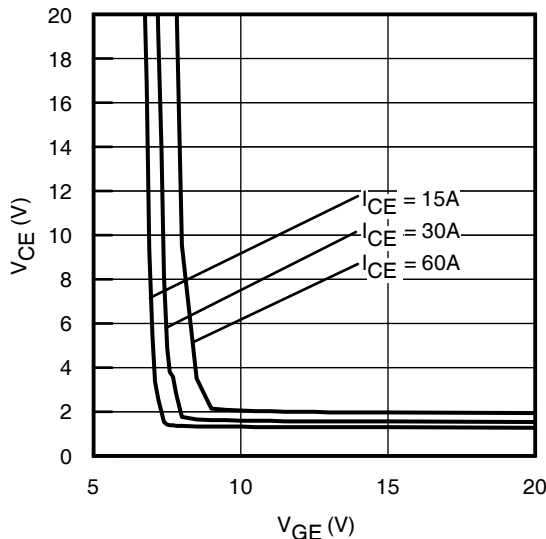


Fig. 9 - Typical V_{CE} vs. V_{GE}
 $T_J = -40^\circ\text{C}$

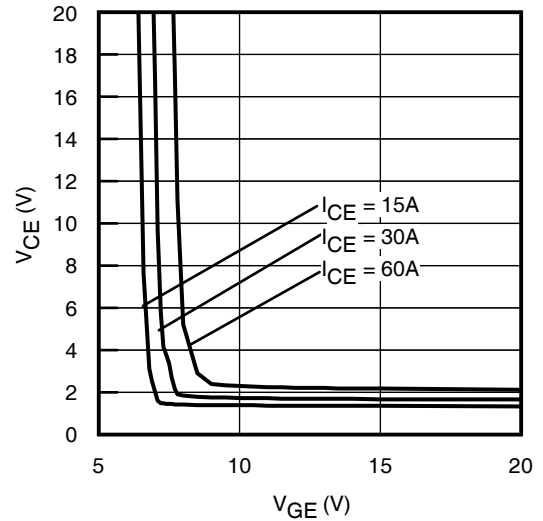


Fig. 10 - Typical V_{CE} vs. V_{GE}
 $T_J = 25^\circ\text{C}$

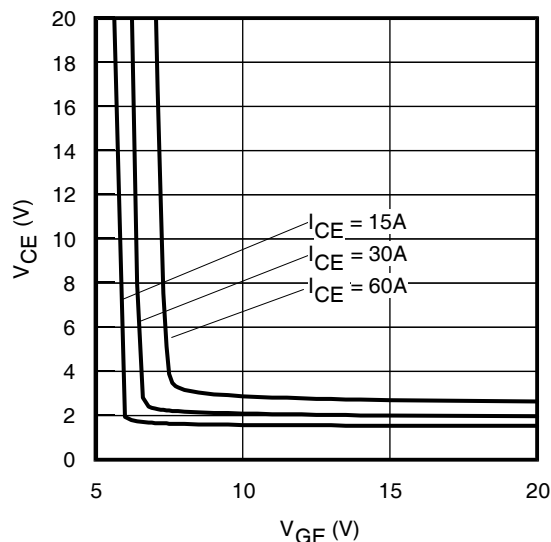


Fig. 11 - Typical V_{CE} vs. V_{GE}
 $T_J = 150^\circ\text{C}$

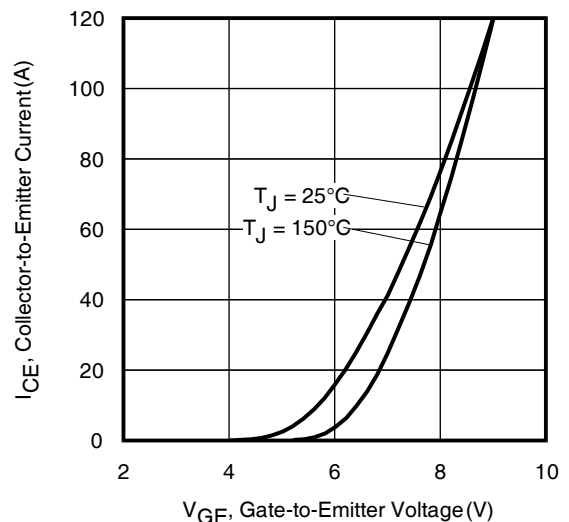


Fig. 12 - Typ. Transfer Characteristics
 $V_{CE} = 50\text{V}$; $t_p = 10\mu\text{s}$

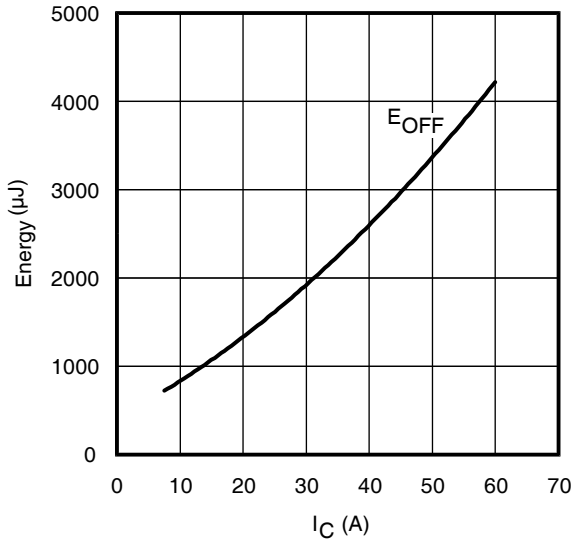


Fig. 13 - Typ. Energy Loss vs. I_C

$T_J = 150^\circ\text{C}$; $L = 200\mu\text{H}$; $V_{CE} = 600\text{V}$; $R_G = 10\Omega$; $V_{GE} = 15\text{V}$

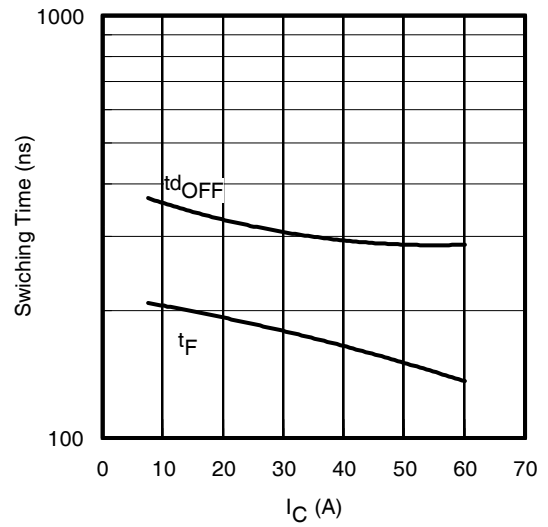


Fig. 14 - Typ. Switching Time vs. I_C

$T_J = 150^\circ\text{C}$; $L = 200\mu\text{H}$; $V_{CE} = 600\text{V}$; $R_G = 10\Omega$; $V_{GE} = 15\text{V}$

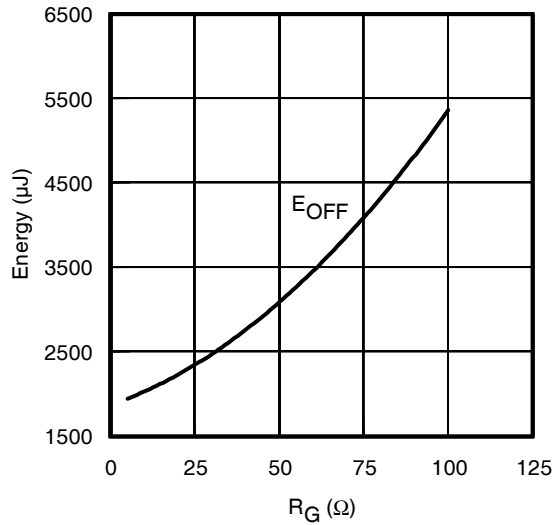


Fig. 15 - Typ. Energy Loss vs. R_G

$T_J = 150^\circ\text{C}$; $L = 200\mu\text{H}$; $V_{CE} = 600\text{V}$; $I_{CE} = 30\text{A}$; $V_{GE} = 15\text{V}$

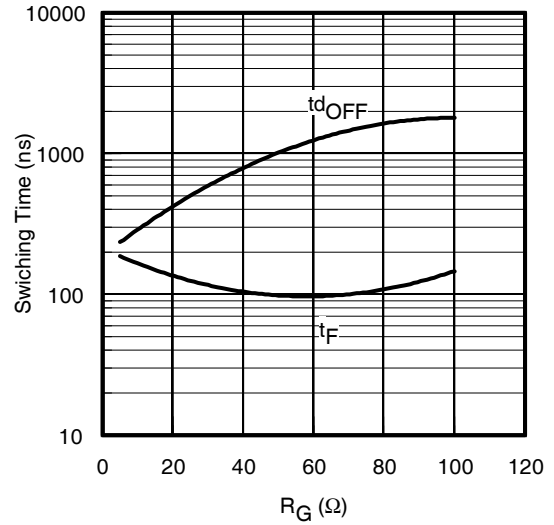


Fig. 16 - Typ. Switching Time vs. R_G

$T_J = 150^\circ\text{C}$; $L = 200\mu\text{H}$; $V_{CE} = 600\text{V}$; $I_{CE} = 30\text{A}$; $V_{GE} = 15\text{V}$

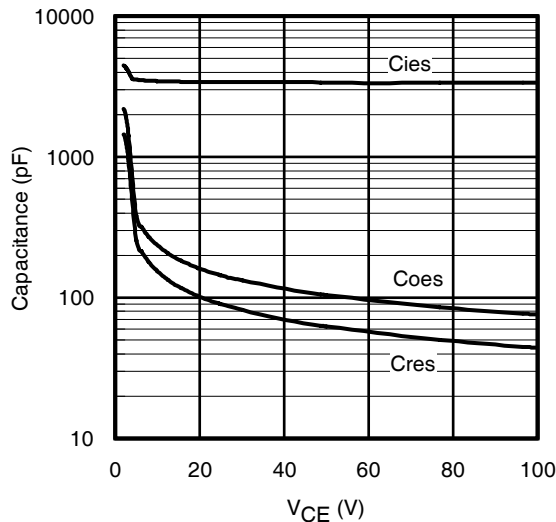


Fig. 17 - Typ. Capacitance vs. V_{CE}
 $V_{GE} = 0\text{V}$; $f = 1\text{MHz}$

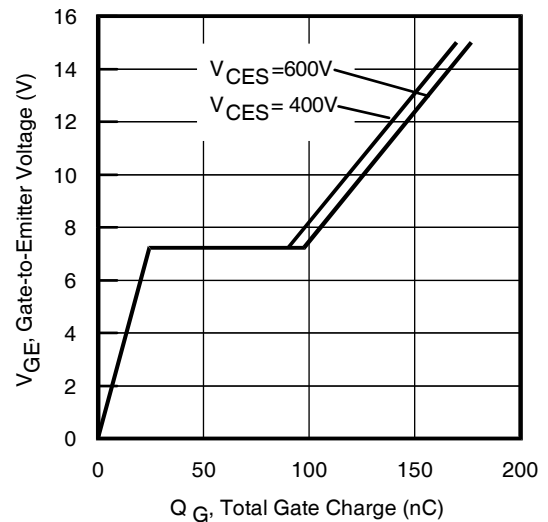


Fig. 18 - Typical Gate Charge vs. V_{GE}
 $I_{CE} = 30\text{A}$; $L = 680\mu\text{H}$

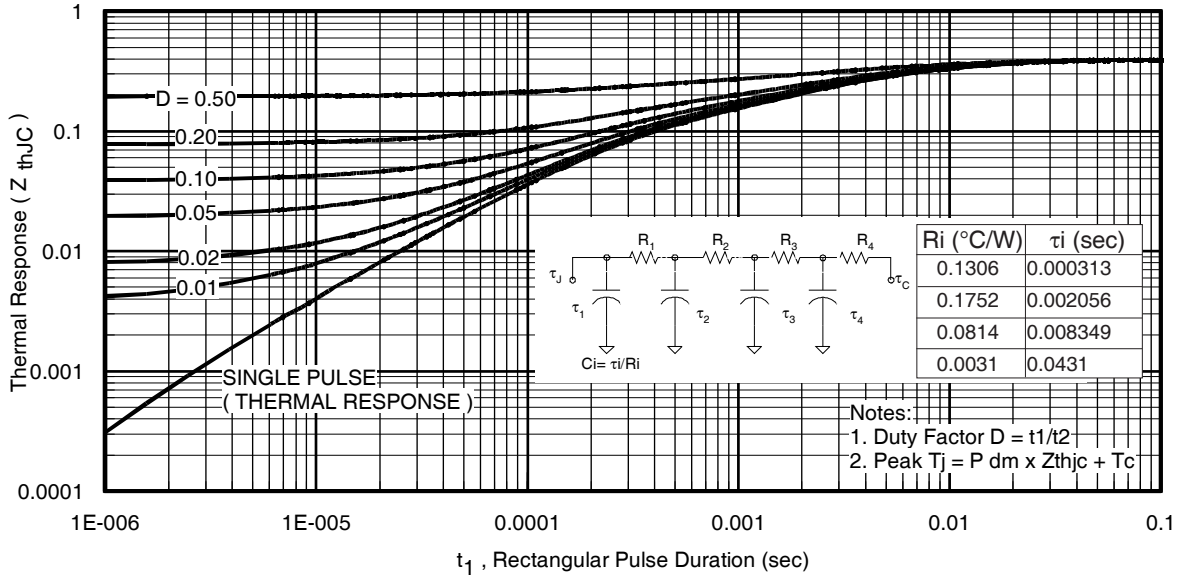


Fig 19. Maximum Transient Thermal Impedance, Junction-to-Case (IGBT)

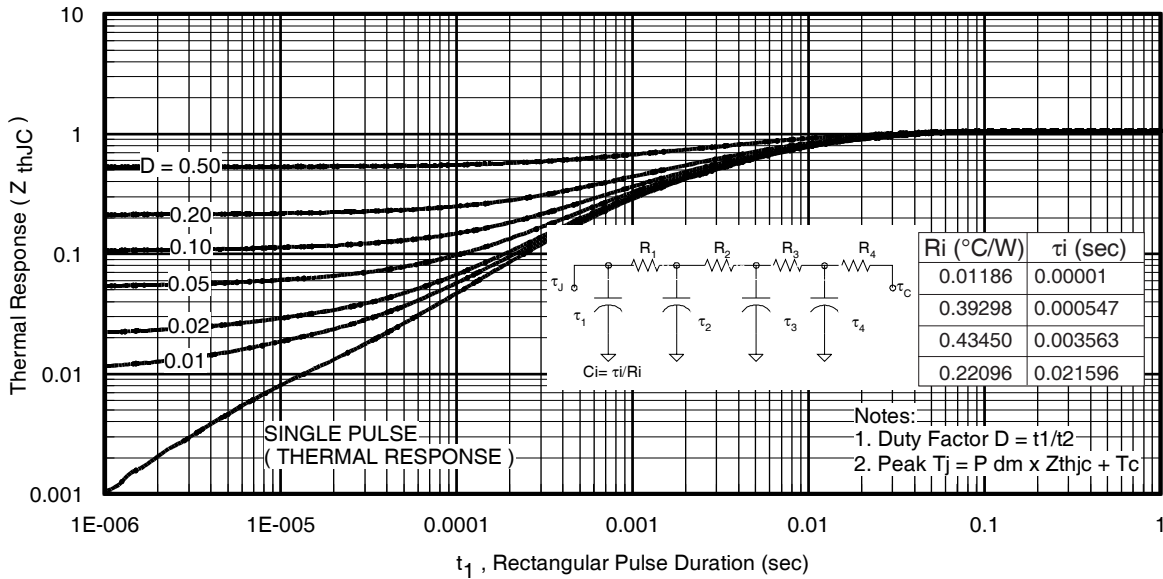


Fig. 20. Maximum Transient Thermal Impedance, Junction-to-Case (DIODE)

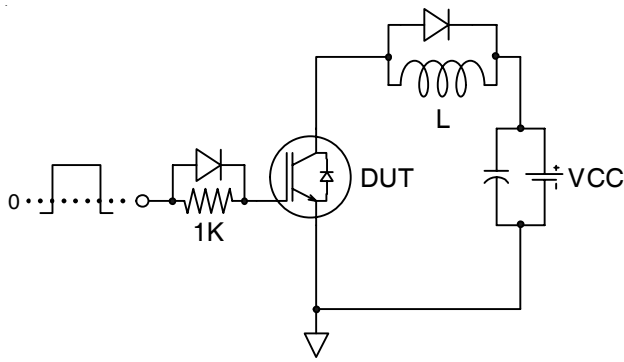


Fig.C.T.1 - Gate Charge Circuit (turn-off)

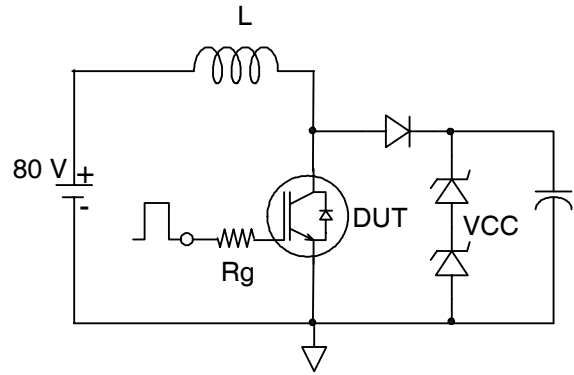


Fig.C.T.2 - RBSOA Circuit

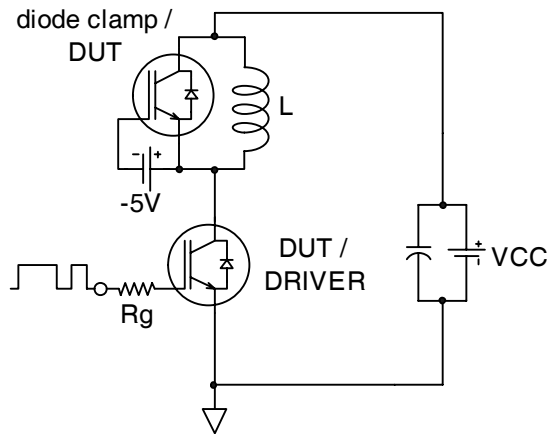


Fig.C.T.3 - Switching Loss Circuit

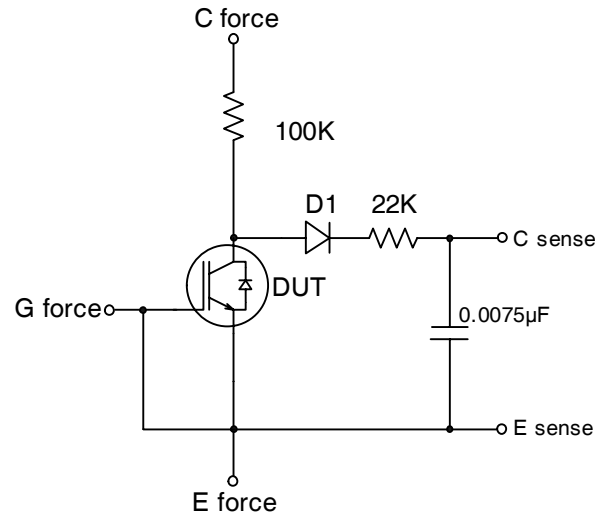


Fig.C.T.4 - BVCES Filter Circuit

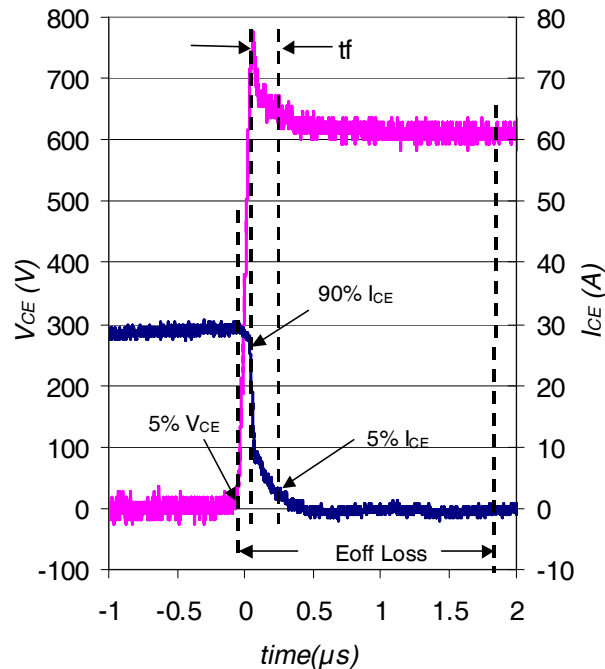
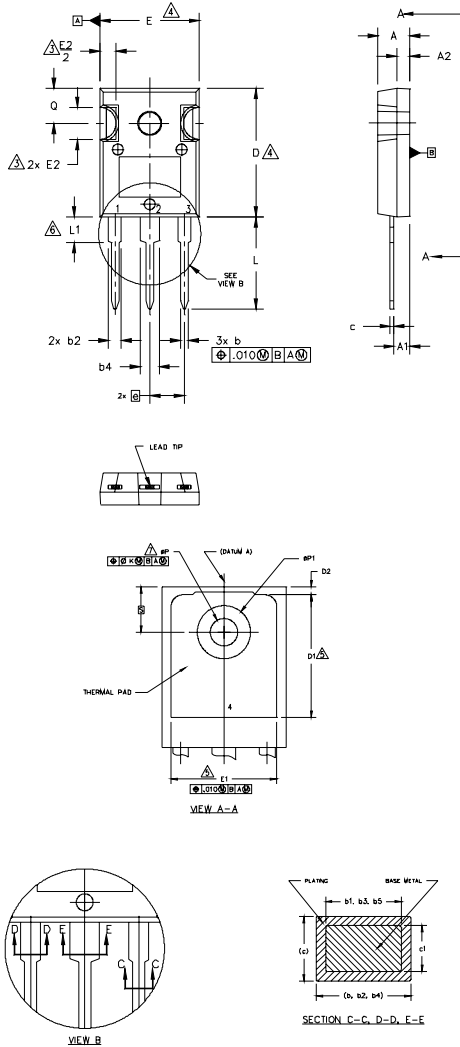


Fig. WF1 - Typ. Turn-off Loss Waveform
@ $T_J = 150^\circ\text{C}$ using Fig. CT.3

IRG7PH42UD1PbF/IRG7PH42UD1-EP

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

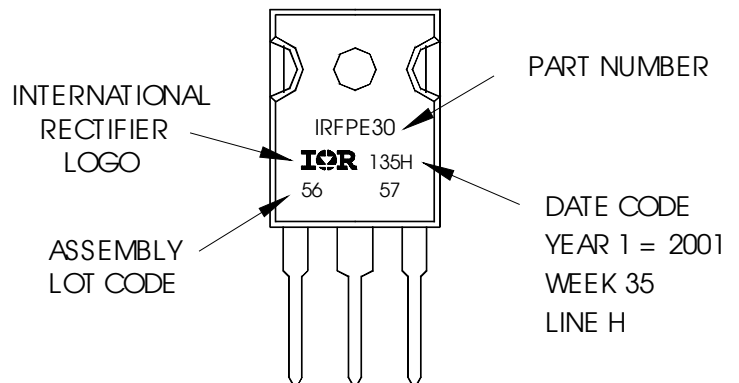
DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"

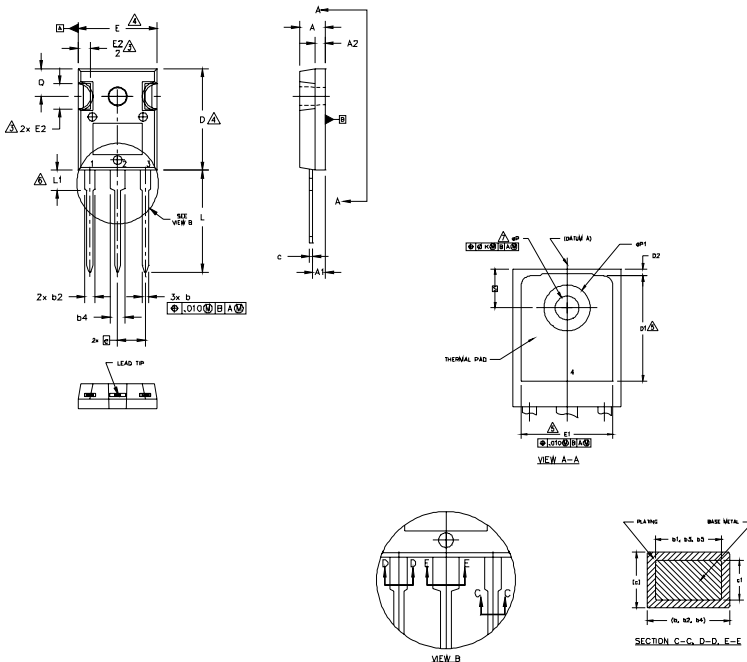


TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

TO-247AD Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
 2. DIMENSIONS ARE SHOWN IN INCHES.
 3. CONTOUR OF SLOT OPTIONAL.
 4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
 6. LEAD FINISH UNCONTROLLED IN L1.
 7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
 8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AD.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	4
D	.776	.815	19.71	20.70	5
D1	.515	-	13.08	-	
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.780	.827	19.57	21.00	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

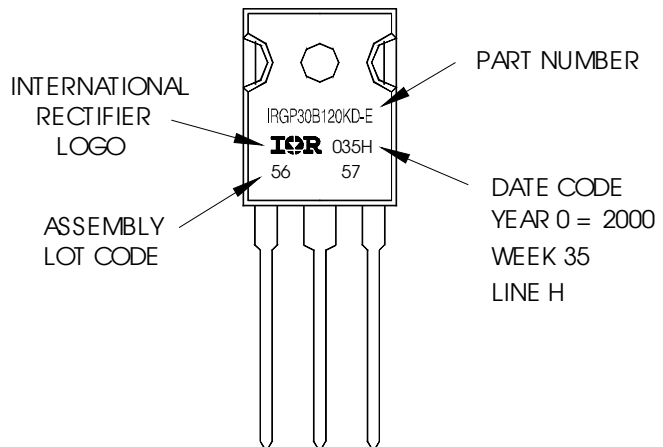
DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AD Part Marking Information

EXAMPLE: THIS IS AN IRGP30B120KD-E
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247AD package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.
This product has been designed and qualified for Industrial market.
Qualification Standards can be found on IR's Web site.