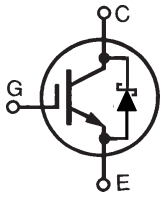
IXYS

GenX3™ 600V IGBT w/ SiC Anti-Parallel Diode

IXGR60N60C3C1

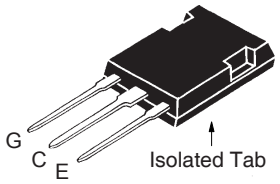
(Electrically Isolated Back Surface)

High Speed PT IGBT for 40-100kHz Switching



V_{CES} = 600V
I_{C110} = 30A
$V_{CE(sat)}$ ≤ 2.5V
$t_{fi(typ)}$ = 50ns

ISOPLUS247™



G = Gate C = Collector
E = Emitter

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	600	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	600	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C (Limited by leads)	75	A
I_{C110}	T_C = 110°C	30	A
I_{F110}	T_C = 110°C	13	A
I_{CM}	T_C = 25°C, 1ms	260	A
I_A	T_C = 25°C	40	A
E_{AS}	T_C = 25°C	400	mJ
SSOA (RBSOA)	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 3Ω Clamped Inductive Load	I_{CM} = 125 @ $V_{CE} \le V_{CES}$	A
P_C	T_C = 25°C	170	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
V_{ISOL}	50/60 Hz, RMS, t = 1minute I_{ISOL} < 1mA t = 10 s	2500 3000	V~ V~
F_C	Mounting Force	20..120/4.5..27	N/lb
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6mm (0.062 in.) from Case for 10s	260	°C
Weight		5	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
$V_{GE(th)}$	I_C = 250μA, V_{CE} = V_{GE}	3.0		5.5	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			50	μA
	T_J = 125°C			1	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V			±100	nA
$V_{CE(sat)}$	I_C = 40A, V_{GE} = 15V, Note 1		2.2	2.5	V
	T_J = 125°C		1.7		V

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Optimized for Low Switching Losses
- Square RBSOA
- Isolated Mounting Surface
- Anti-Parallel Ultra Fast Diode
- High Speed Silicon Carbide Schottky Co-Pack Diode
  - No Reverse Recovery
- 2500V Electrical Isolation
- Avalanche Rated

Advantages

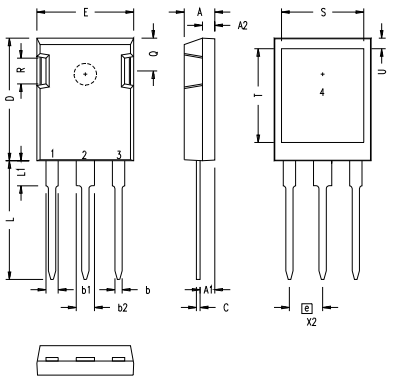
- High Power Density
- Low Gate Drive Requirement

Applications

- High Frequency Power Inverters
- UPS
- Motor Drives
- SMPS
- PFC Circuits
- Battery Chargers
- Welding Machines
- Lamp Ballasts

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	I_C = 40A, V_{CE} = 10V, Note 1	23	38		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		2810		pF
C_{oes}			210		pF
C_{res}			80		pF
Q_g	I_C = 50A, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}		115		nC
Q_{ge}			43		nC
Q_{gc}			22		nC
$t_{d(on)}$	**Inductive Load, T_J = 25°C**		24		ns
t_{ri}	I_C = 40A, V_{GE} = 15V		40		ns
E_{on}	V_{CE} = 480V, R_G = 3Ω		0.83		mJ
$t_{d(off)}$	Note 2		70	110	ns
t_{fi}			50		ns
E_{off}			0.45	0.80	mJ
$t_{d(on)}$	**Inductive Load, T_J = 125°C**		23		ns
t_{ri}	I_C = 40A, V_{GE} = 15V		39		ns
E_{on}	V_{CE} = 480V, R_G = 3Ω		0.78		mJ
$t_{d(off)}$	Note 2		112		ns
t_{fi}			86		ns
E_{off}			0.80		mJ
R_{thJC}				0.73	°C/W
R_{thCS}			0.15		°C/W

ISOPLUS247 (IXGR) Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

Reverse Diode (SiC)

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
V_F	I_F = 20A, V_{GE} = 0V, Note 1		1.65	2.10	V
	T_J = 125°C		1.80		V
R_{thJC}				1.75	°C/W

Notes:

1. Pulse test, t ≤ 300µs, duty cycle, d ≤ 2%.
2. Switching times & energy losses may increase for higher V_{CE}(Clamp), T_J or R_G.

Fig. 1. Output Characteristics @ T_J = 25ºC

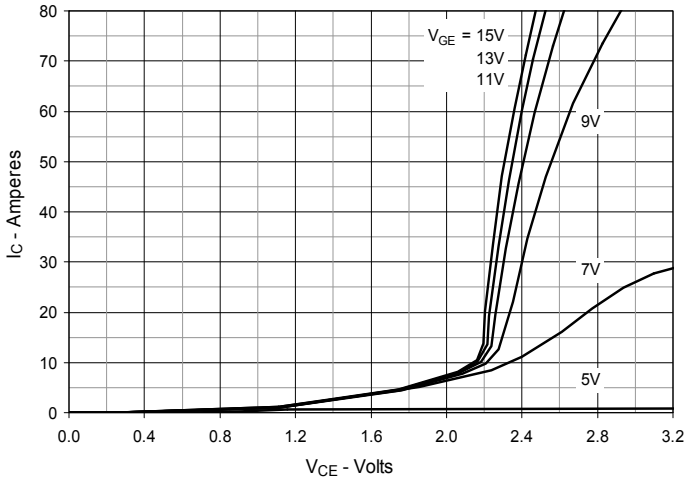


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

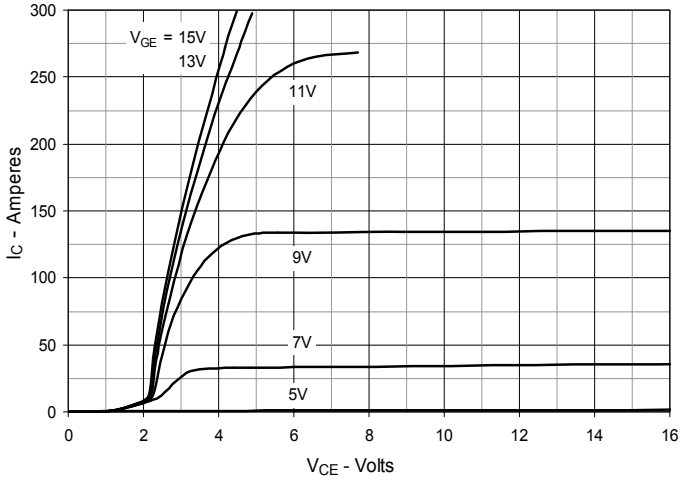


Fig. 3. Output Characteristics @ T_J = 125ºC

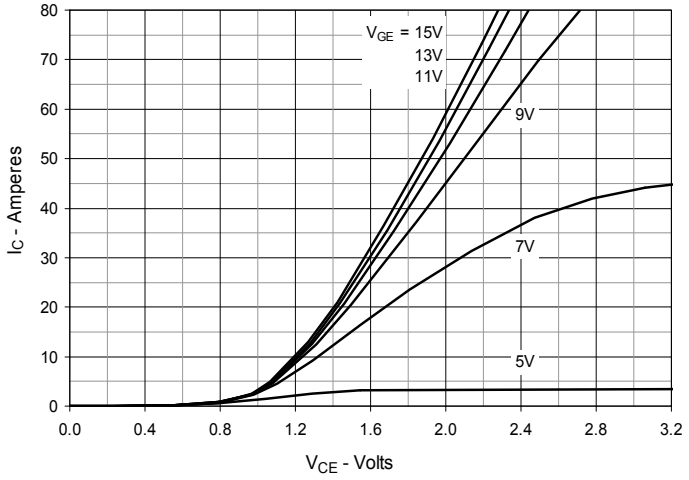


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

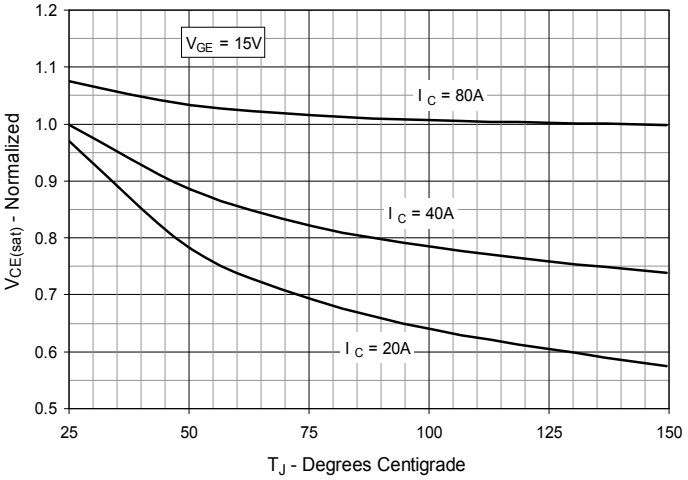


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

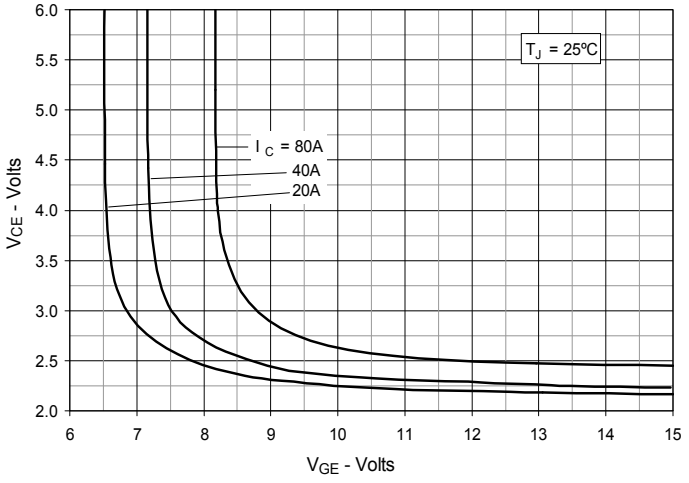


Fig. 6. Input Admittance

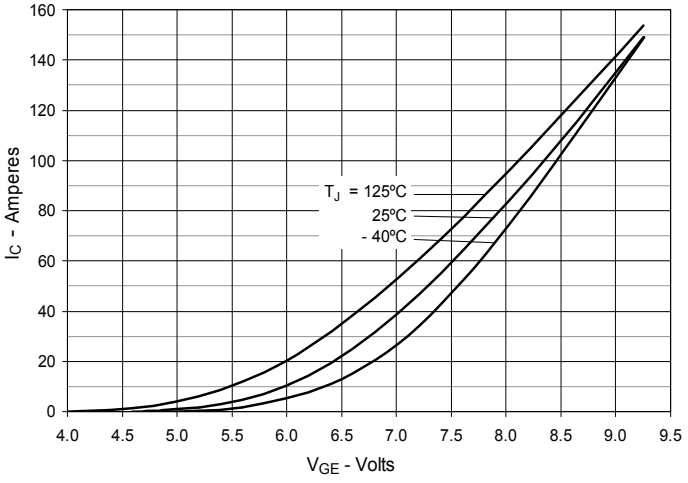


Fig. 7. Transconductance

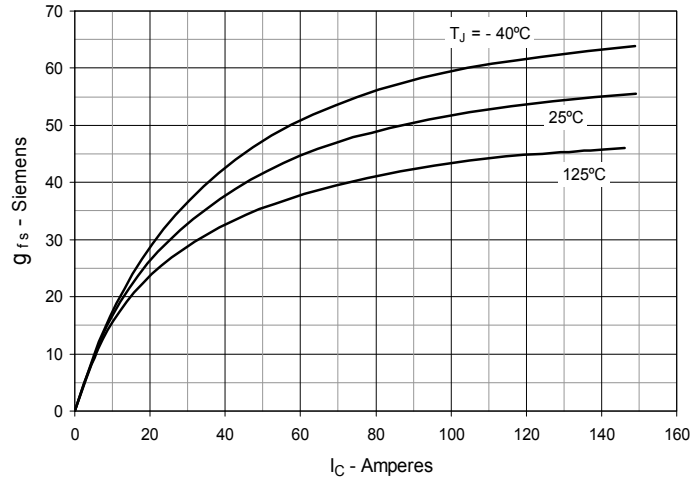


Fig. 8. Gate Charge

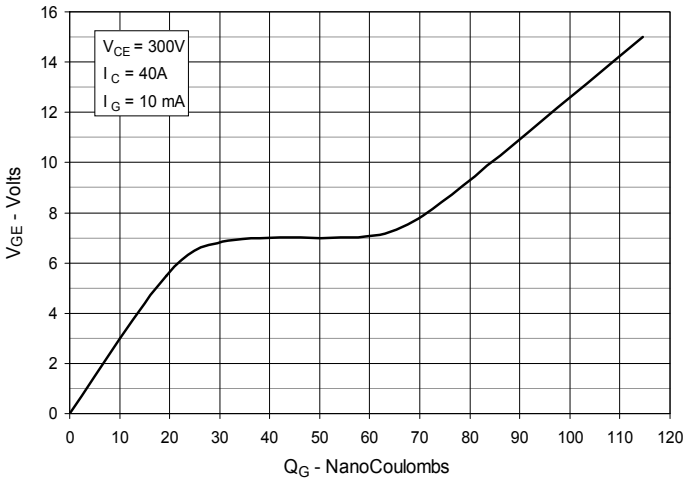


Fig. 9. Capacitance

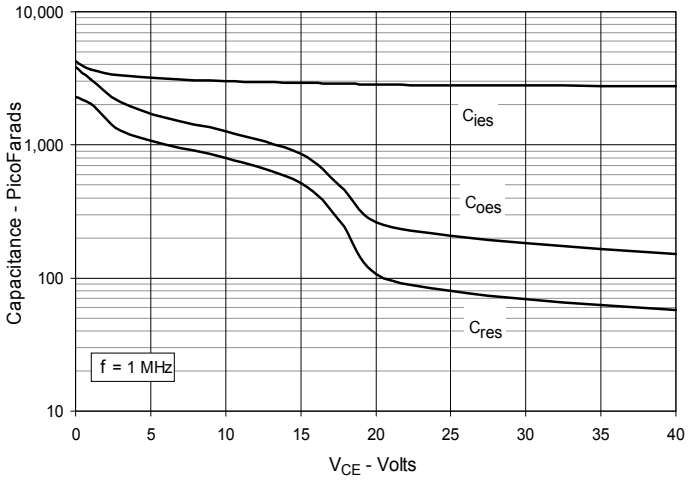


Fig. 10. Reverse-Bias Safe Operating Area

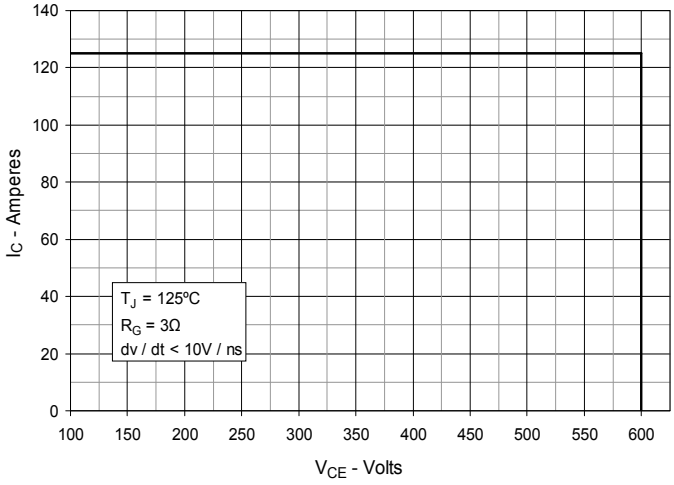


Fig. 11. Maximum Transient Thermal Impedance

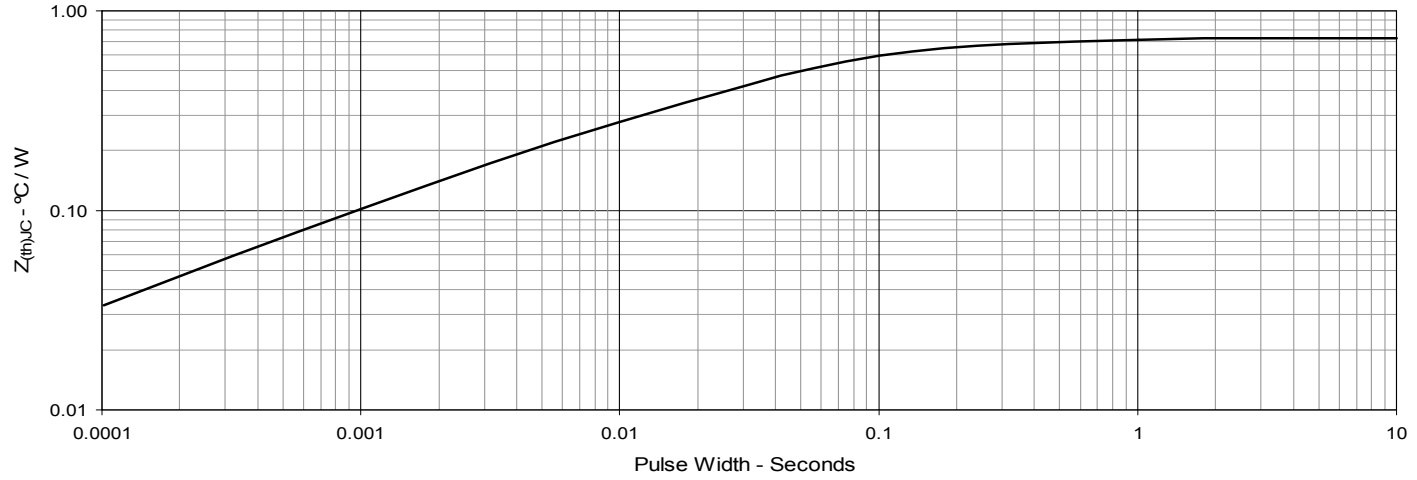


Fig. 12. Inductive Switching Energy Loss vs. Gate Resistance

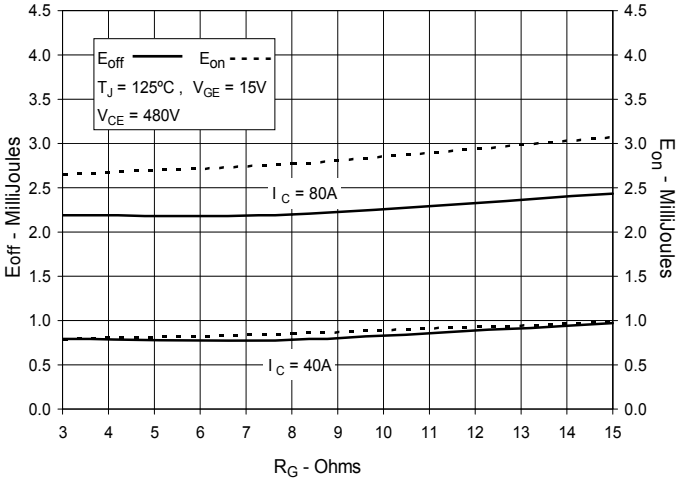


Fig. 13. Inductive Switching Energy Loss vs. Collector Current

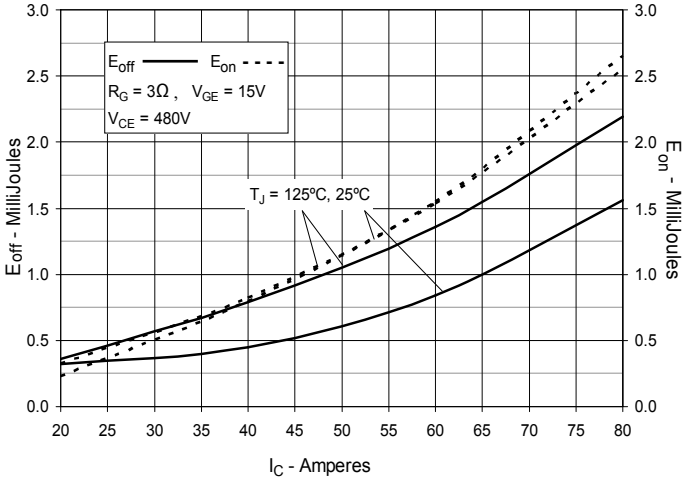


Fig. 14. Inductive Switching Energy Loss vs. Junction Temperature

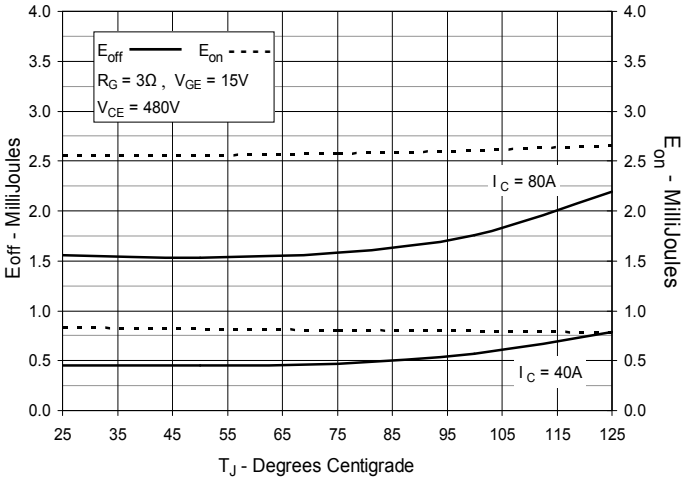


Fig. 15. Inductive Turn-off Switching Times vs. Gate Resistance

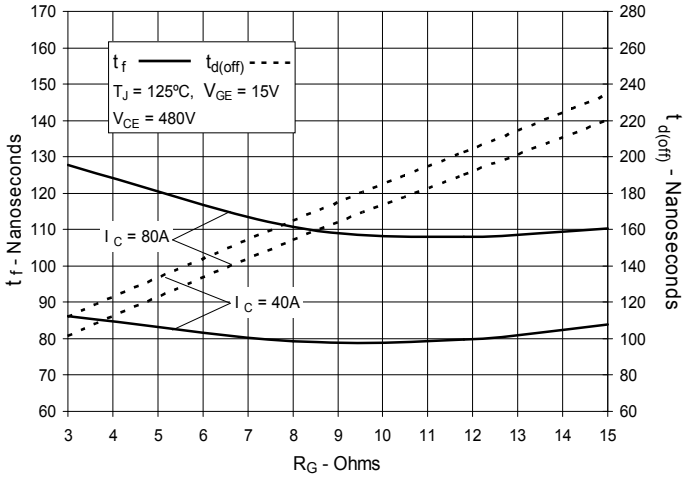


Fig. 16. Inductive Turn-off Switching Times vs. Collector Current

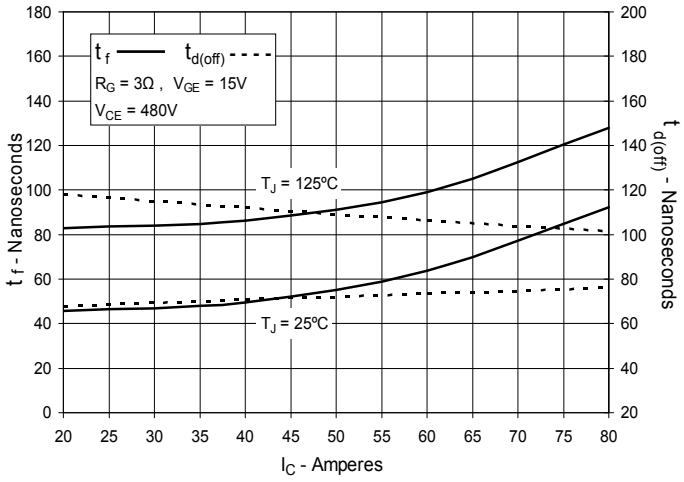


Fig. 17. Inductive Turn-off Switching Times vs. Junction Temperature

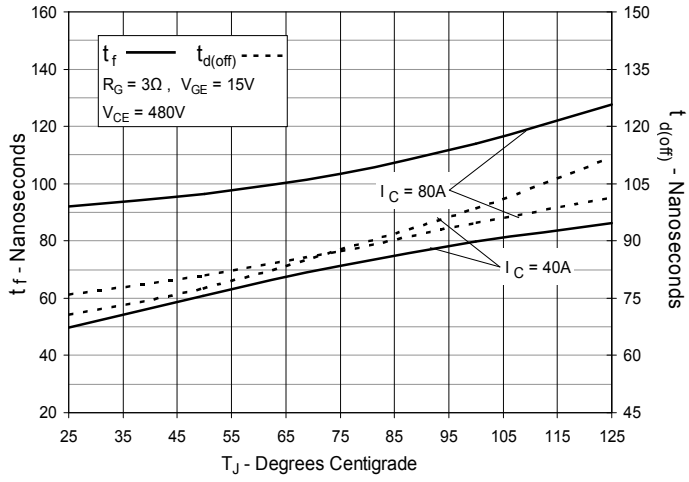


Fig. 18. Inductive Turn-on Switching Times vs. Gate Resistance

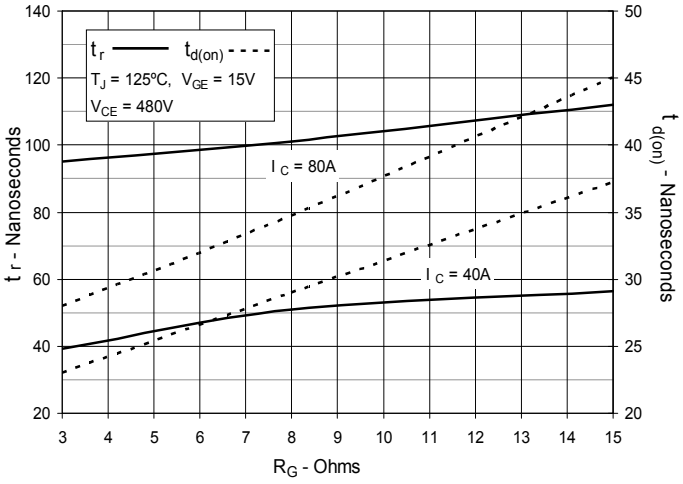


Fig. 19. Inductive Turn-on Switching Times vs. Collector Current

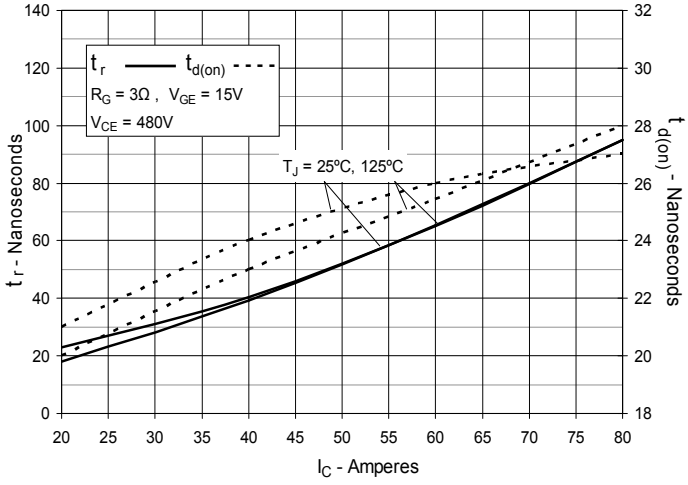


Fig. 20. Inductive Turn-on Switching Times vs. Junction Temperature

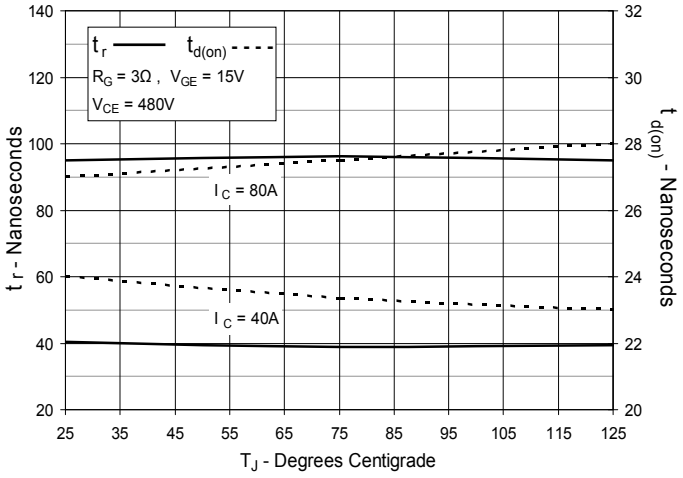


Fig. 21. Forward Current vs. Forward Voltage

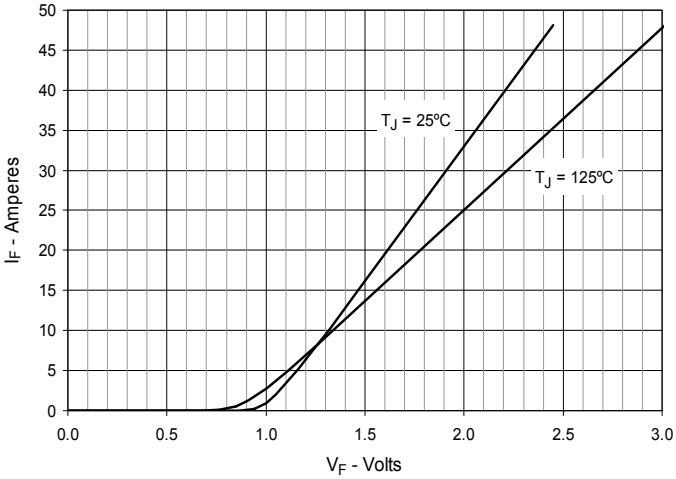
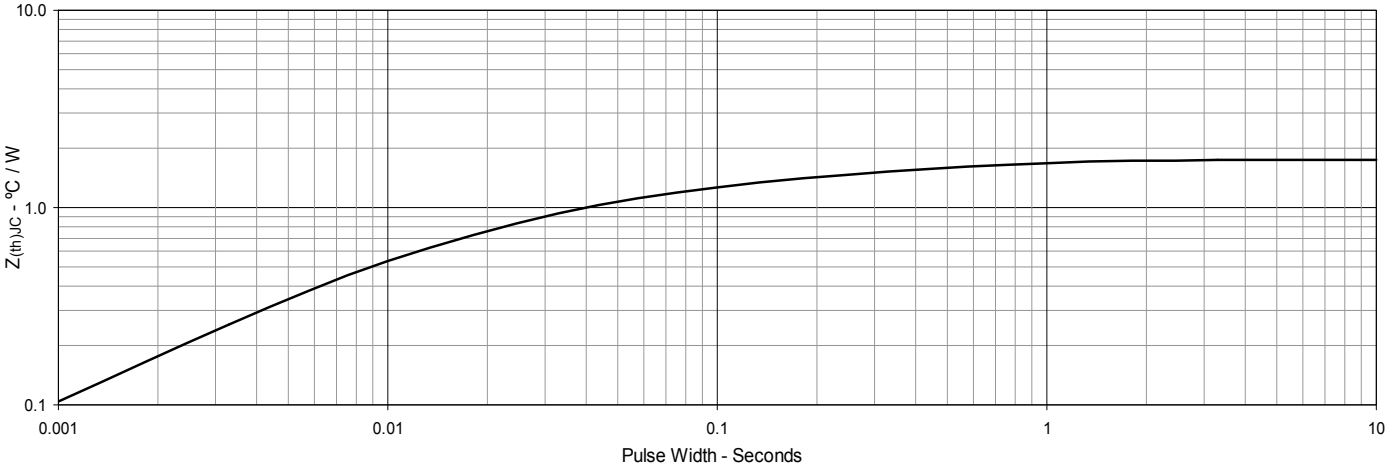


Fig. 22. Maximum Transient Thermal Impedance for Diodes



IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.