

STGW40NC60KD

40 A - 600 V - short circuit rugged IGBT

Features

- Low on-voltage drop (V_{CE(sat)})
- Low C_{res} / C_{ies} ratio (no cross conduction susceptibility)
- Short circuit withstand time 10 µs
- IGBT co-packaged with ultra fast free-wheeling diode

Applications

- High frequency inverters
- Motor drivers



This IGBT utilizes the advanced PowerMESH™ process resulting in an excellent trade-off between switching performance and low on-state behavior.

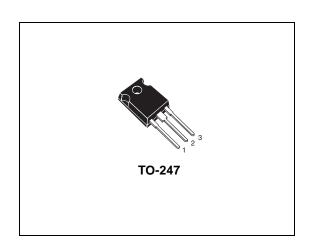


Figure 1. Internal schematic diagram

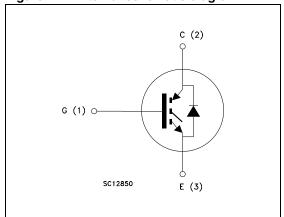


Table 1. Device summary

Order code	Marking Package		Packaging	
STGW40NC60KD	GW40NC60KD	TO-247	Tube	

June 2008 Rev 1 1/14

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STGW40NC60KD Electrical ratings

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CES}	Collector-emitter voltage (V _{GE} = 0)	600	V
I _C ⁽¹⁾	Collector current (continuous) at T _C = 25 °C	70	Α
I _C ⁽¹⁾	Collector current (continuous) at T _C = 100 °C	38	Α
I _{CL} ⁽²⁾	Turn-off latching current	220	Α
I _{CP} ⁽³⁾	Pulsed collector current	220	Α
V _{GE}	Gate-emitter voltage	±20	V
I _F	Diode RMS forward current at T _C = 25 °C	30	Α
I _{FSM}	Surge non repetitive forward current t _p = 10 ms sinusoidal	120	А
P _{TOT}	Total dissipation at T _C = 25 °C 250		W
t _{scw}	Short circuit withstand time, $V_{CE} = 0.5 V_{(BR)CES}$ $T_j = 125$ °C, $R_G = 10 \Omega$, $V_{GE} = 12 V$	10	μs
T _j	Operating junction temperature	- 55 to 150	°C

^{1.} Calculated according to the iterative formula:

$$I_c(T_c) = \frac{T_{J(MAX)} - T_c}{R_{thj-c} \times V_{CE(sat)(MAX)} \cdot (T_c, I_c)}$$

- 2. $V_{clamp} = 80\%, (V_{CES}), T_j = 150^{\circ}C, R_G = 10 \Omega, V_{GE} = 15 V$
- 3. Pulse width limited by max. junction temperature allowed

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
В	Thermal resistance junction-case IGBT max.	0.5	°C/W
R _{thj-case}	Thermal resistance junction-case diode max.		°C/W
R _{thj-amb}	Thermal resistance junction-ambient max	50	°C/W

Electrical characteristics STGW40NC60KD

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)CES}	Collector-emitter breakdown voltage (V _{GE} = 0)	I _C = 1 mA	600			٧
V _{CE(sat)}	Collector-emitter saturation voltage	V_{GE} = 15 V, I_{C} = 30 A V_{GE} = 15 V, I_{C} = 30 A, T_{C} = 125 °C		2.1	2.7	V V
I _{CES}	Collector cut-off current (V _{GE} = 0)	V _{CE} = 600 V V _{CE} = 600 V, T _C = 125 °C			500 5	μA mA
V _{GE(th)}	Gate threshold voltage	$V_{CE} = V_{GE}$, $I_{C} = 250 \mu A$	4.5		6.5	٧
I _{GES}	Gate-emitter cut-off current (V _{CE} = 0)	V _{GE} = ±20 V			±100	nA
g _{fs} ⁽¹⁾	Forward transconductance	V _{CE} = 15 V _, I _C = 30 A		20		S

^{1.} Pulsed: Pulse duration = 300 μ s, duty cycle 1.5%

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{ies} C _{oes} C _{res}	Input capacitance Output capacitance Reverse transfer capacitance	V _{CE} = 25 V, f = 1 MHz, V _{GE} = 0		2870 295 69		pF pF pF
Q _g Q _{ge} Q _{gc}	Total gate charge Gate-emitter charge Gate-collector charge	V_{CE} = 480 V, I_{C} = 30 A, V_{GE} = 15 V (see Figure 18)		135 27 69.5		n C n C

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
t _{d(on)} t _r (di/dt) _{on}	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 480 V, I_{C} = 30 A R_{G} =10 Ω V _{GE} = 15 V, (see Figure 17)		46 18.5 1530		ns ns A/µs
t _{d(on)} t _r (di/dt) _{on}	Turn-on delay time Current rise time Turn-on current slope	$V_{CC} = 480 \text{ V, } I_{C} = 30 \text{ A}$ $R_{G} = 10 \Omega \text{ V}_{GE} = 15 \text{ V,}$ $T_{C} = 125 \text{ °C } \textit{(see Figure 17)}$		45 19 1400		ns ns A/µs
$t_r(V_{off})$ $t_d(_{off})$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC} = 480 V, I_{C} = 30 A R_{G} =10 Ω V _{GE} = 15 V, (see Figure 17)		38 164 87		ns ns ns
t _r (V _{off}) t _d (_{off}) t _f	Off voltage rise time Turn-off delay time Current fall time	$V_{cc} = 480 \text{ V, } I_{C} = 30 \text{ A,}$ $R_{G} = 10 \Omega \text{ V}_{GE} = 15 \text{ V}$ $T_{C} = 125 ^{\circ}\text{C}$ (see Figure 17)		70 208 130		ns ns ns

Table 7. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit
Eon E _{off} ⁽¹⁾ E _{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	$V_{CC} = 480 \text{ V}, I_C = 30 \text{ A}$ $R_G = 10 \Omega V_{GE} = 15 \text{ V},$ (see Figure 17)		595 716 311		μJ μJ μJ
Eon E _{off} ⁽¹⁾ E _{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 480 V, I_{C} = 30 A R_{G} = 10 Ω V _{GE} = 15 V, T_{C} = 125 °C (see Figure 17)		808 1200 2008		μJ μJ μJ

^{1.} Turn-off losses include also the tail of the collector current.

Electrical characteristics STGW40NC60KD

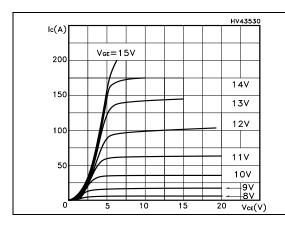
Table 8. Collector-emitter diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _F	Forward on-voltage	I _F = 30 A I _F = 30 A, T _C = 125 °C		2.4 1.8		V V
t _{rr} Q _{rr} I _{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_F = 30 \text{ A}, V_R = 50 \text{ V},$ $di/dt = 100 \text{ A}/\mu\text{s}$ (see Figure 20)		45 56 2.55		ns nC A
t _{rr} Q _{rr} I _{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_F = 30 A,V _R = 50 V, T_C =125 °C, di/dt = 100 A/ μ s (see Figure 20)		100 290 5.8		ns nC A

2.1 Electrical characteristics (curves)

Figure 2. Output characteristics

Figure 3. Transfer characteristics



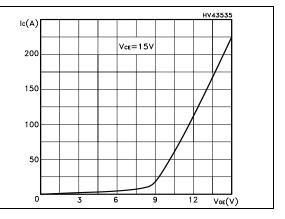
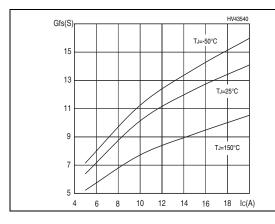


Figure 4. Transconductance

Figure 5. Collector-emitter on voltage vs temperature



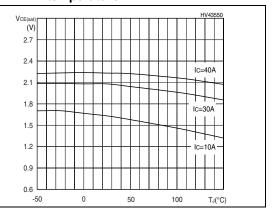
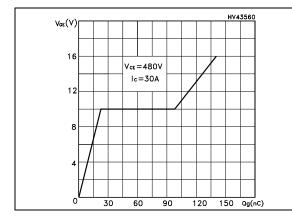
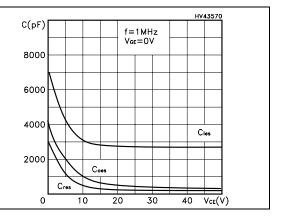


Figure 6. Gate charge vs gate-source voltage Figure 7. Capacitance variations

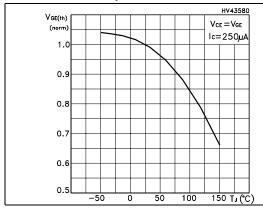




Electrical characteristics STGW40NC60KD

Figure 8. Normalized gate threshold voltage Figure 8. vs temperature

Figure 9. Collector-emitter on voltage vs collector current



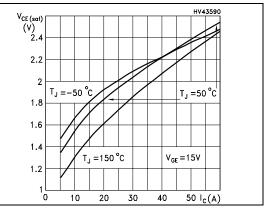
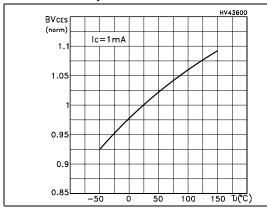


Figure 10. Normalized breakdown voltage vs temperature

Figure 11. Switching losses vs temperature



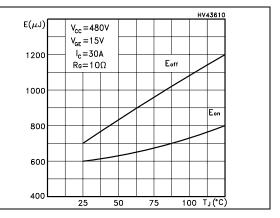
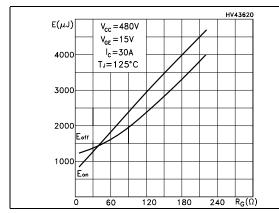


Figure 12. Switching losses vs gate resistance Figure 13. Switching losses vs collector current



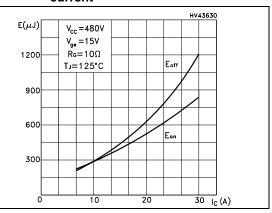


Figure 14. Thermal Impedance

Figure 15. Turn-off SOA

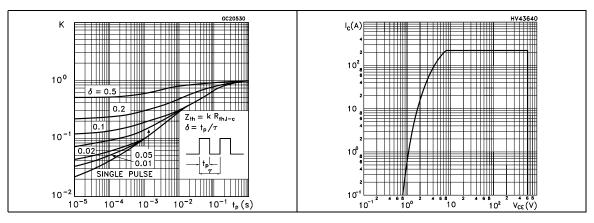
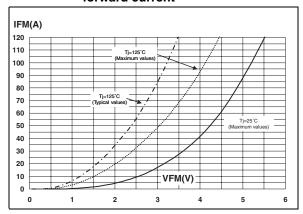


Figure 16. Forward voltage drop versus forward current



Test circuit STGW40NC60KD

3 Test circuit

Figure 17. Test circuit for inductive load switching

Figure 18. Gate charge test circuit

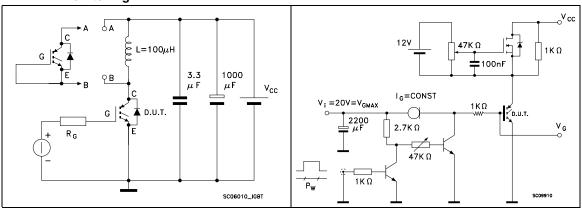
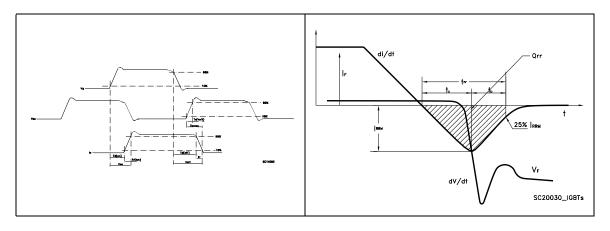


Figure 19. Switching waveforms

Figure 20. Diode recovery times waveform

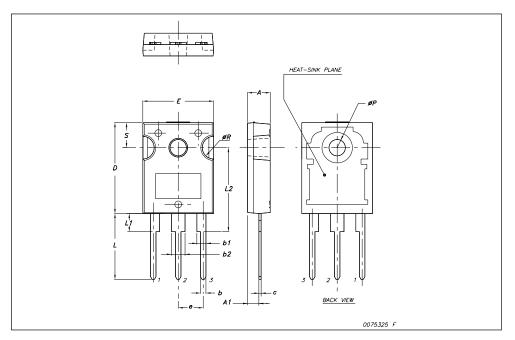


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-247 Mechanical data

Dim.		mm.	
DIII.	Min.	Тур	Max.
Α	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
С	0.40		0.80
D	19.85		20.15
E	15.45		15.75
е		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øΡ	3.55		3.65
øR	4.50		5.50
S		5.50	



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STGW40NC60KD Revision history

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
11-Jun-2008	1	Initial release

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