# Field Programmable PECL Oscillator

*• 9.6 x 11.4 SMD*

## Applications

## Series CPPE9

### Part Numbering Example: CPPE9 LZ A5 B6 100.0

| CPPE9 | L | Z | A5 | B6 | 100.000 |
|---|---|---|---|---|---|
| SERIES | VOLTAGE | ADDED FEATURES | OPERATING TEMP | STABILITY | FREQUENCY |
| | Blank = 5 V<br>L = 3.3 V | Blank = Bulk<br>T = Tube<br>Z = Tape/Reel | Blank = 0 – +70 °C<br>A5 = -20 – +70 °C<br>A7 = -40 – +85 °C | B6 = ±100 ppm<br>BP = ±50 ppm | 1.000 – 133.0 MHz |

| Specifications: | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **Frequency Range:** | 1.0 | | 133.0 | MHz |
| **Available Stability Options:** | -100<br>-50 | | 100<br>50 | ppm<br>ppm |
| **Prog. Supply Voltage:** | 4.75<br>3.135 | 5.0<br>3.3 | 5.25<br>3.465 | V<br>V |
| **Operating Temperature** Range Options: | 0<br>-20<br>-40 | | 70<br>70<br>85 | °C<br>°C<br>°C |
| **Storage Temperature:** | -55 | | 125 | °C |
| **Aging (PPM/1st Year):** Ta=25C, Vdd=3.3V | | | ±5 | |
| **Clock Rise Time** @ 20/80 % PECL | | 0.6 | 1.5 | ns |
| **Clock Fall Time** @ 80/20 % PECL | | 0.5 | 1.5 | ns |
| **Output Level:** | PECL | | | |

Tristate internal pull up, output active when high

Notes: Recommended 0.01 µF bypass capacitor from Vdd to Gnd. Capacitor should be as close to oscillator as possible.

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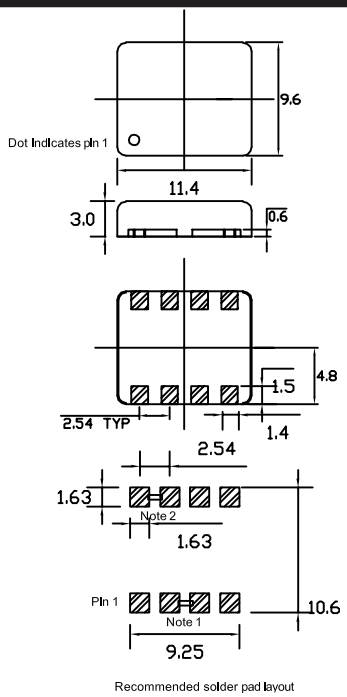
## CPPE9

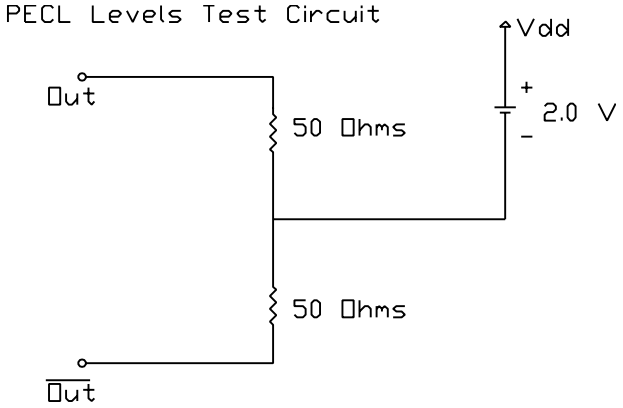



Recommended solder pad layout

**PIN FUNCTION**
PIN 1 OE
PIN 2 CONNECT TO PIN 3
PIN 3 CONNECT TO PIN 2
PIN 4 GND
PIN 5 PECL-
PIN 6 PECL+
PIN 7 VDD
PIN 8 VDD

Note 1: Connect pin 2 to pin 3
Note 2: Connect pin 7 to pin 8

## LEVELS TEST CIRCUIT




## OUTPUT SKEW