advanced

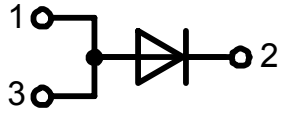
Schottky

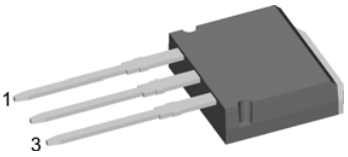
V_{RRM} = 45 V
I_{FAV} = 15 A
V_F = 0.63 V

High Performance Schottky Diode
Low Loss and Soft Recovery
Single Diode

Part number *(Marking on product)*

DSA 15 IM 45IB





Features / Advantages:

- Very low Vf
- Extremely low switching losses
- Low Irm-values
- Improved thermal behaviour
- High reliability circuit operation
- Low voltage peaks for reduced protection circuits
- Low noise switching
- Low losses

Applications:

- Rectifiers in switch mode power supplies (SMPS)
- Free wheeling diode in low voltage converters

Package:

TO-262 (I2Pak)

- Industry standard outline
- Epoxy meets UL 94V-0
- RoHS compliant

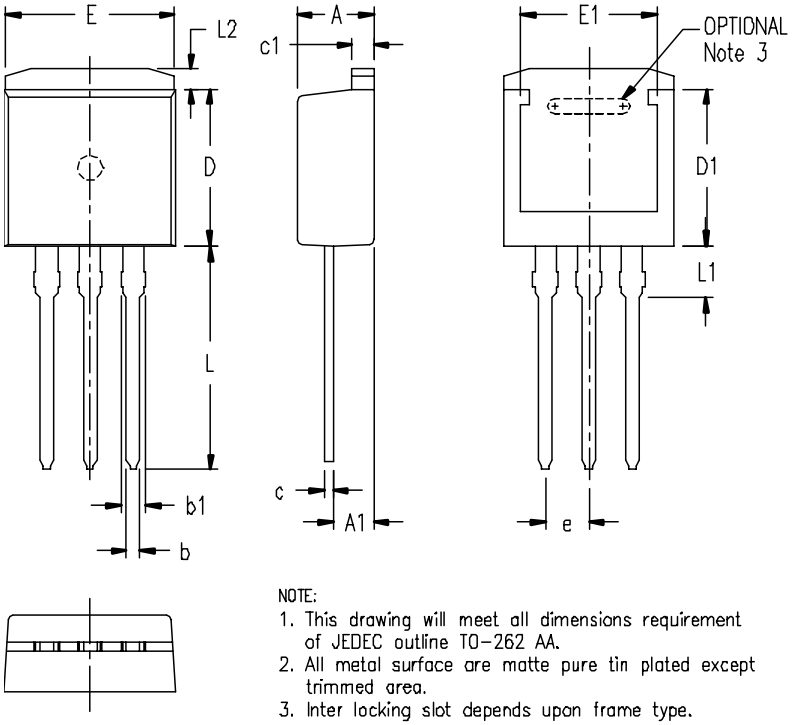
Symbol	Definition	Conditions		Ratings min.	typ.	max.	Unit
V_{RRM}	*max. repetitive reverse voltage*		T_{VJ} = 25 °C			45	V
I_R	*reverse current*	V_R = 45 V	T_{VJ} = 25 °C			0.3	mA
		V_R = 45 V	T_{VJ} = 125 °C			2.5	mA
V_F	*forward voltage*	I_F = 15 A	T_{VJ} = 25 °C			0.75	V
		I_F = 30 A				0.91	V
		I_F = 15 A	T_{VJ} = 125 °C			0.63	V
		I_F = 30 A				0.79	V
I_{FAV}	*average forward current*	rectangular, d = 0.5	T_C = 155 °C			15	A
V_{F0}	*threshold voltage* } *for power loss calculation only*		T_{VJ} = 175 °C			0.42	V
r_F	*slope resistance* }					9.9	mΩ
R_{thJC}	*thermal resistance junction to case*					1.75	K/W
T_{VJ}	*virtual junction temperature*			-55		175	°C
P_{tot}	*total power dissipation*		T_C = 25 °C			85	W
I_{FSM}	*max. forward surge current*	t_p = 10 ms (50 Hz), sine	T_{VJ} = 45 °C			140	A
C_J	*junction capacitance*	V_R = V; f = 1 MHz	T_{VJ} = 25 °C				pF
E_{AS}	*non-repetitive avalanche energy*	I_{AS} = A; L = 100 µH	T_{VJ} = 25 °C			tbd	mJ
I_{AR}	*repetitive avalanche current*	$V_A = 1.5 \cdot V_R$ typ.; f = 10 kHz				tbd	A

advanced

Symbol	Definition	Conditions	Ratings min.	typ.	max.	Unit
I_{RMS}	*RMS current*	per pin*			35	A
R_{thCH}	*thermal resistance case to heatsink*			0.50		K/W
M_D	*mounting torque*					Nm
F_C	*mounting force with clip*		20		60	N
T_{stg}	*storage temperature*		-55		150	°C
Weight				2		g

* Irms is typically limited by: 1. pin-to-chip resistance; or by 2. current capability of the chip.
In case of 1, a common cathode/anode configuration and a non-isolated backside, the whole current capability can be used by connecting the backside.

Outlines TO-262 (I2Pak)



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.160	.190	4.06	4.83
A1	.080	.110	2.03	2.79
b	.025	.035	0.64	0.88
b1	.025	.039	1.14	1.40
c	.018	.025	0.46	0.64
c1	.045	.055	1.14	1.40
D	.340	.380	8.64	9.65
D1	.270	.290	6.86	7.37
E	.380	.405	9.65	10.29
E1	.245	.320	6.22	8.13
e	.100 BSC		2.54 BSC	
L	.500	.560	12.70	14.22
L1	.100	.125	2.54	3.18
L2	.040	.055	1.02	1.40

NOTE:
1. This drawing will meet all dimensions requirement of JEDEC outline TO-262 AA.
2. All metal surface are matte pure tin plated except trimmed area.
3. Inter locking slot depends upon frame type.