

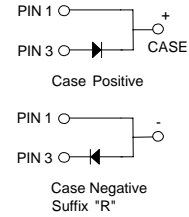
# FES16AT - FES16JT



TO-220AC

## Features

- Low forward voltage drop.
- High surge current capacity.
- High current capability.
- High reliability.



## Fast Rectifiers (Glass Passivated)

### Absolute Maximum Ratings\*

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Value								Units
		16AT	16BT	16CT	16DT	16FT	16GT	16HT	16JT	
$V_{RRM}$	Maximum Repetitive Reverse Voltage	50	100	150	200	300	400	500	600	V
$I_{F(AV)}$	Average Rectified Forward Current, .375" lead length @ $T_A = 100^\circ\text{C}$	16								A
$I_{FSM}$	Non-repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave	250								A
$T_{stg}$	Storage Temperature Range	-65 to +150								V
$T_J$	Operating Junction Temperature	-65 to +150								pF

\*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

## Thermal Characteristics

Symbol	Parameter	Value	Units
$P_D$	Power Dissipation	7.81	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	16	$^\circ\text{C}/\text{W}$
$R_{\theta JL}$	Thermal Resistance, Junction to Lead	1.2	$^\circ\text{C}/\text{W}$

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Device								Units
		16AT	16BT	16CT	16DT	16FT	16GT	16HT	16JT	
$V_F$	Forward Voltage @ 8.0A	0.95				1.3		1.5		V
$t_{rr}$	Reverse Recovery Time $I_F = 0.5\text{ A}, I_R = 1.0\text{ A}, I_{RR} = 0.25\text{ A}$	35				50				ns
$I_R$	Reverse Current @ rated $V_R$ $T_A = 25^\circ\text{C}$ $T_A = 100^\circ\text{C}$	10				500				$\mu\text{A}$ $\mu\text{A}$
$C_T$	Total Capacitance $V_R = 4.0, f = 1.0\text{ MHz}$	170						145		pF

## Typical Characteristics

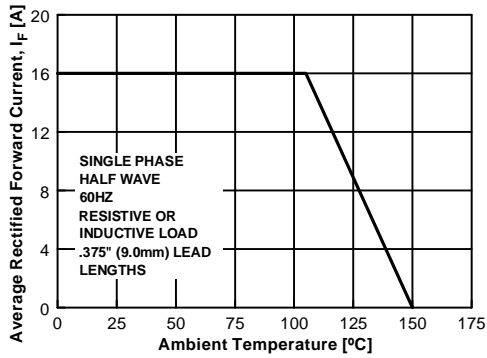


Figure 1. Forward Current Derating Curve

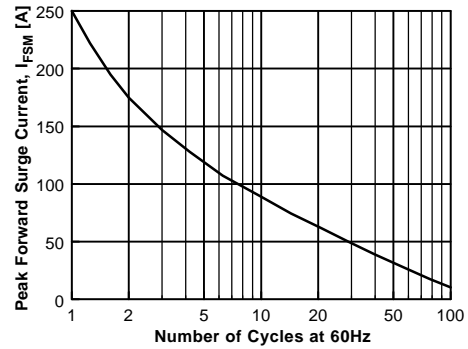


Figure 2. Non-Repetitive Surge Current

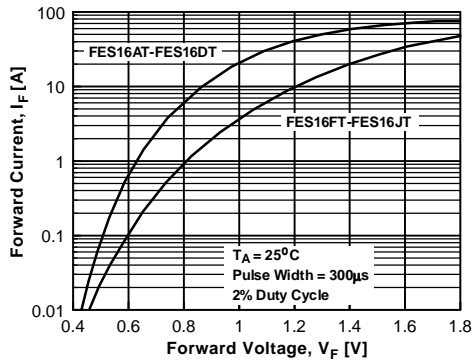


Figure 3. Forward Voltage Characteristics

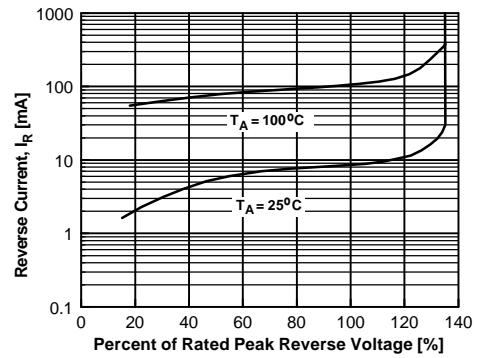


Figure 4. Reverse Current vs Reverse Voltage

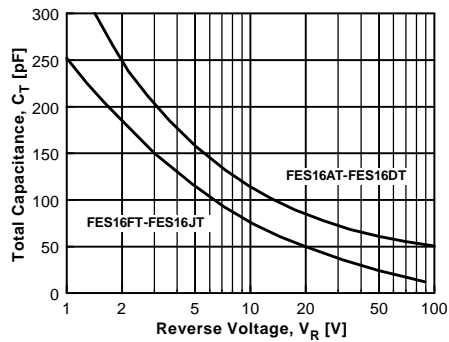
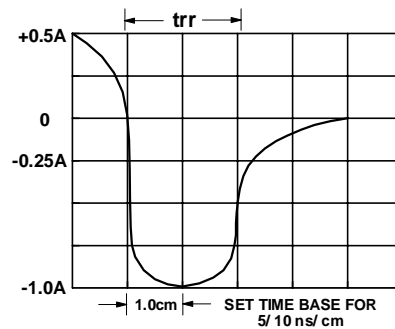
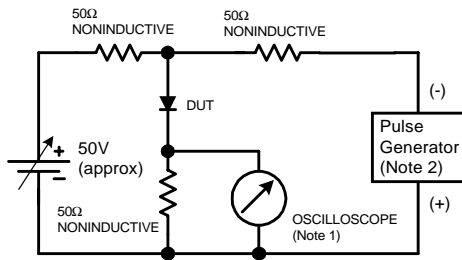


Figure 5. Total Capacitance



Reverse Recovery Time Characteristic and Test Circuit Diagram

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