HSMP-382x, 482x
Surface Mount RF PIN Switch and Limiter Diodes

Data Sheet

Lead (Pb) Free
RoHS 6 fully
compliant

Description/Applications

The HSMP-382x series is optimized for switching applications where ultra-low resistance is required. The HSMP-482x diode is ideal for limiting and low inductance switching applications up to 1.5 GHz.

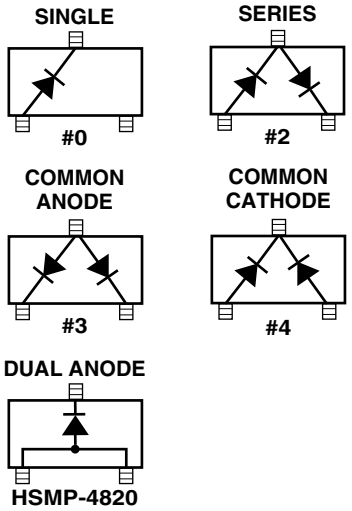
A SPICE model is not available for PIN diodes as SPICE does not provide for a key PIN diode characteristic, carrier lifetime.

Features

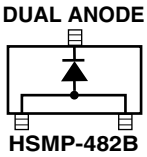
- Diodes Optimized for:
  Low Current Switching
  Low Distortion Attenuating
- Power Limiting/Circuit Protection
- Surface Mount SOT-23 and SOT-323 Packages
  Single and Dual Versions
  Tape and Reel Options Available
- Low Failure in Time (FIT) Rate[1]
- Lead-free

Note:
1. For more information see the Surface Mount PIN Reliability Data Sheet.

Package Lead Code Identification, SOT-23 (Top View)



Package Lead Code Identification, SOT-323 (Top View)



Absolute Maximum Ratings[1] T_C = +25°C

Symbol	Parameter	Unit	SOT-23	SOT-323
I_f	Forward Current (1 µs Pulse)	Amp	1	1
P_{IV}	Peak Inverse Voltage	V	50	50
T_j	Junction Temperature	°C	150	150
T_{stg}	Storage Temperature	°C	-65 to 150	-65 to 150
θ_{jc}	Thermal Resistance[2]	°C/W	500	150

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. T_C = +25°C, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

Electrical Specifications T_C = 25°C

Part Number HSMP-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Maximum Total Capacitance C_T (pF)
3820	F0	0	Single	50	0.6	0.8
3822	F2	2	Series			
3823	F3	3	Common Anode			
3824	F4	4	Common Cathode			
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10$ µA	f = 100 MHz I_F = 10 mA	f = 1 MHz V_R = 20 V

High Frequency (Low Inductance, 500 MHz – 3 GHz) PIN Diodes

Part Number HSMP-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Typical Total Capacitance C_T (pF)	Maximum Total Capacitance C_T (pF)	Typical Total Inductance L_T (nH)
4820	FA	A	Dual Anode	50	0.6	0.75	1.0	1.0
482B	FA	A	Dual Anode					
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10$ µA	I_F = 10 mA	f = 1 MHz V_R = 20 V	f = 1 MHz V_R = 0 V	f = 500 MHz – 3 GHz

Typical Parameters at T_C = 25°C

Part Number HSMP-	Series Resistance R_S (Ω)	Carrier Lifetime τ (ns)	Reverse Recovery Time T_{rr} (ns)	Total Capacitance C_T (pF)
382x	1.5	70	7	0.60 @ 20 V
Test Conditions	f = 100 MHz I_F = 10 mA	I_F = 10 mA	V_R = 10 V I_F = 20 mA 90% Recovery	

Typical Parameters at T_C = 25°C (unless otherwise noted), Single Diode

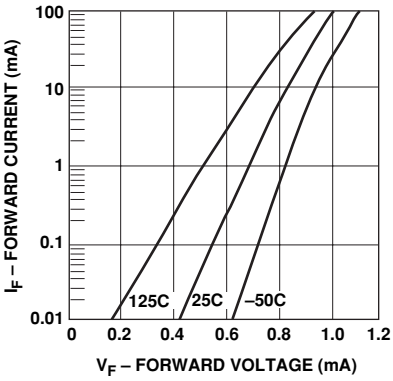


Figure 1. Forward Current vs. Forward Voltage.

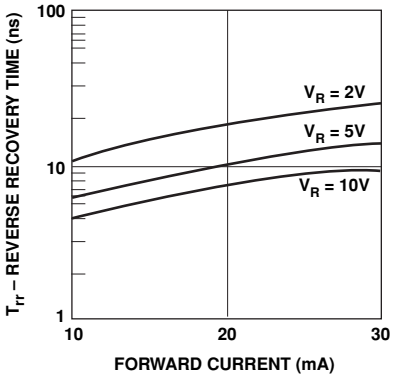


Figure 2. Reverse Recovery Time vs. Forward Current for Various Reverse Voltages.

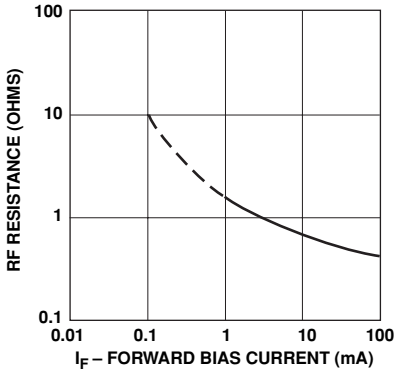


Figure 3. RF Resistance at 25C vs. Forward Bias Current.

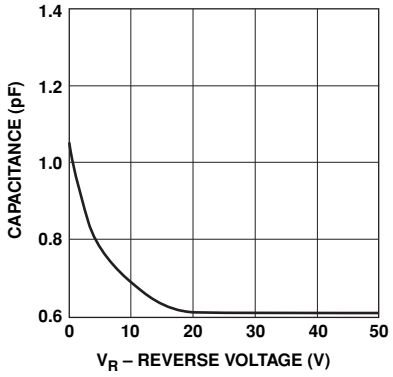


Figure 4. Capacitance vs. Reverse Voltage.

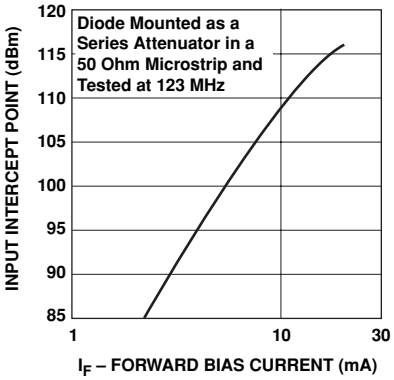


Figure 5. 2nd Harmonic Input Intercept Point vs. Forward Bias Current.

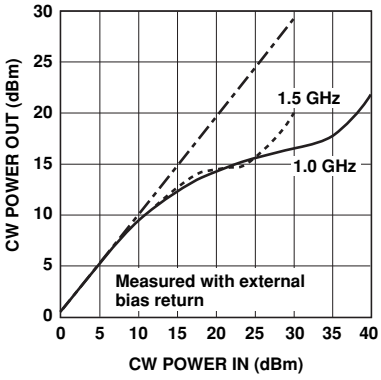


Figure 6. Large Signal Transfer Curve of the HSMP-482x Limiter.

Typical Applications for Multiple Diode Products

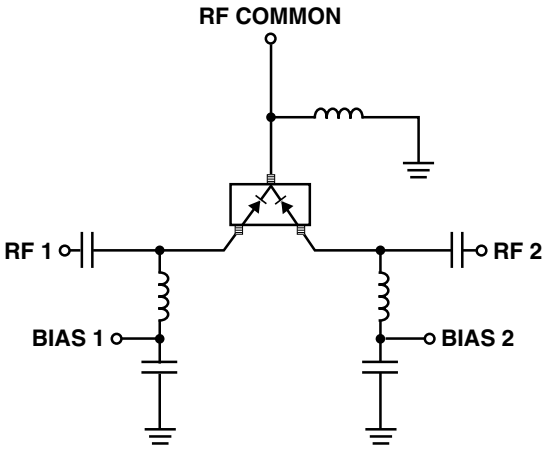


Figure 7. Simple SPDT Switch, Using Only Positive Current.

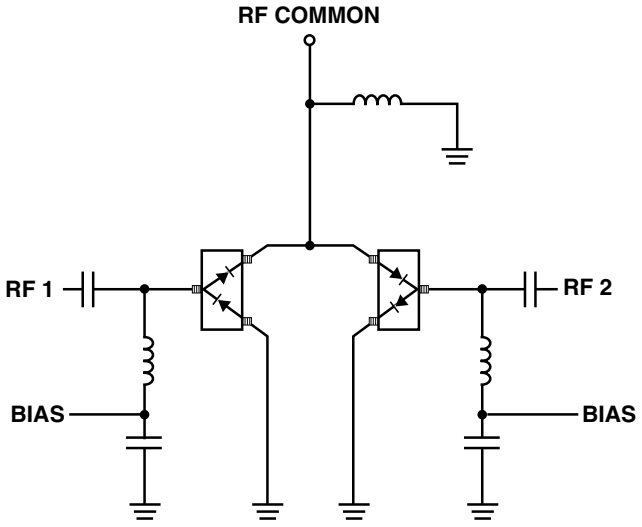


Figure 8. High Isolation SPDT Switch, Dual Bias.

Typical Applications for Multiple Diode Products, continued

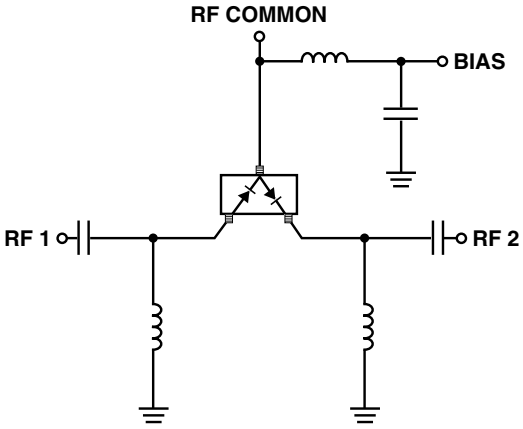


Figure 9. Switch Using Both Positive and Negative Bias Current.

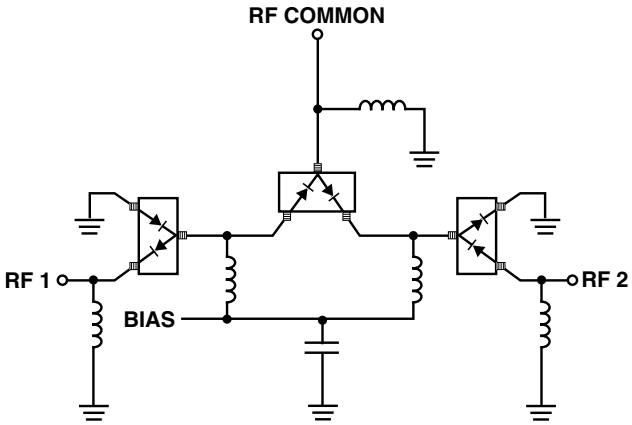


Figure 10. Very High Isolation SPDT Switch, Dual Bias.

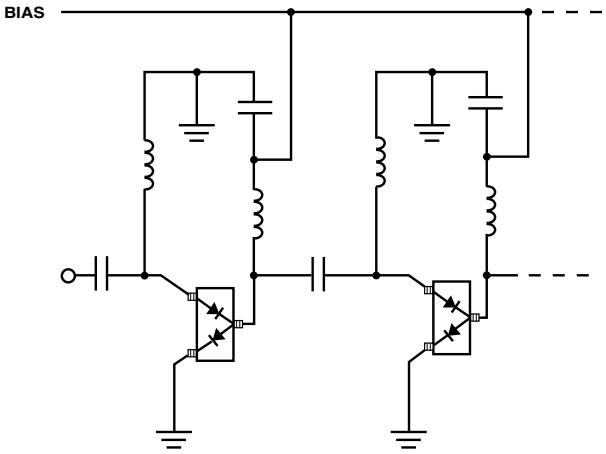


Figure 11. High Isolation SPST Switch (Repeat Cells as Required.

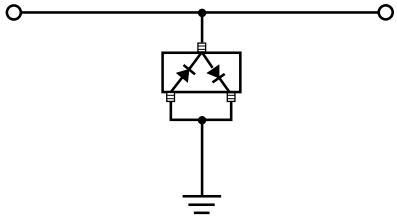


Figure 12. Power Limiter Using HSMP-3822 Diode Pair. See Application Note 1050 for details.

Typical Applications for HSMP-482x Low Inductance Series

Microstrip Series Connection for HSMP-482x Series

In order to take full advantage of the low inductance of the HSMP-482x series when using them in series applications, both lead 1 and lead 2 should be connected together, as shown in Figure 14.

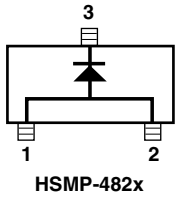


Figure 13. Internal Connections.

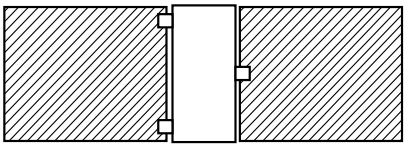


Figure 14. Circuit Layout.

Microstrip Shunt Connections for HSMP-482x Series

In Figure 15, the center conductor of the microstrip line is interrupted and leads 1 and 2 of the HSMP-482x diode are placed across the resulting gap. This forces the 0.5 nH lead inductance of leads 1 and 2 to appear as part of a low pass filter, reducing the shunt parasitic inductance and increasing the maximum available attenuation. The 0.3 nH of shunt inductance external to the diode is created by the via holes, and is a good estimate for 0.032" thick material.

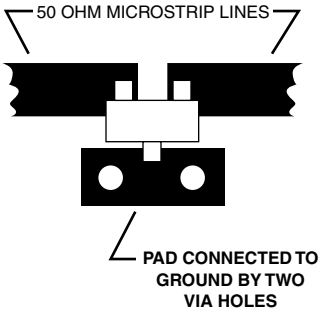


Figure 15. Circuit Layout, HSMP-482x Limiter.

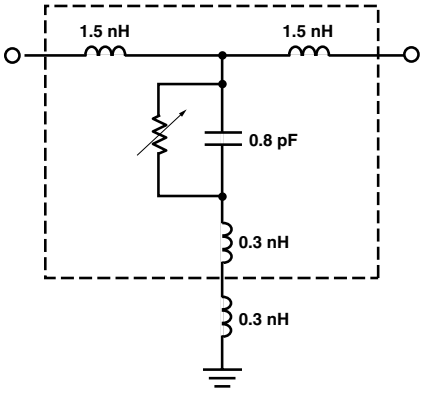


Figure 16. Equivalent Circuit.

Co-Planar Waveguide Shunt Connection for HSMP-482x Series

Co-Planar waveguide, with ground on the top side of the printed circuit board, is shown in Figure 17. Since it eliminates the need for via holes to ground, it offers lower shunt parasitic inductance and higher maximum attenuation when compared to a microstrip circuit. See AN1050 for details.

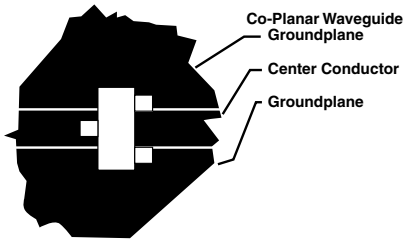


Figure 17. Circuit Layout.

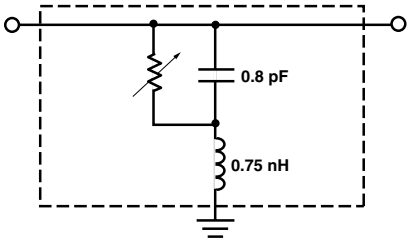


Figure 18. Equivalent Circuit.

Assembly Information

SOT-323 PCB Footprint

A recommended PCB pad layout for the miniature SOT-323 (SC-70) package is shown in Figure 19 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the performance.

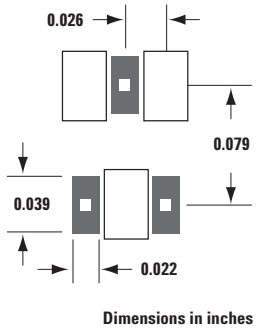


Figure 19. Recommended PCB Pad Layout for Avago's SC70 3L/SOT-323 Products.

SOT-23 PCB Footprint

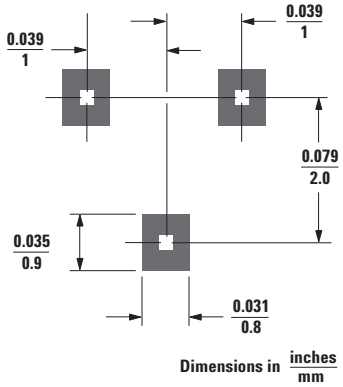


Figure 20. Recommended PCB Pad Layout for Avago's SOT-23 Products.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-323/-23 package, will reach solder reflow temperatures faster than those with a greater mass.

Avago's diodes have been qualified to the time-temperature profile shown in Figure 21. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 260°C.

These parameters are typical for a surface mount assembly process for Avago diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

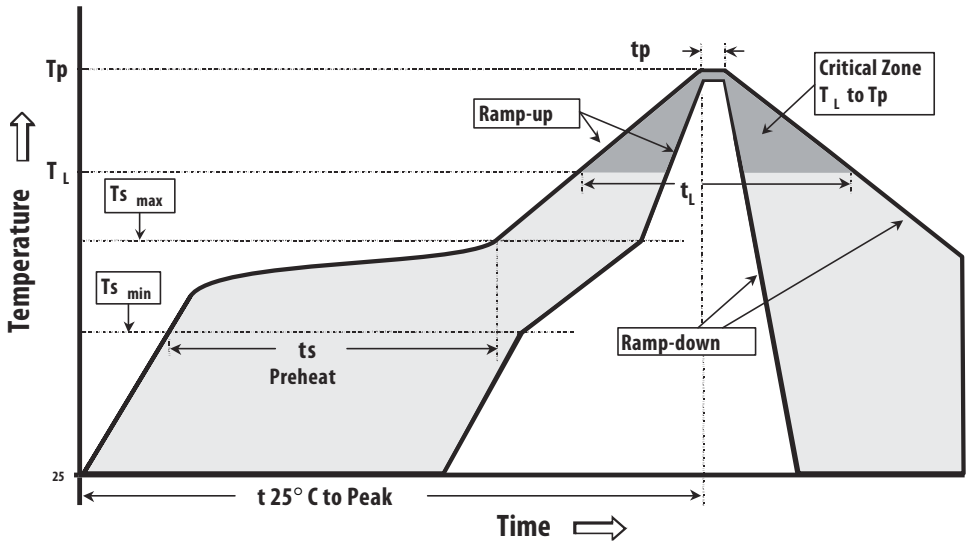


Figure 21. Surface Mount Assembly Profile.

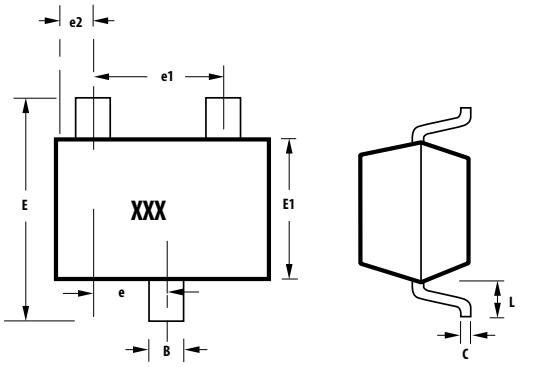
Lead-Free Reflow Profile Recommendation (IPC/JEDEC J-STD-020C)

Reflow Parameter		Lead-Free Assembly
Average ramp-up rate (Liquidus Temperature ($T_{S(max)}$ to Peak)		3°C/ second max
Preheat	Temperature Min ($T_{S(min)}$)	150°C
	Temperature Max ($T_{S(max)}$)	200°C
	Time (min to max) (t_S)	60-180 seconds
Ts(max) to TL Ramp-up Rate		3°C/second max
Time maintained above:	Temperature (T_L)	217°C
	Time (t_L)	60-150 seconds
Peak Temperature (T_P)		260 +0/-5°C
Time within 5 °C of actual Peak temperature (t_P)		20-40 seconds
Ramp-down Rate		6°C/second max
Time 25 °C to Peak Temperature		8 minutes max

Note 1: All temperatures refer to topside of the package, measured on the package body surface

Package Dimensions

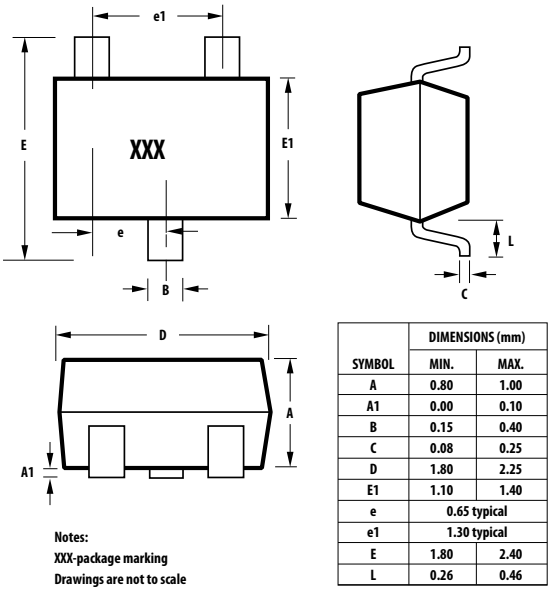
Outline 23 (SOT-23)



SYMBOL	DIMENSIONS (mm) MIN.	MAX.
A	0.79	1.20
A1	0.000	0.100
B	0.30	0.54
C	0.08	0.20
D	2.73	3.13
E1	1.15	1.50
e	0.89	1.02
e1	1.78	2.04
e2	0.45	0.60
E	2.10	2.70
L	0.45	0.69

Notes:
XXX-package marking
Drawings are not to scale

Outline SOT-323 (SC-70)



SYMBOL	DIMENSIONS (mm) MIN.	MAX.
A	0.80	1.00
A1	0.00	0.10
B	0.15	0.40
C	0.08	0.25
D	1.80	2.25
E1	1.10	1.40
e	0.65 typical	
e1	1.30 typical	
E	1.80	2.40
L	0.26	0.46

Notes:
XXX-package marking
Drawings are not to scale

Package Characteristics

Lead Material ..... Copper (SOT-323); Alloy 42 (SOT-23)
Lead Finish ..... Tin 100% (Lead-free option)
Maximum Soldering Temperature ..... 260°C for 5 seconds
Minimum Lead Strength ..... 2 pounds pull
Typical Package Inductance ..... 2 nH
Typical Package Capacitance ..... 0.08 pF (opposite leads)

Ordering Information

Specify part number followed by option. For example:

HSMP - 382x - XXX

- XXX: Bulk or Tape and Reel Option
- 382x: Part Number; x = Lead Code
- HSMP: Surface Mount PIN

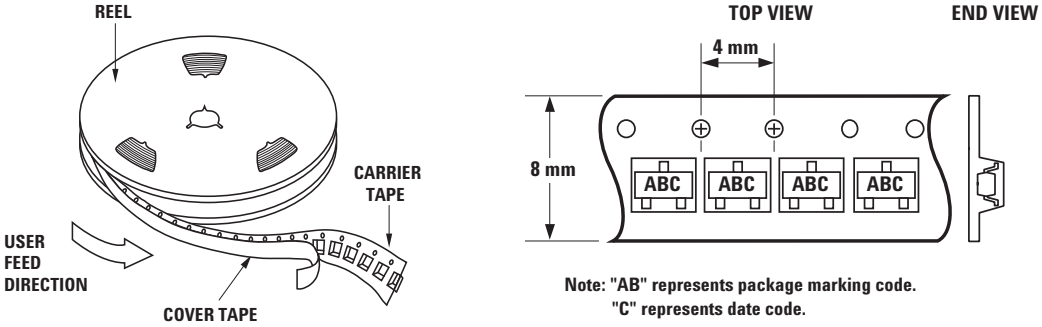
Option Descriptions

-BLKG = Bulk, 100 pcs. per antistatic bag
-TR1G = Tape and Reel, 3000 devices per 7" reel
-TR2G = Tape and Reel, 10,000 devices per 13" reel

Tape and Reeling conforms to Electronic Industries RS-481, "Taping of Surface Mounted Components for Automated Placement."

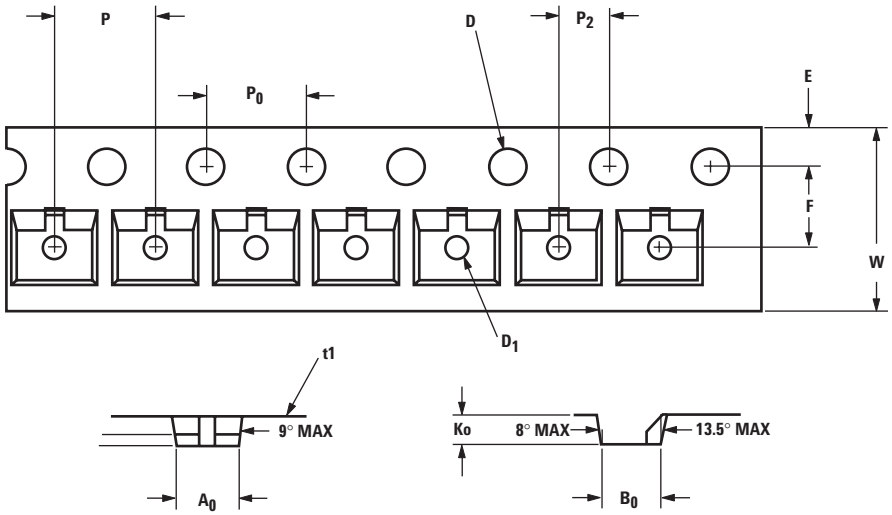
Device Orientation

For Outlines SOT-23/323



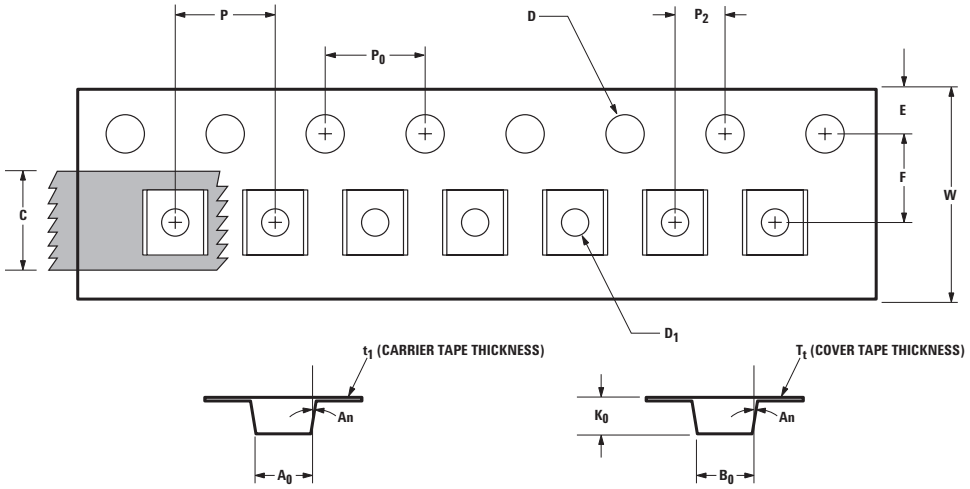
Note: "AB" represents package marking code.
"C" represents date code.

Tape Dimensions and Product Orientation
For Outline SOT-23



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	3.15 ± 0.10	0.124 ± 0.004
	WIDTH	B_0	2.77 ± 0.10	0.109 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.05	0.039 ± 0.002
PERFORATION	DIAMETER	D	1.50 + 0.10	0.059 + 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 +0.30 –0.10	0.315 +0.012 –0.004
	THICKNESS	t1	0.229 ± 0.013	0.009 ± 0.0005
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

Tape Dimensions and Product Orientation
For Outline SOT-323



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.40 ± 0.10	0.094 ± 0.004
	WIDTH	B_0	2.40 ± 0.10	0.094 ± 0.004
	DEPTH	K_0	1.20 ± 0.10	0.047 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.254 ± 0.02	0.0100 ± 0.0008
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002
ANGLE	FOR SOT-323 (SC70-3 LEAD)	An	8°C MAX	
	FOR SOT-363 (SC70-6 LEAD)		10°C MAX	

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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