- **1N5283 THRU 1N5314 AVAILABLE IN JANHC AND JANKC PER MIL-PRF-19500/463**
- **CURRENT REGULATOR CHIPS**
- **ALL JUNCTIONS COMPLETELY PROTECTED WITH SILICON DIOXIDE**
- **ELECTRICALLY EQUIVALENT TO 1N5283 THRU 1N5314**
- **CONSTANT CURRENT OVER WIDE VOLTAGE RANGE**
- **COMPATIBLE WITH ALL WIRE BONDING AND DIE ATTACH TECHNIQUES, WITH THE EXCEPTION OF SOLDER REFLOW**

CD5283 thru CD5314

MAXIMUM RATINGS

Operating Temperature: -55°C to +175°C
Storage Temperature: -55°C to +175°C
Peak Operating Voltage: 100 VOLTS

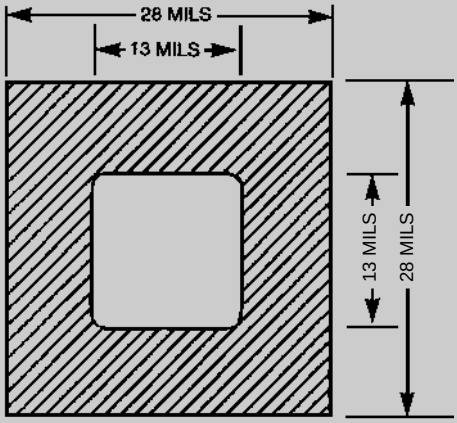
ELECTRICAL CHARACTERISTICS @ 25°C, unless otherwise speci½ed

TYPE NUMBER	REGULATOR CURRENT Ip (mA) @ V_T = 25V (Note 3)			MINIMUM DYNAMIC IMPEDANCE @V_T = 25V Z_T (M)	MINIMUM KNEE IMPEDANCE @V_K = 6.0 V Z_K (M)	MAXIMUM LIMITING VOLTAGE @ I_L = 0.8 Ip (min)
	NOM	MIN	MAX	(Note 1)	(Note 2)	V_L (VOLTS)
CD5283	0.22	0.198	0.242	25.0	2.75	1.00
CD5284	0.24	0.216	0.264	19.0	2.35	1.00
CD5285	0.27	0.243	0.297	14.0	1.95	1.00
CD5286	0.30	0.270	0.330	9.0	1.60	1.00
CD5287	0.33	0.297	0.363	6.6	1.35	1.00
CD5288	0.39	0.351	0.429	4.10	1.00	1.05
CD5289	0.43	0.387	0.473	3.30	0.870	1.05
CD5290	0.47	0.423	0.517	2.70	0.750	1.05
CD5291	0.56	0.504	0.616	1.90	0.560	1.10
CD5292	0.62	0.558	0.682	1.55	0.470	1.13
CD5293	0.68	0.612	0.748	1.35	0.400	1.15
CD5294	0.75	0.675	0.825	1.15	0.335	1.20
CD5295	0.82	0.738	0.902	1.00	0.290	1.25
CD5296	0.91	0.819	1.001	0.880	0.240	1.29
CD5297	1.00	0.900	1.100	0.800	0.205	1.35
CD5298	1.10	0.990	1.210	0.700	0.180	1.40
CD5299	1.20	1.08	1.32	0.640	0.155	1.45
CD5300	1.30	1.17	1.43	0.580	0.135	1.50
CD5301	1.40	1.26	1.54	0.540	0.115	1.55
CD5302	1.50	1.35	1.65	0.510	0.105	1.60
CD5303	1.60	1.44	1.76	0.475	0.092	1.65
CD5304	1.80	1.62	1.98	0.420	0.074	1.75
CD5305	2.00	1.80	2.20	0.395	0.061	1.85
CD5306	2.20	1.98	2.42	0.370	0.052	1.95
CD5307	2.40	2.16	2.64	0.345	0.044	2.00
CD5308	2.70	2.43	2.97	0.320	0.035	2.15
CD5309	3.00	2.70	3.30	0.300	0.029	2.25
CD5310	3.30	2.97	3.63	0.280	0.024	2.35
CD5311	3.60	3.24	3.96	0.265	0.020	2.50
CD5312	3.90	3.51	4.29	0.255	0.017	2.60
CD5313	4.30	3.87	4.73	0.245	0.014	2.75
CD5314	4.70	4.23	5.17	0.235	0.012	2.90

NOTE 1 Z_T is derived by superimposing A 90Hz RMS signal equal to 10% of V_T on V_T.

NOTE 2 Z_K is derived by superimposing A 90Hz RMS signal equal to 10% of V_K on V_K.

NOTE 3 I_P is read using a pulse measurement, 10 milliseconds maximum.



BACKSIDE IS CATHODE

A = Anode

DESIGN DATA

METALLIZATION:
Top: (Anode).....Al
Back: (Cathode).....Au

AL THICKNESS.....25,000 Å Min

GOLD THICKNESS...4,000 Å Min

CHIP THICKNESS.....10 Mils

TOLERANCES: ALL Dimensions ± 2 mils, Except Anode Pad Where Tolerance is ± 0.1 mils.

Microsemi

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