T-46-13-29

CY7C268
CY7C269

CYPRESS SEMICONDUCTOR

8192 x 8 Registered Diagnostic PROM

Features

- CMOS for optimum speed/power
- High speed
  - 15-ns max set-up
  - 12-ns clock to output
- Low power
  - 660 mW (commercial)
  - 770 mW (military)
- On-chip edge-triggered registers
  - Ideal for pipelined microprogrammed systems
- On-chip diagnostic shift register
  - For serial observability and controlability of the output register
- EPROM technology
  - 100% programmable
  - Reprogrammable (7C269W)
- 5V ±10% V_{CC}, commercial and military
- Capable of withstanding >2001V static discharge
- Slim 300-mil, 28-pin plastic or hermetic DIP (7C269)

Functional Description

The CY7C268 and the CY7C269 are 8192 x 8 registered diagnostic PROMs. They are both organized as 8,192 words by 8 bits wide, and they have both a pipeline output register and an onboard diagnostic shift register. Both devices feature a programmable initialize byte that may be loaded into the pipeline register with the initialize signal. The programmable initialize byte is the 8,193rd byte in the PROM, and may be programmed to any desired value.

The CY7C268 has 32 pins and features full diagnostic capabilities while the CY7C269 provides limited diagnostics and is available in a space-efficient 28-pin package. This allows the designers to optimize designs for either board-area efficiency with the CY7C269, or combine the CY7C268 with other diagnostic products using the standard interface.

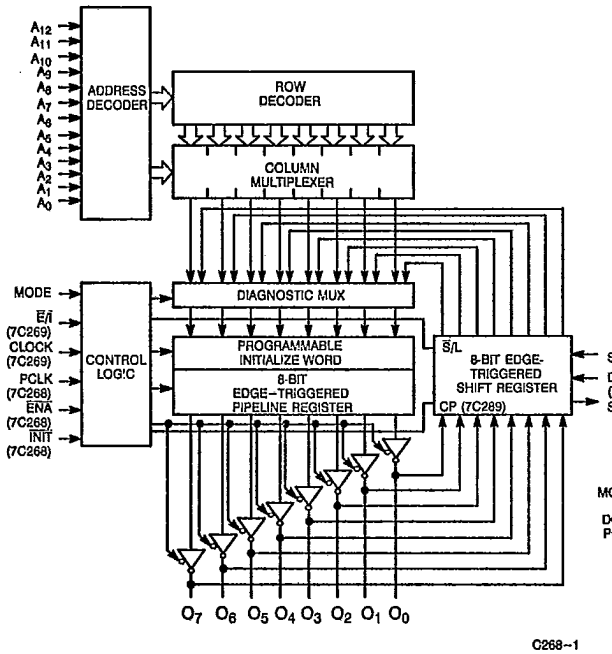
CY7C268

The CY7C268 provides 13 address signals (A_0 through A_{12}), 8 data out signals (O_0 through O_7), $\overline{ENA}$ (enable), PCLK (pipeline clock) and $\overline{INIT}$ (initialize) for control.

The full standard feature diagnostics of the CY7C268 utilize the SDI and SDO (shift in and shift out), MODE, and DCLK signals. These signals allow serial data to be shifted into and out of the diagnostic shift register at the same time the pipeline register is used for normal operation. The MODE signal is used to control the transfer of the information in the diagnostic register to the pipeline register, or the data on the output bus into the diagnostic register. The data on the output bus may be provided from the pipeline register or from an external source.

When the MODE signal is LOW, the PROM operates in a normal pipeline mode. The contents of the addressed memory location are loaded into the pipeline register on the rising edge of PCLK. the outputs are enabled with the $\overline{ENA}$ signal either synchronously or asynchronously, depending on how the device is configured when programmed. If programmed for asynchronous enable, $\overline{ENA}$ LOW enables the outputs. If configured for synchronous enable, $\overline{ENA}$ LOW will enable the outputs synchronously with PCLK during the rising edge of PCLK. $\overline{ENA}$

Logic Block Diagram



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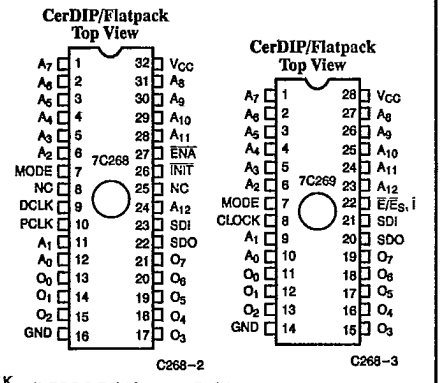
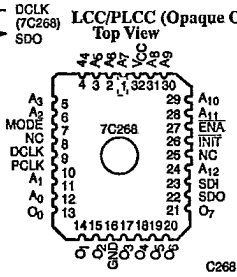
Pin Configurations

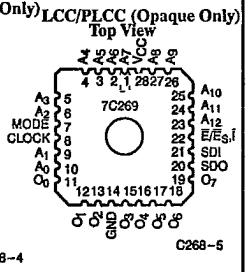


C268-2

C268-3



C268-4



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Functional Description (continued)

HIGH will synchronously disable the outputs during the rising edge of PCLK. The asynchronous initialize signal, $\overline{INIT}$, transfers the initialize byte into the pipeline register on a HIGH to LOW transition. $\overline{INIT}$ LOW disables PCLK and must transition back to a HIGH in order to enable PCLK. DCLK shifts data into SDI and out of SDO on each rising edge.

When MODE is HIGH, the rising edge of the PCLK signal loads the pipeline register with the contents of the diagnostic register. Similarly, DCLK, in this mode, loads the diagnostic register with the information on the data output pins. The information loaded will be either the contents of the pipeline register if the outputs are enabled, or data on the bus if the outputs are disabled (in a high-impedance state).

CY7C269

The CY7C269 is optimized for applications that require diagnostics in a minimum amount of board area. Packaged in 28 pins, it has 13 address signals (A_0 through A_{12}), 8 data out signals (O_0 through O_7), $\overline{E}/I$ (Enable or Initialize), and CLOCK (pipeline and diagnostic clock). Additional diagnostic signals consist of MODE, SDI (shift in) and SDO (shift out). Normal pipelined operation and diagnostic operation are mutually exclusive.

When the MODE signal is LOW, the 7C269 operates in a normal pipelined mode. CLOCK functions as a pipeline clock, loading the contents of the addressed memory location into the pipeline register on each rising edge. The data will appear on the outputs if they are enabled. One pin on the 7C269 is programmed to perform either the Enable or the Initialize function. If the $\overline{E}/I$ pin is used for a $\overline{INIT}$ (asynchronous initialize) function, the outputs are permanently enabled and the initialize word is loaded into the pipeline register on a HIGH to LOW transition of the $\overline{INIT}$ signal. The $\overline{INIT}$ LOW disables CLOCK and must return high to re-enable CLOCK. If the $\overline{E}/I$ pin is used for an enable signal, it may be programmed for either synchronous or asynchronous operation. This enable function then operates exactly the same as the 7C268.

When the MODE signal is HIGH, the 7C269 operates in the diagnostic mode. The $\overline{E}/I$ signal becomes a secondary mode signal designating whether to shift the diagnostic shift register or to load either the diagnostic register or the pipeline register. If $\overline{E}/I$ is HIGH, CLOCK performs the function of DCLK, shifting SDI into the least-significant location of the diagnostic register and all bits one location toward the most-significant location on each rising edge. The contents of the most-significant location in the diagnostic register are available on the SDO pin.

If the $\overline{E}/I$ signal is LOW, SDI becomes a direction signal, transferring the contents of the diagnostic register into the pipeline register when SDI is LOW. When SDI is HIGH, the contents of the output pins are transferred into the diagnostic register. Both transfers occur on a LOW to HIGH transition of the CLOCK. If the outputs are enabled, the contents of the pipeline register are transferred into the diagnostic register. If the outputs are disabled, an external source of data may be loaded into the diagnostic register. In this condition, the SDO signal is internally driven to be the same as the SDI signal, thus propagating the "direction of transfer information" to the next device in the string.

Selection Guide

		7C269–15	7C269–18	7C269–25
Maximum Set-Up Time (ns)		15	18	25
Maximum Clock to Output (ns)		12	15	20
Maximum Operating Current (mA)	Commercial	120	120	120
	Military		140	140

		7C268–40 7C269–40	7C268–50 7C269–50	7C268–60 7C269–60
Maximum Set-Up Time (ns)		40	50	60
Maximum Clock to Output (ns)		20	25	25
Maximum Operating Current (mA)	Commercial	100	80	80
	Military		120	100

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

DC Program Voltage 13.0V

UV Exposure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	– 40°C to +85°C	5V ± 10%
Military[2]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameters	Description	Test Conditions		7C269–15 Min.	7C269–15 Max.	7C269–18 Min.	7C269–18 Max.	7C269–25 Min.	7C269–25 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	Com'l		0.4		0.4		0.4	V
		V_{CC} = Min., I_{OL} = 6.0 mA	Mil		0.4		0.4		0.4	
V_{IH}	Input HIGH Voltage			2.0		2.0		2.0		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−40	+40	−40	+40	−40	+40	µA
I_{OS}[5]	Output Short Circuit Current				90		90		90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		120		120		120	mA
			Mil				140		140	
V_{PP}	Programming Supply Voltage			12	13	12	13	12	13	V
I_{PP}	Programming Supply Current				50		50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4		0.4	V

Parameters	Description	Test Conditions		7C268–40 7C269–40 Min.	7C268–40 7C269–40 Max.	7C268–50 7C269–50 Min.	7C268–50 7C269–50 Max.	7C268–60 7C269–60 Min.	7C268–60 7C269–60 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA	Com'l		0.4		0.4		0.4	V
		V_{CC} = Min., I_{OL} = 8.0 mA	Mil		0.4		0.4		0.4	
V_{IH}	Input HIGH Voltage			2.0		2.0		2.0		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−40	+40	−40	+40	−40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND			90		90		90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		100		80		80	mA
			Mil				120		100	
V_{PP}	Programming Supply Voltage			12	13	12	13	12	13	V
I_{PP}	Programming Supply Current				50		50		50.	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4		0.4	V

Notes:
1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See Introduction to CMOS PROMs in this Data Book for general information on testing.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

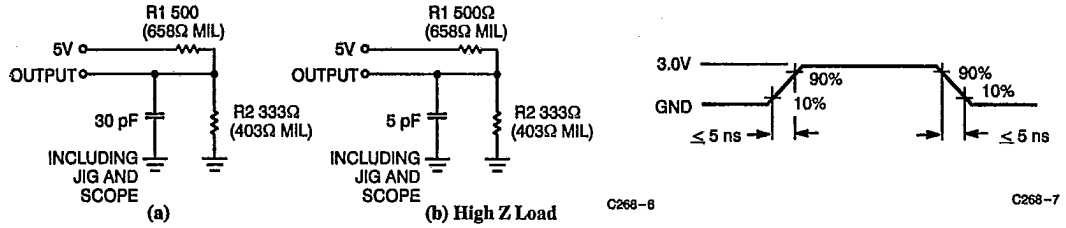
Capacitance[4, 6]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = 5.0V$	10	pF
C_{OUT}	Output Capacitance		10	pF

Note:
6. Tested initially and after any design or process changes that may affect these parameters.

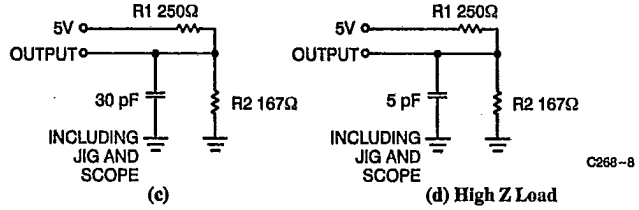
AC Test Loads and Waveforms

Test Load for −15 through −25 speeds

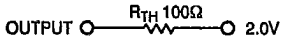


Equivalent to: THÉVENIN EQUIVALENT

Test Load for −40 through −60 speeds



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3,4]

Parameters	Description	7C269−15		7C269−18		7C269−25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AS}	Address Set-Up to Clock	15		18		25		ns
t_{HA}	Address Hold from Clock	0		0		0		ns
t_{CO}	Clock to Output Valid		12		15		20	ns
t_{PW}	Clock Pulse Width	12		15		15		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock (Sync Enable Only)	12		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock	5		5		5		ns
t_{DI}	$\overline{INIT}$ to Out Valid		15		18		25	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock	12		15		20		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	12		18		25		ns
t_{COS}	Output Valid from Clock (Sync. Mode)		12		15		20	ns
t_{HZS}	Output Inactive from Clock (Sync. Mode)		12		15		20	ns
t_{DOE}	Output Valid from $\overline{E}$ LOW (Asynch. Mode)		12		15		20	ns
t_{HZE}	Output Inactive from $\overline{E}$ HIGH (Async. Mode)		12		15		20	ns

Switching Characteristics Over the Operating Range[3,4] (continued)

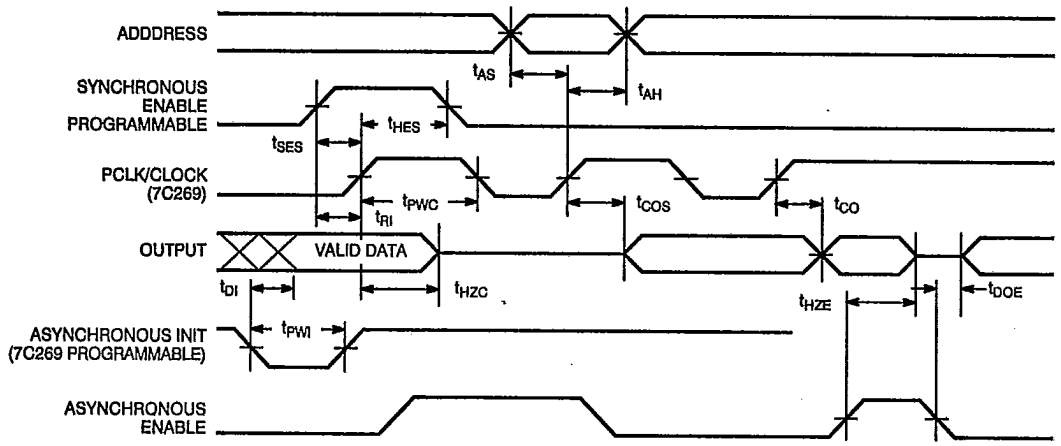
Parameters	Description	7C268–40 7C269–40		7C268–50 7C269–50		7C268–60 7C269–60		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AS}	Address Set-Up to Clock	40		50		60		ns
t_{HA}	Address Hold from Clock	0		0		0		ns
t_{CO}	Clock to Output Valid		20		25		25	ns
t_{PW}	Clock Pulse Width	15		20		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock (Sync Enable Only)	15		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock	5		5		5		ns
t_{DI}	$\overline{INIT}$ to Output Valid		25		35		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock	20		25		25		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	25		35		35		ns
t_{COS}	Output Valid from Clock (Sync. Mode)		20		25		25	ns
t_{HZS}	Output Inactive from Clock (Sync. Mode)		20		25		25	ns
t_{DOE}	Output Valid from $\overline{E}$ LOW (Asynch. Mode)		20		25		25	ns
t_{HZE}	Output Inactive from $\overline{E}$ HIGH (Async. Mode)		20		25		25	ns

Diagnostic Mode Switching Characteristics Over the Operating Range[3,4]

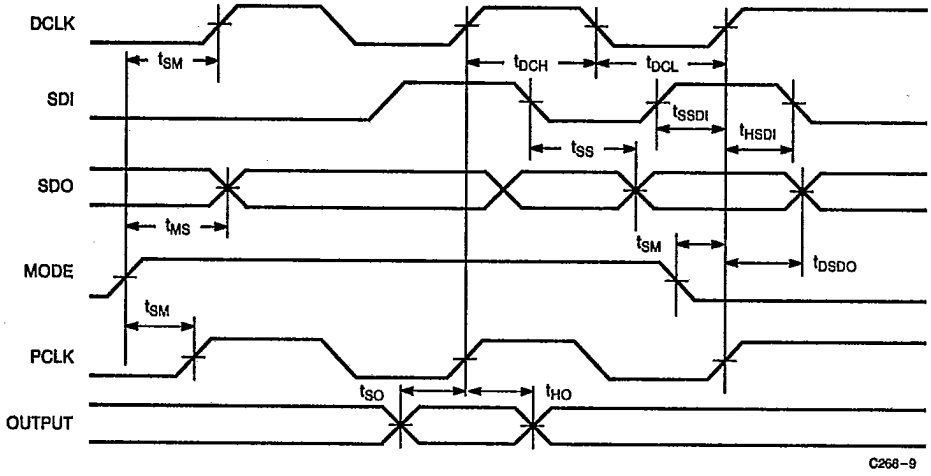
Parameters	Description		7C269–15		7C269–18		7C269–25		7C268–40,50,60 7C269–40,50,60		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SSDI}	Set-Up SDI to Clock	Com'l	20		25		25		30		ns
		Mil			25		30		35		
t_{HSDI}	SDI Hold from Clock	Com'l	0		0		0		0		ns
		Mil			0		0		0		
t_{DSDO}	SDO Delay from Clock	Com'l		20		25		25		30	ns
		Mil				25		30		40	
t_{DCL}	Minimum Clock LOW	Com'l	20		25		25		25		ns
		Mil			25		25		25		
t_{DCH}	Minimum Clock HIGH	Com'l	20		25		25		25		ns
		Mil			25		25		25		
t_{SM}	Set-Up to Mode Change	Com'l	20		25		25		25		ns
		Mil			25		30		30		
t_{HM}	Hold from Mode Change (7C269)	Com'l	0		0		0		0		ns
		Mil			0		0		0		
t_{MS}	Mode to SDO	Com'l		20		25		25		25	ns
		Mil				25		30		30	
t_{SS}	SDI to SDO	Com'l		30		35		40		40	ns
		Mil				35		40		45	
t_{SO}	Data Set-Up to DCLK	Com'l	20		25		25		25		ns
		Mil			25		30		30		
t_{HO}	Data Hold from DCLK	Com'l	10		10		10		10		ns
		Mil			13		13		15		

Switching Waveforms[3,4]

Pipeline Operation (Mode = 0)

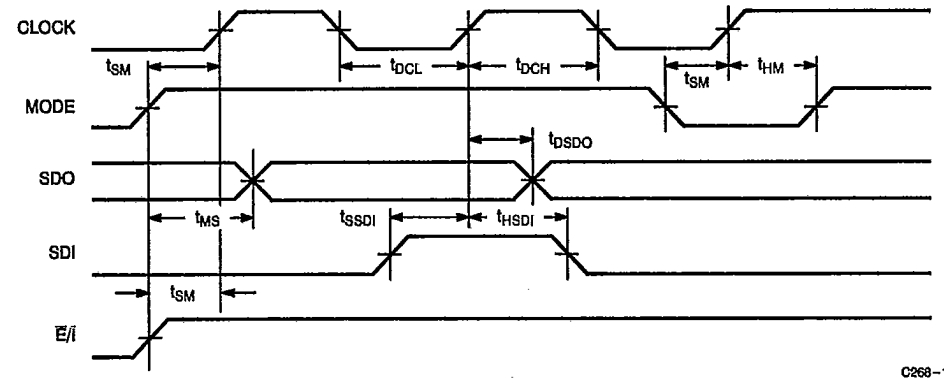


Diagnostic Waveform for the 7C268

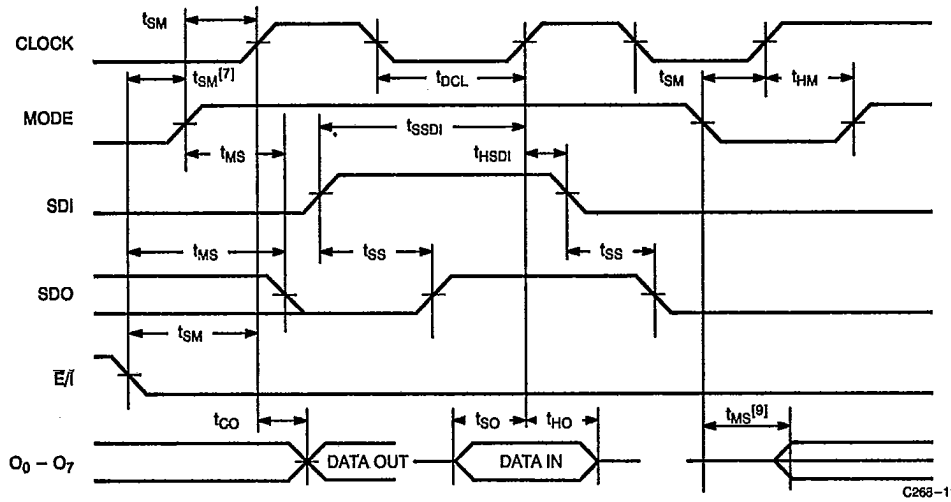


Switching Waveforms[3,4] (continued)

Diagnostic Application for the 7C269 (Shifting the Shadow Register[8])



Diagnostic Application for the 7C269 (Parallel Data Transfer)



Notes:

7. Asynchronous enable mode only.
8. Diagnostic register = shadow register = shift register.
9. The mode transition to HIGH latches the asynchronous enable state. If the enable state is changed and held before leaving the diagnostic mode (mode H ↓ L) then the output impedance change delay is t_{MS}.

PROMs

Bit Map Data

Programmer Address (Hex.)		RAM Data
Decimal	Hex	Contents
0	0	Data
.	.	.
.	.	.
8191	1FFF	Data
8192	2000	Init Byte
8193	2001	Control Byte

Control Byte

00 Asynchronous output enable (default condition)
01 Synchronous output enable
02 Asynchronous initialize (CY7C269 only)

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. CY7C268 Mode Selection

Mode		Pin Function[10]							
	Read or Output Disable	A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
	Other	A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Load SR to PR		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Load Output to SR		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Shift SR		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Asynchronous Enable Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Synchronous Enable Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Asynchronous Initialization Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Program Memory		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Program Verify		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Program Inhibit		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Program Synchronous Enable		V_{IHP}	V_{IHP}	$A_{10} - A_7$	V_{IHP}	V_{PP}	$A_4 - A_3$	V_{IHP}	V_{PP}
Program Initial Byte		X	V_{ILP}	$A_{10} - A_7$	V_{IHP}	V_{PP}	$A_4 - A_3$	V_{ILP}	V_{PP}

Mode		Pin Function[10]							
	Read or Output Disable	A_0	MODE	DCLK	PCLK	SDI	SDO	$\overline{E}$, $\overline{E}_S$, I	$O_7 - O_0$
	Other	A_0	$\overline{PGM}$	DCLK	PCLK	NA	$\overline{VFY}$	V_{PP}	$D_7 - D_0$
Read		A_0	V_{IL}	X	V_{IL}/V_{IH}	X	SDO	V_{IL}	$O_7 - O_0$
Load SR to PR		A_0	V_{IH}	V_{IL}	V_{IL}/V_{IH}	X	SDI	X	$O_7 - O_0$
Load Output to SR		A_0	V_{IH}	V_{IH}/V_{IH}	V_{IL}	V_{IL}	SDI	V_{IH}	$O_7 - O_0$
Shift SR		A_0	V_{IH}	V_{IL}/V_{IH}	V_{IL}	D_{IN}	SDO	X	$O_7 - O_0$
Asynchronous Enable Read		A_0	V_{IL}	V_{IL}	X	V_{IL}	SDO	V_{IL}	$O_7 - O_0$
Synchronous Enable Read		A_0	V_{IL}	V_{IL}	V_{IL}/V_{IH}	V_{IL}	SDO	V_{IL}	$O_7 - O_0$
Asynchronous Initialization Read		A_0	V_{IL}	V_{IL}	X	V_{IL}	SDO	V_{IL}	$O_7 - O_0$
Program Memory		A_0	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Verify		A_0	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		A_0	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	High Z
Program Synchronous Enable		V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Initial Byte		V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$

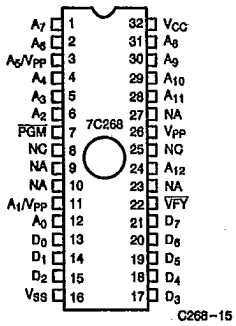
Table 2. CY7C269 Mode Selection

Mode		Pin Function[10]							
	Read or Output Disable	A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
	Other	A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Load SR to PR		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Load Output to SR		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Shift SR		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Asynchronous Enable Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Synchronous Enable Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Asynchronous Initialization Read		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Program Memory		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Program Verify		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Program Inhibit		A_{12}	A_{11}	$A_{10} - A_7$	A_6	A_5	$A_4 - A_3$	A_2	A_1
Program Synchronous Enable		V_{IHP}	V_{IHP}	$A_{10} - A_7$	V_{IHP}	V_{PP}	$A_4 - A_3$	V_{IHP}	V_{PP}
Program Initialize		V_{ILP}	V_{IHP}	$A_{10} - A_7$	V_{IHP}	V_{PP}	$A_4 - A_3$	V_{ILP}	V_{PP}
Program Initial Byte		A_{12}	V_{ILP}	$A_{10} - A_7$	V_{IHP}	V_{PP}	$A_4 - A_3$	V_{ILP}	V_{PP}

Mode		Pin Function[10]						
	Read or Output Disable	A_0	MODE	CLK	SDI	SDO	$\overline{E}, \overline{I}$	$O_7 - O_0$
	Other	A_0	$\overline{PGM}$	CLK	NA	$\overline{VFY}$	V_{PP}	$D_7 - D_0$
Read		A_0	V_{IL}	V_{IL}/V_{IH}	X	High Z	V_{IL}	$O_7 - O_0$
Load SR to PR		A_0	V_{IH}	V_{IL}/V_{IH}	V_{IL}	SDI	V_{IL}	$O_7 - O_0$
Load Output to SR		A_0	V_{IH}	V_{IL}/V_{IH}	V_{IH}	SDI	V_{IL}	$O_7 - O_0$
Shift SR		A_0	V_{IH}	V_{IL}/V_{IH}	D_{IN}	SDO	V_{IH}	$O_7 - O_0$
Asynchronous Enable Read		A_0	V_{IL}	V_{IL}	X	High Z	V_{IL}	$O_7 - O_0$
Synchronous Enable Read		A_0	V_{IL}	V_{IL}/V_{IH}	X	High Z	V_{IL}	$O_7 - O_0$
Asynchronous Initialization Read		A_0	V_{IL}	V_{IL}	X	High Z	V_{IL}	$O_7 - O_0$
Program Memory		A_0	V_{ILP}	V_{ILP}	X	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Verify		A_0	V_{IHP}	V_{ILP}	X	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		A_0	V_{IHP}	V_{ILP}	X	V_{IHP}	V_{PP}	High Z
Program Synchronous Enable		V_{ILP}	V_{ILP}	V_{ILP}	X	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Initialize		V_{ILP}	V_{ILP}	V_{ILP}	X	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Initial Byte		V_{IHP}	V_{ILP}	V_{ILP}	X	V_{IHP}	V_{PP}	$D_7 - D_0$

Note:
10. X = "don't care" but not to exceed $V_{CC} \pm 5\%$.

CerDIP/Flatpack



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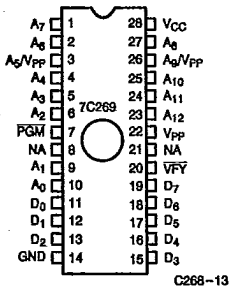
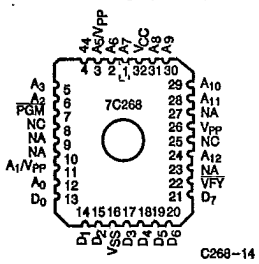
CerDIP/Flatpack



C268-13

LCC/PLCC (Opaque Only)



C268-14

LCC/PLCC (Opaque Only)

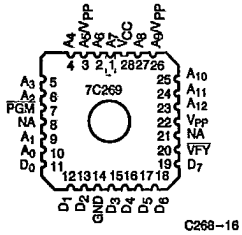


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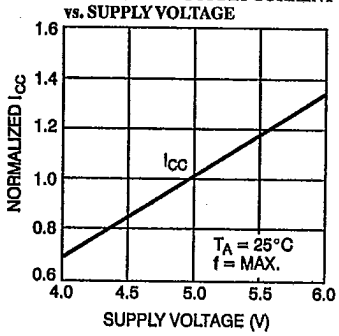
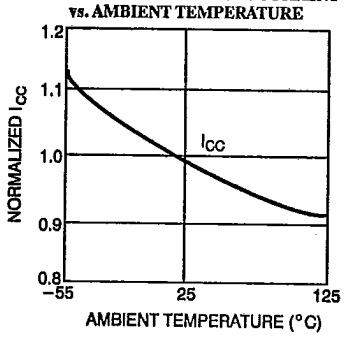
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

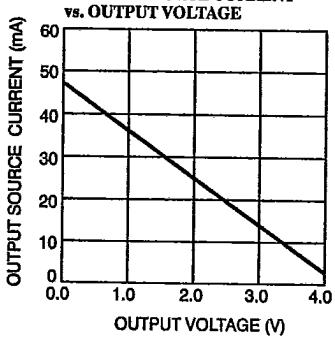
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



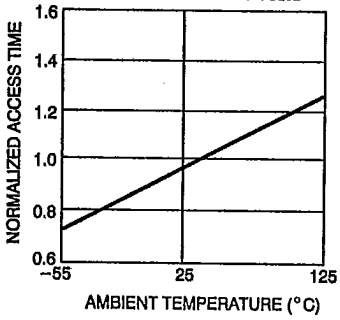
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



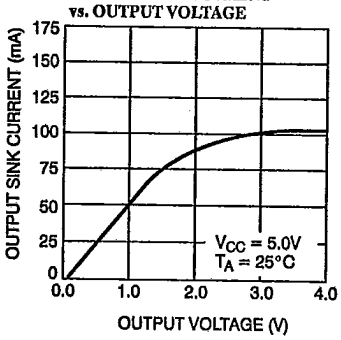
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



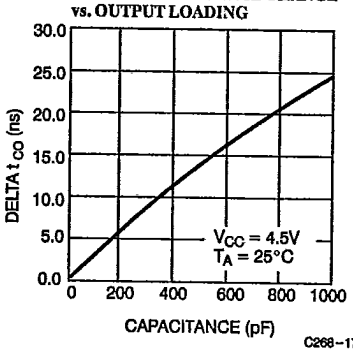
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



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PROMs 3

Ordering Information[11]

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
40	100	CY7C268–40DC	D20	Commercial
		CY7C268–40WC	W20	
50	80	CY7C268–50DC	D20	Commercial
		CY7C268–50WC	W20	
	120	CY7C268–50DMB	D20	Military
		CY7C268–50LMB	L55	
		CY7C268–50QMB	Q55	
		CY7C268–50WMB	W20	
60	80	CY7C268–60DC	D20	Commercial
		CY7C268–60WC	W20	
	100	CY7C268–60DMB	D20	Military
		CY7C268–60LMB	L55	
		CY7C268–60QMB	Q55	
		CY7C268–60WMB	W20	

Notes:

11. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
15	120	CY7C269–15DC	D22	Commercial
		CY7C269–15PC	P21	
		CY7C269–15WC	W22	
18	120	CY7C269–18DC	D22	Commercial
		CY7C269–18PC	P21	
		CY7C269–18WC	W22	
	140	CY7C269–18DMB	D22	Military
		CY7C269–18LMB	L64	
		CY7C269–18QMB	Q64	
		CY7C269–18WMB	W22	
25	140	CY7C269–25DC	D22	Commercial
		CY7C269–25LC	L64	
		CY7C269–25PC	P21	
		CY7C269–25QC	Q64	
		CY7C269–25WC	W22	
		CY7C269–25DMB	D22	Military
		CY7C269–25LMB	L64	
		CY7C269–25QMB	Q64	
		CY7C269–25WMB	W22	
40	100	CY7C269–40DC	D22	Commercial
		CY7C269–40PC	P21	
		CY7C269–40WC	W22	
50	80	CY7C269–50DC	D22	Commercial
		CY7C269–50PC	P21	
		CY7C269–50WC	W22	
	120	CY7C269–50DMB	D22	Military
		CY7C269–50LMB	L64	
		CY7C269–50QMB	Q64	
		CY7C269–50WMB	W22	
60	80	CY7C269–60DC	D22	Commercial
		CY7C269–60PC	P21	
		CY7C269–60WC	W22	
	100	CY7C269–60DMB	D22	Military
		CY7C269–60LMB	L64	
		CY7C269–60QMB	Q64	
		C7C269Y–60WMB	W22	

T-46-13-29

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{AS}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{PW}	7, 8, 9, 10, 11
t_{SES}	7, 8, 9, 10, 11
t_{HES}	7, 8, 9, 10, 11
t_{COS}	7, 8, 9, 10, 11

Diagnostic Mode Switching Characteristics

Parameters	Subgroups
t_{SSDI}	7, 8, 9, 10, 11
t_{HSDI}	7, 8, 9, 10, 11
t_{DSDO}	7, 8, 9, 10, 11
t_{DCL}	7, 8, 9, 10, 11
t_{DCH}	7, 8, 9, 10, 11
t_{HM}[12]	7, 8, 9, 10, 11
t_{MS}	7, 8, 9, 10, 11
t_{SS}	7, 8, 9, 10, 11

Notes:
12. 7C269 only.

Document #: 38–00069–C