HIGH SPEED 2K x 8 CMOS PROM/RPROM

KEY FEATURES

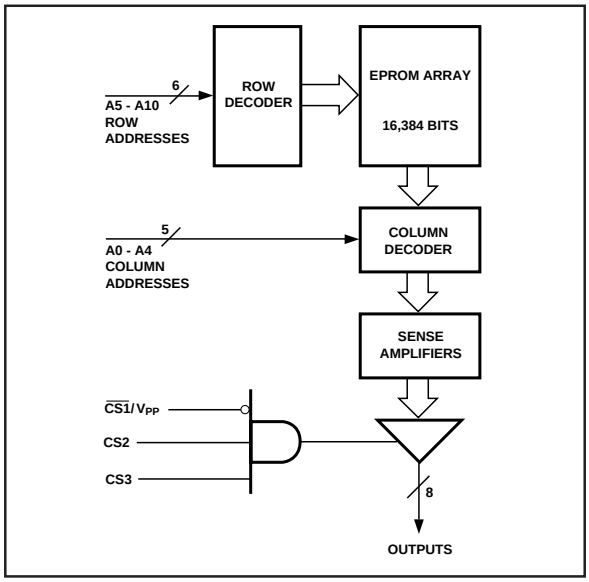
- **Ultra-Fast Access Time**
  - — t_{ACC} = 25 ns
  - — t_{CS} = 12 ns
- **Low Power Consumption**
- **Fast Programming**
- **Available in 300 Mil DIP and PLDCC**
- **Pin Compatible with Am27S191/291 and N82S191 Bipolar PROMs**
- **Immune to Latch-UP**
  - — Up to 200 mA
- **ESD Protection Exceeds 2000V**

GENERAL DESCRIPTION

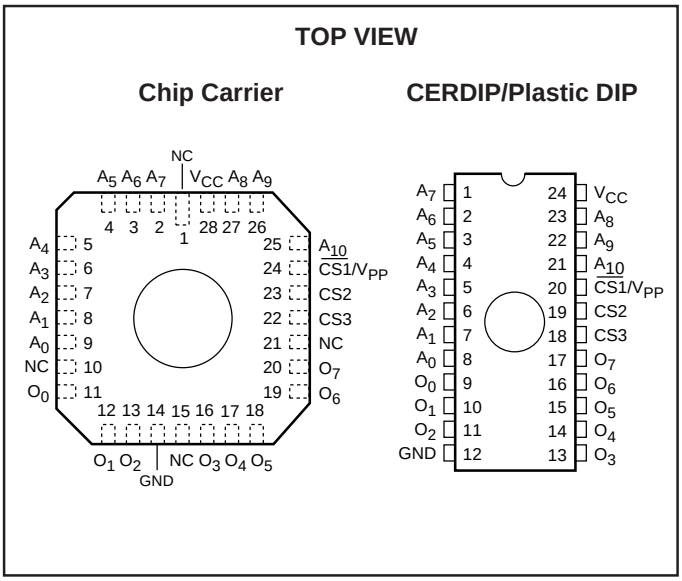
The WS57C191C/291C is an extremely High Performance 16K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology which enables it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts. The WS57C191C/291C is also configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

The WS57C191C is packaged in a conventional 600 mil DIP package as well as a Plastic Leaded Chip Carrier (PLDCC) and a Ceramic Leadless Chip Carrier (CLLCC). The WS57C291C is packaged in a space saving 300 mil DIP package configuration. Both are available in commercial, industrial, and military operating temperature ranges.

BLOCK DIAGRAM



PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	191C/291C-25	191C/291C-35	191C/291C-45	191C/291C-55
Address Access Time (Max)	25 ns	35 ns	45 ns	55 ns
CS to Output Valid Time (Max)	12 ns	20 ns	20 ns	20 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature.....–65° to + 150°C

Voltage on any Pin with
Respect to Ground .....–0.6V to +7V

V_{PP} with Respect to Ground.....–0.6V to + 14V

ESD Protection.....>2000V

***NOTICE:**
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

MODE SELECTION

PINS / MODE	$\overline{CS1}$/ V_{PP}	CS2	CS3	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IH}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	X	V_{CC}	High Z
Output Disable	X	V_{IL}	X	V_{CC}	High Z
Program	V_{PP}	X	X	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	X	X	V_{IL}	V_{CC}	High Z

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 10%
Industrial	–40°C to +85°C	+5V ± 10%
Military	–55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 3)		–0.1	0.8	V
V_{IH}	Input High Voltage	(Note 3)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	V_{CC} = 5.5V, f = 0 MHz (Note 1), Output Not Loaded Add 2mA/MHz for AC Operation	Comm'l		30	mA
			Industrial		35	mA
			Military		35	mA
I_{CC2}	V_{CC} Active Current (TTL)	V_{CC} = 5.5V, f = 0 MHz (Note 2), Output Not Loaded Add 2mA/MHz for AC Operation	Comm'l		40	mA
			Industrial		50	mA
			Military		50	mA
I_{LI}	Input Leakage Current	V_{IN} = 5.5V or Gnd		–10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		–10	10	µA

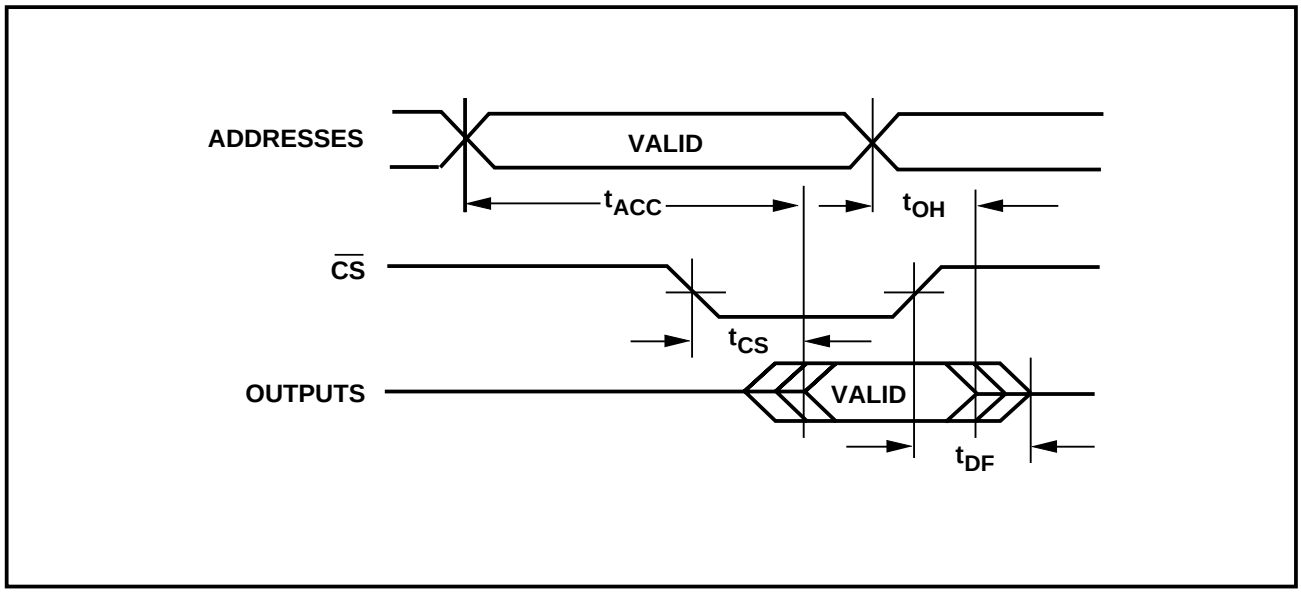
NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \le 0.8V$, $V_{IH} \ge 2.0V$.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	191C/291C-25		191C/291C-35		191C/291C-45		191C/291C-55		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		25		35		45		55	ns
$\overline{CS}$ to Output Delay	t_{CS}		12		20		20		20	
Output Disable to Output Float*	t_{DF}		12		20		20		20	
Address to Output Hold	t_{OH}	0		0		0		0		

*Sampled, Not 100% Tested

AC READ TIMING DIAGRAM

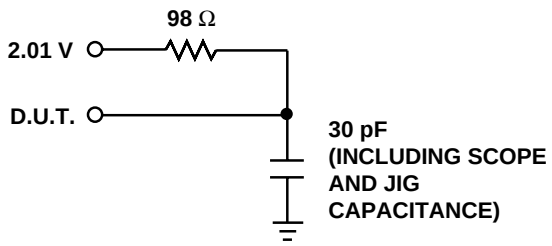


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

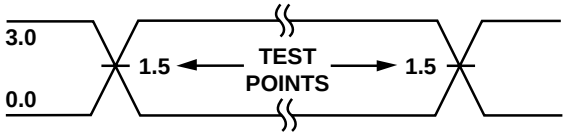
SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0 V	18	25	pF

NOTES: 4. This parameter is only sampled and is not 100% tested.
5.Typical values are for TA = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



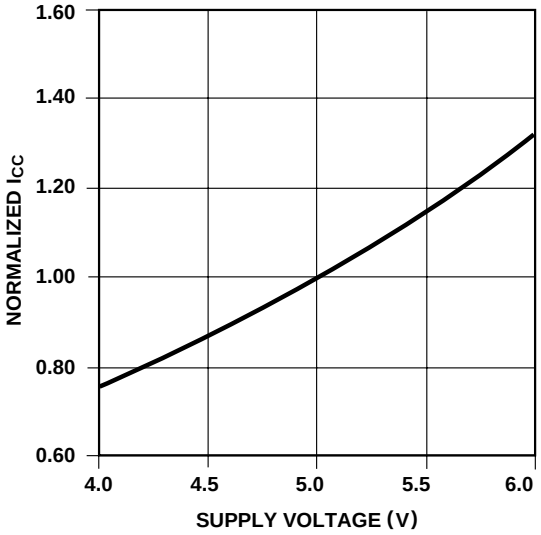
A.C. TESTING INPUT/OUTPUT WAVEFORM



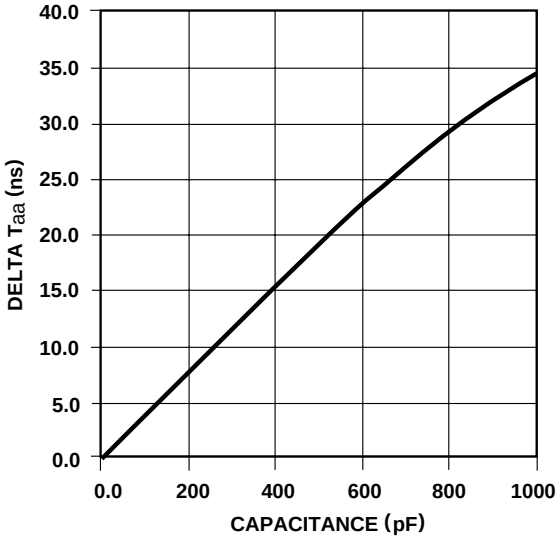
A.C. testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Timing measurements are made at 1.5 V for input and output transitions in both directions.

NOTE: 6. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 0.1 microfarad capacitor in parallel with a 0.01 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

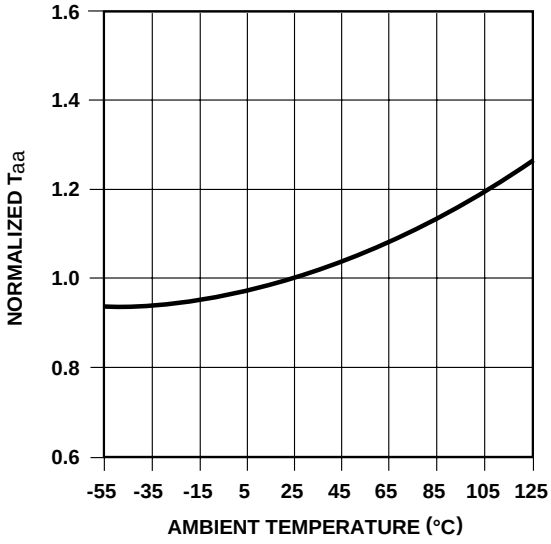
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



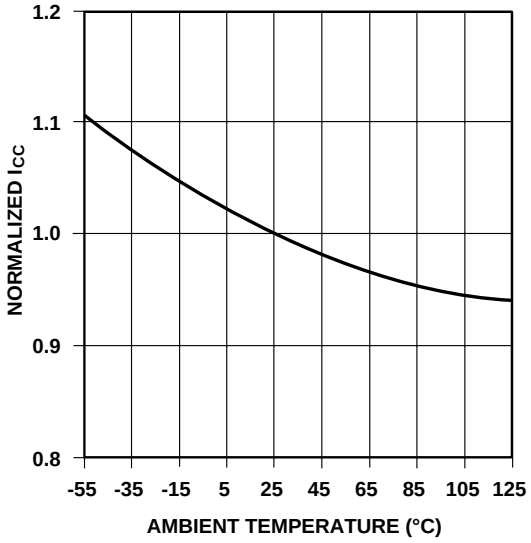
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED T_{aa} vs. AMBIENT TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 ± 0.25 V)

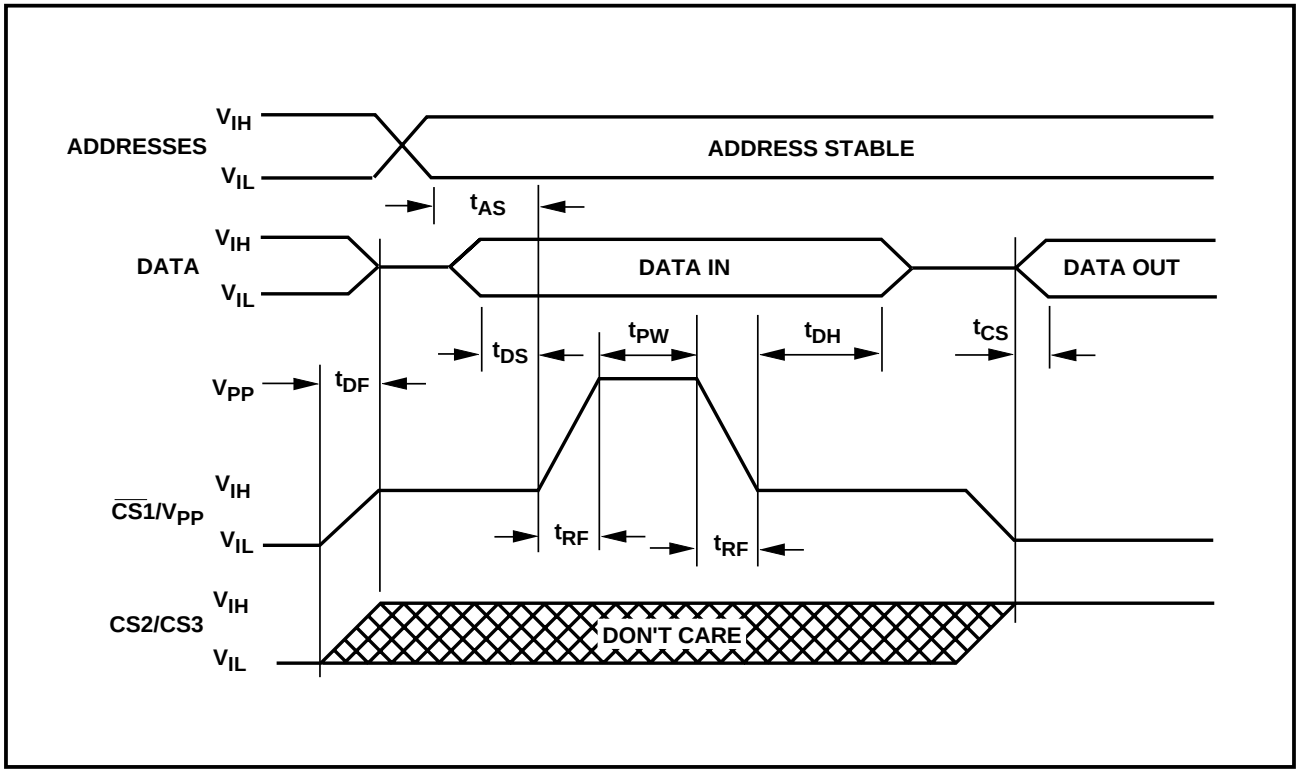
SYMBOLS	PARAMETER	MIN	MAX	UNITS
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse		60	mA
I_{CC}	V_{CC} Supply Current		25	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = –4 mA)	2.4		V

NOTES: 8. V_{PP} must not be greater than 13 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 ± 0.25 V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{DF}	Chip Disable Setup Time			30	ns
t_{DS}	Data Setup Time	2			µs
t_{PW}	Program Pulse Width	100		200	µs
t_{DH}	Data Hold Time	2			µs
t_{CS}	Chip Select Delay			30	ns
t_{RF}	V_{PP} Rise and Fall Time	1			µs

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C191C					
WS57C191C-25D	25	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C191C-25J	25	28 Pin PLDCC	J3	Comm'l	Standard
WS57C191C-25P	25	24 Pin Plastic DIP, 0.6"	P2	Comm'l	Standard
WS57C191C-35D	35	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C191C-35J	35	28 Pin PLDCC	J3	Comm'l	Standard
WS57C191C-35P	35	24 Pin Plastic DIP, 0.6"	P2	Comm'l	Standard
WS57C191C-45D	45	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C191C-45DI	45	24 Pin CERDIP, 0.6"	D1	Industrial	Standard
WS57C191C-45DMB*	45	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C191C-45J	45	28 Pin PLDCC	J3	Comm'l	Standard
WS57C191C-45P	45	24 Pin Plastic DIP, 0.6"	P2	Comm'l	Standard
WS57C191C-55D	55	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C191C-55DMB*	55	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C291C					
WS57C291C-25S	25	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C291C-25T	25	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C291C-35S	35	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C291C-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C291C-35TMB*	35	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C291C-45S	45	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C291C-45T	45	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C291C-45TI	45	24 Pin CERDIP, 0.3"	T1	Industrial	Standard
WS57C291C-45TMB*	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C291C-55T	55	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C291C-55TMB*	55	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

NOTE: 9. The actual part marking will not include the initials "WS."

*SMD product. See section 4 for DESC SMD number.

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS57C191C and WS57C291C are programmed using Algorithm D shown on page 5-9.