REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R028-94.	93-11-05	M. A. Frye
B	Updated boilerplate. Added device types 04-07. Removed programming requirements from drawing. Editorial changes throughout.	94-04-15	M. A. Frye
C	Changes in accordance with NOR 5962-R279-94.	94-09-20	M. A. Frye
D	Boilerplate update, part of 5 year review. ksr	07-10-02	Robert M. Heber

THE ORIGINAL FIRST PAGE HAS BEEN REPLACED.

REV																			
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REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D			
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A

PREPARED BY
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COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-07-11

REVISION LEVEL
D

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 512 X 8 REGISTERED PROGRAMMABLE READ ONLY MEMORY (PROM), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-88518**

SHEET 1 OF 11

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-88518	01	X	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		512 X 8-bit registered PROM	30
02		512 X 8-bit registered PROM	35
03		512 X 8-bit registered PROM	40
04		512 X 8-bit registered PROM	30
05		512 X 8-bit registered PROM	35
06		512 X 8-bit registered PROM	40
07		512 X 8-bit registered PROM	25

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	CDIP4-T24 or GDIP3-T24	24	Dual-in-line
3	CQCC1-N28	28	Square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 2/

Supply voltage range to ground potential (V_{CC})	-0.5 V dc to +7.0 V dc
DC voltage range applied to the outputs in the high Z state	-0.5 V dc to +7.0 V dc
DC input voltage	-3.0 V dc to +7.0 V dc
Maximum power dissipation	1.0 W 3/
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+150°C 4/
Storage temperature range (T_{STG})	-65°C to +150°C
Temperature under bias	-55°C to +125°C
Data retention	10 years, minimum

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Input high voltage range (V_{IH})	+2.0 V dc
Input low voltage range (V_{IL})	+0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin and will also be listed in MIL-HDBK-103.
2/ Unless otherwise specified, all voltages are referenced to ground.
3/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.
4/ Maximum junction temperature may be inceased to +175°C during burn-in and steady state life tests.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, C, or D (see 4.4), the devices shall be programmed by the manufacturer prior to test with a checkerboard pattern or equivalent (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.3 Logic diagram(s). The logic diagram shall be as specified on figure 3.

3.2.4 AC test loads and waveforms. The ac test loads and waveforms shall be as specified on figure 4.

3.2.5 Switching waveforms. The switching waveforms shall be as specified on figure 5.

3.2.6 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done initially and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but will guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Output voltage high	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4 mA V_{IH} = 2.0 V, V_{IL} = 0.8 V	1, 2, 3	ALL	2.4		V
Output voltage low	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 16 mA V_{IH} = 2.0 V, V_{IL} = 0.8 V	1, 2, 3	ALL		0.4	V
Input leakage current	I_{IX}	V_{CC} = 5.5 V V_{IN} = 5.5 V and GND.	1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V V_{OUT} = 5.5 and GND 1/ Outputs disabled	1, 2, 3	ALL	-10	10	µA
Output short circuit current	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = GND Unused outputs are open 2/ 3/	1, 2, 3	All	-20	-90	mA
Power supply current	I_{CC}	V_{CC} = 5.5 V, $0.0\ V \le V_{IN} \le V_{CC}$	1, 2, 3	ALL		120	mA
Input capacitance	C_{IN}	V_{CC} =5.0 V, f = 1 MHz See 4.3.1c	4	All		10	pF
Output capacitance	C_{OUT}	V_{CC} = 5.0 V, f = 1 MHz See 4.3.1c	4	All		10	pF
Functional tests		See 4.3.1e	7, 8A,8B	All			
Address setup to clock high	t_{SA}	See figure 4 and 5 as applicable	9, 10, 11	01,04 02,05 03,06 07	30 35 40 25		ns
Address hold from clock high	t_{HA}		9, 10, 11	ALL	0		ns
Clock high to output valid	t_{CO}		9, 10, 11	01,04 02,05 03,06 07		15 20 25 12	ns
Clock pulse width	t_{PWC}		9, 10, 11	01,04 02,03, 05,06 07	15 20 10		ns
$\overline{E}$s setup to clock high 3/	t_{SEs}		9, 10, 11	All	10		ns
$\overline{E}$s hold from clock HIGH 3/	t_{HEs}		9, 10, 11	01-06 07	5 0		ns

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output valid from clock high	t_{COS}	See figure 4 and 5 as applicable, 3/ 4/	9, 10, 11	01,04,07		20	ns
				02,05		25	
				03,06		30	
Output inactive from clock high	t_{HZC}	See figure 4 and 5 as applicable, 3/ 4/ 5/	9, 10, 11	01,04,07		20	ns
				02,05		25	
				03,06		30	
Output valid from $\overline{E}$ low	t_{DOE}	See figure 4 and 5 as applicable, 3/ 6/	9, 10, 11	01,04,07		20	ns
				02,05		25	
				03,06		30	
Output inactive from $\overline{E}$ high	t_{HZE}	See figure 4 and 5 as applicable, 3/ 4/ 5/	9, 10, 11	01,04,07		20	ns
				02,05		25	
				03,06		30	
Delay from $\overline{PRESET}$ or $\overline{CLEAR}$ to valid output	t_{DP} t_{DC}	See figure 4 and 5	9, 10, 11	All		20	ns
$\overline{PRESET}$ or $\overline{CLEAR}$ recovery to clock high	t_{RP} t_{RC}	See figure 4 and 5	9, 10, 11	01-06		20	ns
				07		15	
$\overline{PRESET}$ or $\overline{CLEAR}$ pulse width	t_{PWP} t_{PWC}	See figure 4 and 5 3/	9, 10, 11	01-06		20	ns
				07		15	

1/ For the tests using synchronous enable, the device must be clocked after applying these voltages to perform this measurement.

2/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

4/ Applies only when the synchronous (Es) function is used.

5/ Transition is measured at steady state high level -500 mV or steady state low level +500 mV on the output from the 1.5 V level on the input with loads shown on figure 4; C_L = 5 pF.

6/ Applies only when the asynchronous ($\overline{E}$) function is used.

Device types	ALL	
Case outlines	L	3
Terminal number	Terminal symbol	
1	A_7	NC
2	A_6	A_7
3	A_5	A_6
4	A_4	A_5
5	A_3	A_4
6	A_2	A_3
7	A_1	A_2
8	A_0	A_1
9	O_0	A_0
10	O_1	NC
11	O_2	O_0
12	GND	O_1
13	O_3	O_2
14	O_4	GND
15	O_5	NC
16	O_6	O_3
17	O_7	O_4
18	$\overline{PGM}$ (CP)	O_5
19	$\overline{VFY}$ ($\overline{Es}$)	O_6
20	V_{PP} ($\overline{CLR}$)	O_7
21	$\overline{E}$	NC
22	$\overline{PS}$	$\overline{PGM}$ (CP)
23	A_8	$\overline{VFY}$ ($\overline{Es}$)
24	V_{CC}	$\overline{CLR}$
25	---	$\overline{E}$
26	---	$\overline{PS}$
27	---	A_8
28	---	V_{CC}

NC = no connection

FIGURE 1. Terminal connections.

	Read or output disable	CP	$\overline{E}_S$	$\overline{CLR}$	$\overline{E}$	$\overline{PS}$	Outputs
	Other	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	$\overline{E}$	$\overline{PS}$	
Mode	Read 1/ 2/ 3/	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data out
	Output disable 1/ 4/	X	V_{IH}	V_{IH}	X	V_{IH}	High Z
	Output disable 1/	X	X	V_{IH}	V_{IH}	V_{IH}	High Z
	$\overline{CLEAR}$ 1/	X	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Zeros
	$\overline{PRESET}$ 1/	X	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Ones

1/ X = don't care, but not to exceed V_{PP} = 13.0 V, maximum.
2/ During read operation, the output latches are loaded on a "0" to "1" transition of CP.
3/ Pin Es must be LOW prior to the "0" to "1" transition on CP that loads the register.
4/ Es must be HIGH prior to the "0" to "1" transition on CP that loads the register.

FIGURE 2. Truth table.

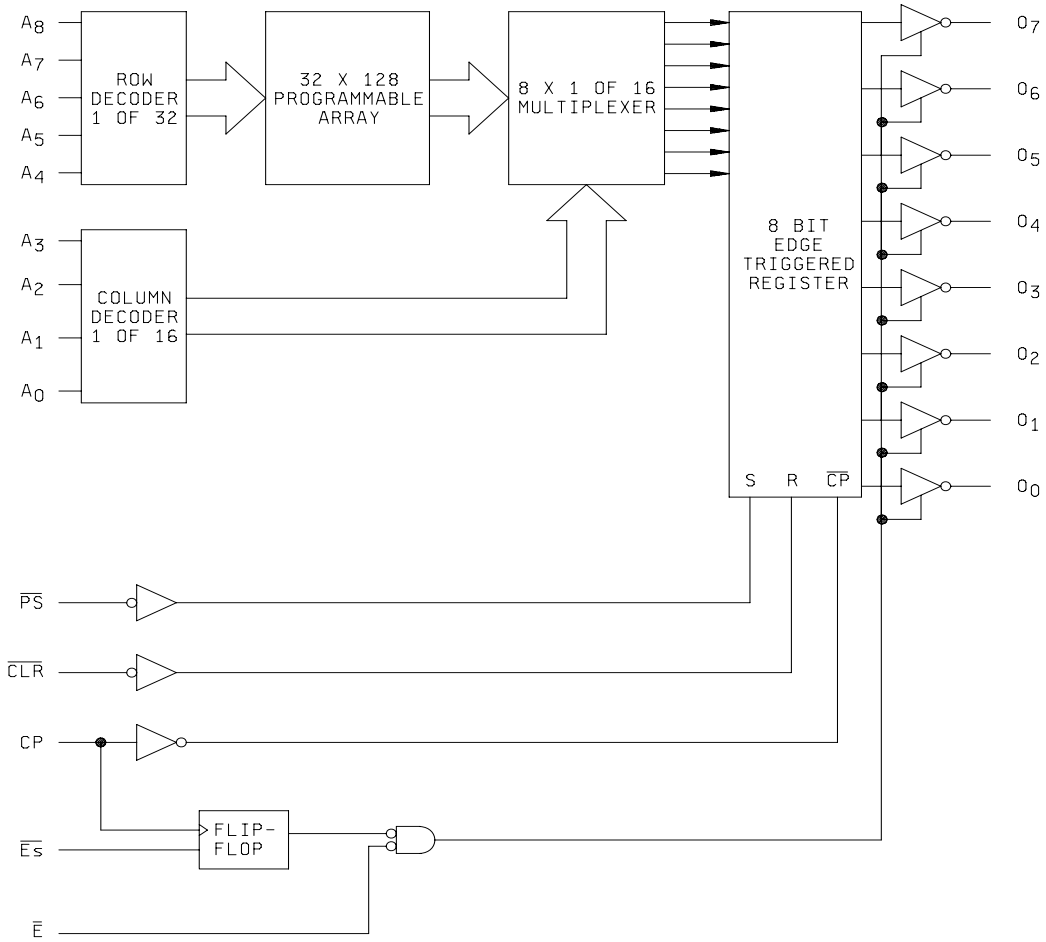
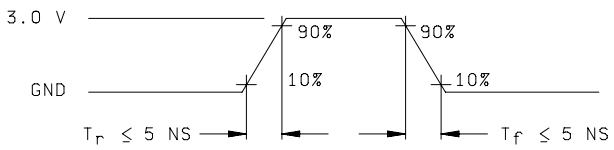
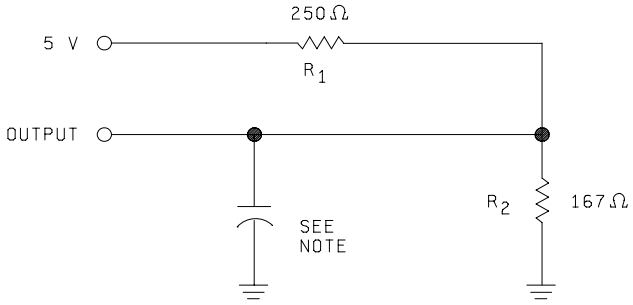


FIGURE 3. Logic diagram

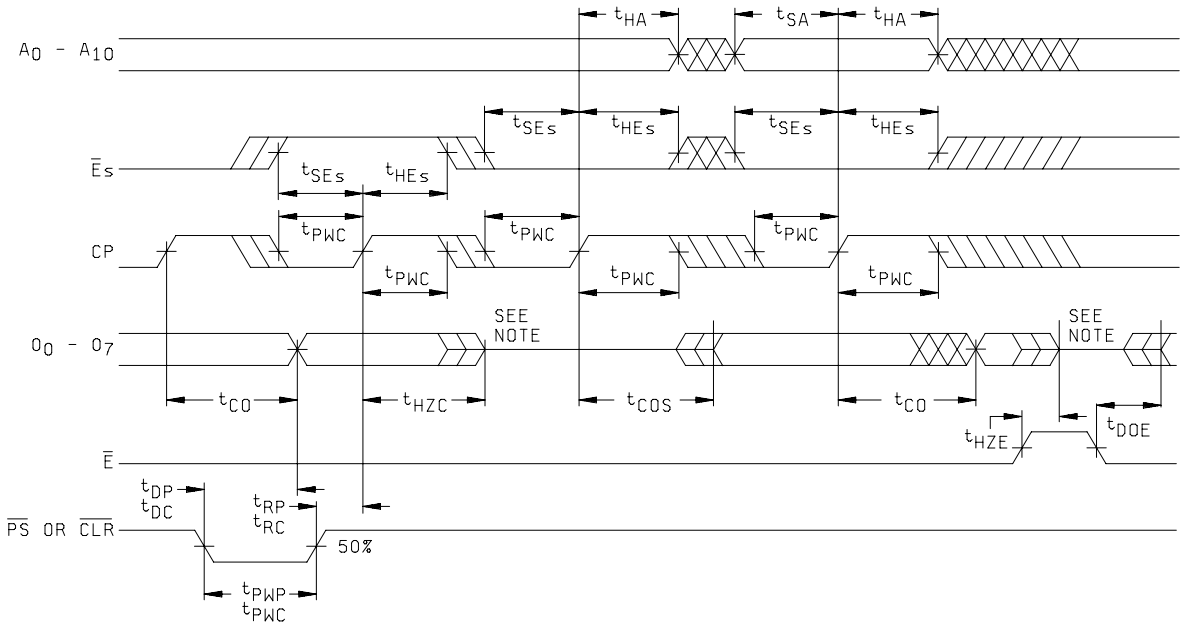


ALL INPUT PULSES



NOTES:
1. C_L includes probe and jig capacitance. C_L = 50 pF for all switching characteristics except t_{HZC} and t_{HZE}. C_L = 5 pF for t_{HZC} and t_{HZE}.
2. Tests are performed with rise and fall times of 5 ns or less.
3. All device test loads should be located within two inches of device outputs.

FIGURE 4. Output load circuit and test conditions.



Note: Transition is measured at steady state high level -500 mV or steady state low level +500 mV on the output from the 1.5 V level on the input with loads shown on figure 4; CL = 5 pF.

FIGURE 5. Switching waveforms.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-STD-883 test requirements	Subgroups (in accordance with Method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7*, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

1/ * Indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ ** See 4.3.1c.
4/ As a minimum, subgroups 7 and 8 shall consist of verifying the data pattern.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures and all input and output terminals tested.

d. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of Group A, subgroups 9, 10, and 11.

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.2.2). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

e. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) TA = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. For quality conformance inspection, the programmability sample (see 4.3.1d) shall be included in subgroup 1 test.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-10-02

Approved sources of supply for SMD 5962-88518 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8851801LA	0C7V7 3/	QP7C225A-30DMB CY7C225-30DMB
5962-88518013A	0C7V7 3/	QP7C225A-30LMB CY7C225-30LMB
5962-8851802LA	0C7V7 3/	QP7C225A-35DMB CY7C225-35DMB
5962-88518023A	0C7V7 3/	QP7C225A-35LMB CY7C225-35LMB
5962-8851803LA	0C7V7 3/	QP7C225A-40DMB CY7C225-40DMB
5962-88518033A	0C7V7 3/	QP7C225A-40LMB CY7C225-40LMB
5962-8851804LA	0C7V7 0C7V7 3/	QP7C225A-30DMB CY7C225A-30DMB CY7C225-30DMB
5962-88518043A	0C7V7 0C7V7 3/	QP7C225A-30LMB CY7C225A-30LMB CY7C225-30LMB
5962-8851805LA	0C7V7 0C7V7 3/	QP7C225A-35DMB CY7C225A-35DMB CY7C225-35DMB
5962-88518053A	0C7V7 0C7V7 3/	QP7C225A-35LMB CY7C225A-35LMB CY7C225-35LMB
5962-8851806LA	0C7V7 0C7V7 3/	QP7C225A-40DMB CY7C225A-40DMB CY7C225-40DMB
5962-88518063A	0C7V7 0C7V7 3/	QP7C225A-40LMB CY7C225A-40LMB CY7C225-40LMB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8851807LA	0C7V7 0C7V7 3/	QP7C225A-25DMB CY7C225A-25DMB CY7C225-25DMB
5962-88518073A	0C7V7 0C7V7 3/	QP7C225A-25LMB CY7C225A-25LMB CY7C225-25LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.