



## THIS SPEC IS OBSOLETE

Spec No: 38-04004

Spec Title: CY7C276 16K x 16 Reprogrammable PROM

Sunset Owner: P Indira (PCI)

Replaced by: None

# 16K x 16 Reprogrammable PROM

## Features

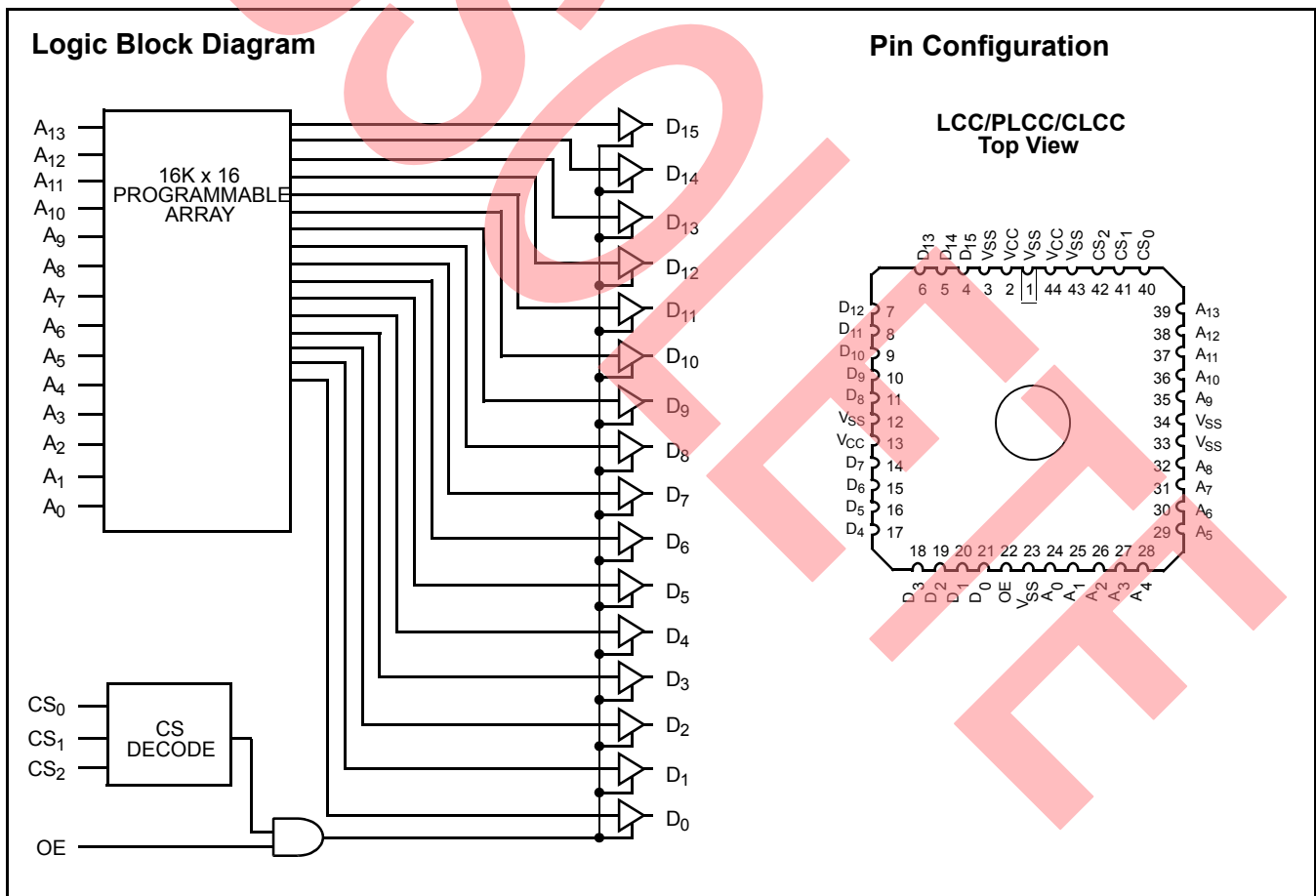
- 0.8-micron CMOS for optimum speed/power
- High speed
  - 25-ns access time
- 16-bit-wide words
- Three programmable chip selects
- Programmable output enable
- 44-pin PLCC and 44-pin LCC packages
- 100% reprogrammable in windowed packages
- TTL-compatible I/O
- Capable of withstanding greater than 2001V static discharge

## Functional Description

The CY7C276 is a high-performance 16K-word by 16-bit CMOS PROM. It is available in a 44-pin PLCC and a 44-pin LCC packages, and is 100% reprogrammable in windowed packages. The memory cells utilize proven EPROM floating gate technology and word-wide programming algorithms.

The CY7C276 allows the user to independently program the polarity of each chip select ( $CS_2$ – $CS_0$ ). This provides on-chip decoding of up to eight banks of PROM. The polarity of the asynchronous output enable pin (OE) is also programmable.

In order to read the CY7C276, all three chip selects must be active and OE must be asserted. The contents of the memory location addressed by the address lines ( $A_{13}$ – $A_0$ ) will become available on the output lines ( $D_{15}$ – $D_0$ ). The data will remain on the outputs until the address changes or the outputs are disabled.



**Selection Guide**

|                           |            | <b>CY7C276-25</b> | <b>CY7C276-30</b> | <b>Unit</b> |
|---------------------------|------------|-------------------|-------------------|-------------|
| Maximum Access Time       |            | 25                | 30                | ns          |
| Maximum Operating Current | Commercial | 175               | 175               | mA          |

**Maximum Ratings<sup>[1]</sup>**

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature .....                           | -65°C to +150°C |
| Ambient Temperature with Power Applied.....         | -55°C to +125°C |
| Supply Voltage to Ground Potential.....             | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State ..... | -0.5V to +7.0V  |
| DC Input Voltage.....                               | -3.0V to +7.0V  |

|                               |                                       |
|-------------------------------|---------------------------------------|
| DC Program Voltage .....      | 13.0V                                 |
| UV Erasure .....              | 7258 Wsec/cm <sup>2</sup>             |
| Static Discharge Voltage..... | >2001V (per MIL-STD-883, Method 3015) |
| Latch-Up Current.....         | >200 mA                               |

**Operating Range**

| <b>Range</b> | <b>Ambient Temperature</b> | <b>V<sub>CC</sub></b> |
|--------------|----------------------------|-----------------------|
| Commercial   | 0°C to +70°C               | 5V ±10%               |

**Electrical Characteristics<sup>[2, 3]</sup>**

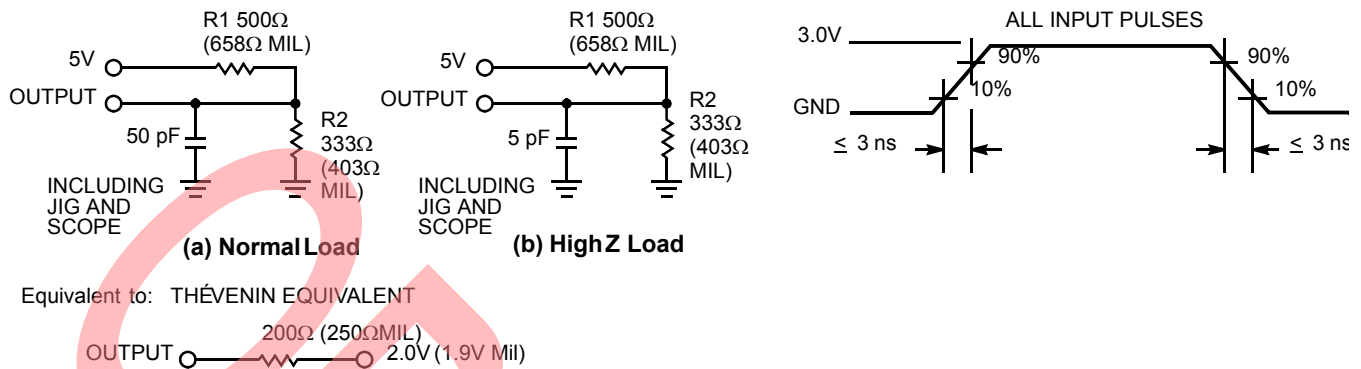
| <b>Parameter</b> | <b>Description</b>           | <b>Test Conditions</b>  | <b>CY7C276-25<br/>CY7C276-30</b> |                 | <b>Unit</b> |
|------------------|------------------------------|---|----------------------------------|-----------------|-------------|
|                  |                              |   | <b>Min.</b>                      | <b>Max.</b>     |             |
| V <sub>OH</sub>  | Output HIGH Voltage          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA   | 2.4                              |                 | V           |
| V <sub>OL</sub>  | Output LOW Voltage           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA (6.0 mA Mil)                                     |                                  | 0.4             | V           |
| V <sub>IH</sub>  | Input HIGH Level             | Guaranteed Input Logical HIGH Voltage for All Inputs  | 2.0                              | V <sub>CC</sub> | V           |
| V <sub>IL</sub>  | Input LOW Level              | Guaranteed Input Logical LOW Voltage for All Inputs   | -3.0                             | 0.8             | V           |
| I <sub>IX</sub>  | Input Leakage Current        | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>   | -10                              | +10             | μA          |
| V <sub>CD</sub>  | Input Clamp Diode Voltage    |   | Note 2                           |                 | μA          |
| I <sub>OZ</sub>  | Output Leakage Current       | V <sub>CC</sub> = Max., V <sub>OL</sub> ≤ V <sub>OUT</sub> ≤ V <sub>OH</sub> ,<br>Output Disabled | -40                              | +40             | μA          |
| I <sub>OS</sub>  | Output Short Circuit Current | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0V <sup>[4]</sup>                                    | -20                              | -90             | mA          |
| I <sub>CC</sub>  | Power Supply Current         | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0.0 mA   | Com'l                            | 175             | mA          |

**Capacitance<sup>[2]</sup>**

| <b>Parameter</b> | <b>Description</b> | <b>Test Conditions</b>                                      | <b>Max.</b> | <b>Unit</b> |
|------------------|--------------------|---|-------------|-------------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 10          | pF          |
| C <sub>OUT</sub> | Output Capacitance |   | 10          | pF          |

**Notes:**

1. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. See Introduction to CMOS PROMs in this Data Book for general information on testing.
3. See the last page of this specification for Group A subgroup testing information.
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

**AC Test Loads and Waveforms**

**Switching Characteristics** Over the Operating Range<sup>[2,3]</sup>

| Parameter  | Description                  | CY7C276-25 |      | CY7C276-30 |      | Unit |
|------------|------------------------------|------------|------|------------|------|------|
|            |                              | Min.       | Max. | Min.       | Max. |      |
| $t_{AA}$   | Address to Output Data Valid |            | 25   |            | 30   | ns   |
| $t_{CSOV}$ | CS Active to Output Valid    |            | 13   |            | 15   | ns   |
| $t_{CSOZ}$ | CS Inactive to High Z Output |            | 13   |            | 15   | ns   |
| $t_{OEV}$  | OE Active to Output Valid    |            | 11   |            | 12   | ns   |
| $t_{OEZ}$  | OE Inactive to High Z Output |            | 11   |            | 12   | ns   |

**Erasure Characteristics**

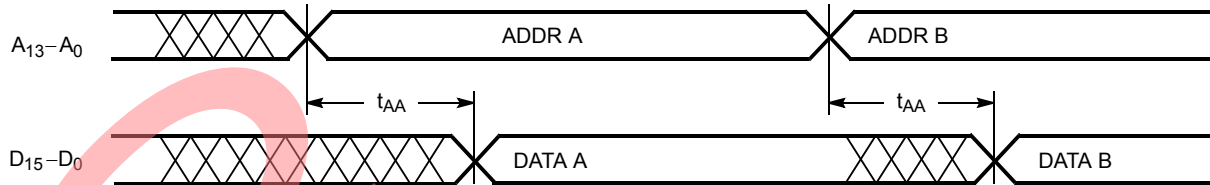
The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating the exposure time would be approximately 35 minutes. The CY7C276 needs to be within 1 inch of the lamp during erasure.

Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm<sup>2</sup> is the recommended maximum dosage.

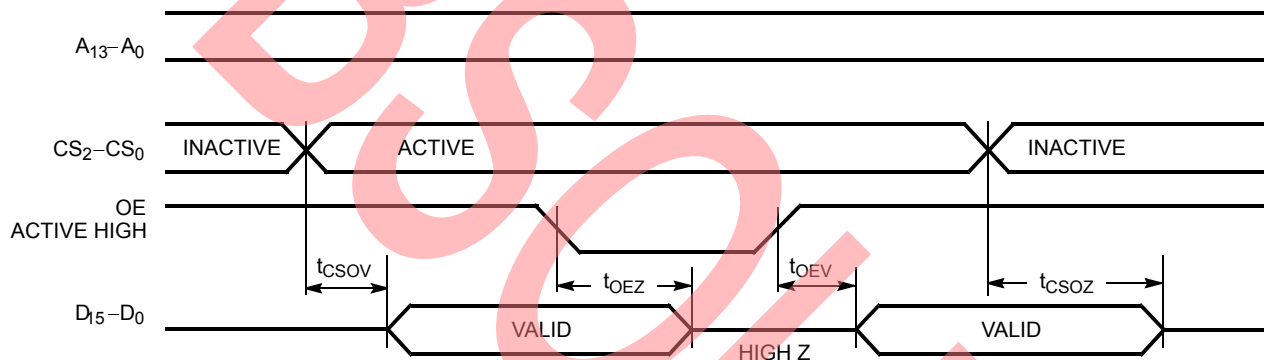
Wavelengths of light less than 4000 Angstroms begin to erase the CY7C276 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

## Switching Waveforms

### Read Operation Timing Diagram <sup>[5]</sup>



### Chip Select and Output Enable Timing Diagrams



**Note:**

- CS<sub>2</sub> - CS<sub>0</sub>, OE assumed active.

### Architecture Configuration Bits

The CY7C276 has four user-programmable options in addition to the reprogrammable data array. For detailed programming information contact your local Cypress representative.

The programmable options determine the active polarity for the three chip selects (CS<sub>2</sub>-CS<sub>0</sub>) and OE. When these control bits are programmed with a 0 the inputs are active LOW. When these control bits are programmed with a 1 the inputs are active HIGH.

### Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

**Table 1. Control Word for Architecture Configuration**

| Control Option  | Control Word    |                               | Function  |
|-----------------|-----------------|-------------------------------|---|
|                 | Bit             | Programmed Level              |   |
| OE              | D <sub>0</sub>  | 0 = Default<br>1 = Programmed | OE Active LOW<br>OE Active HIGH                           |
| CS <sub>0</sub> | D <sub>12</sub> | 0 = Default<br>1 = Programmed | CS <sub>0</sub> Active LOW<br>CS <sub>0</sub> Active HIGH |
| CS <sub>1</sub> | D <sub>13</sub> | 0 = Default<br>1 = Programmed | CS <sub>1</sub> Active LOW<br>CS <sub>1</sub> Active HIGH |
| CS <sub>2</sub> | D <sub>14</sub> | 0 = Default<br>1 = Programmed | CS <sub>2</sub> Active LOW<br>CS <sub>2</sub> Active HIGH |

**Bit Map**

| Programmer Address (Hex) | RAM Data     |
|--------------------------|--------------|
| 0000                     | Data         |
| ·                        | ·            |
| ·                        | ·            |
| ·                        | ·            |
| 3FFF                     | Data         |
| 4000                     | Control Word |

Control Word (4000H)

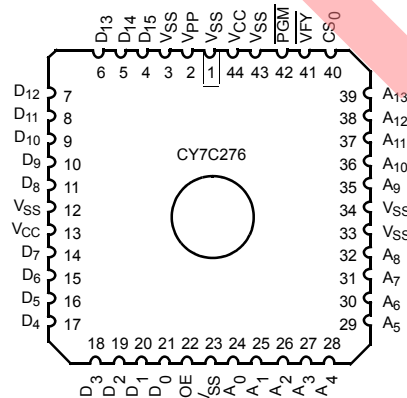
 D15 D0  
 X CS2 CS1 CS0 X X X X X X X X 1 X X OE

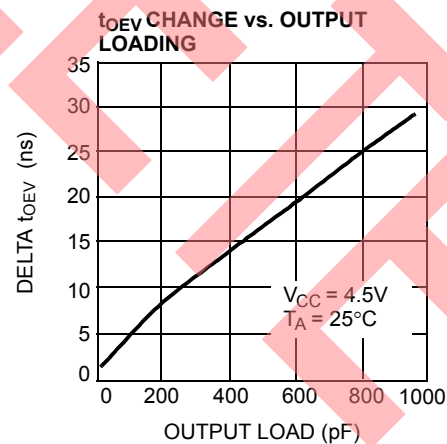
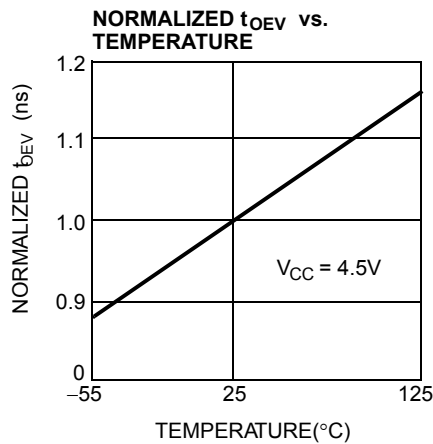
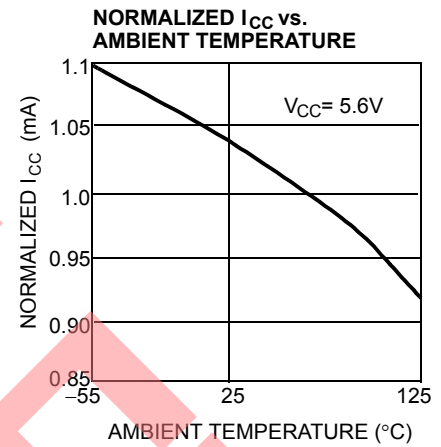
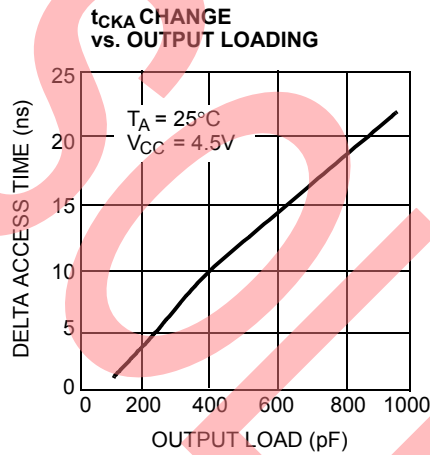
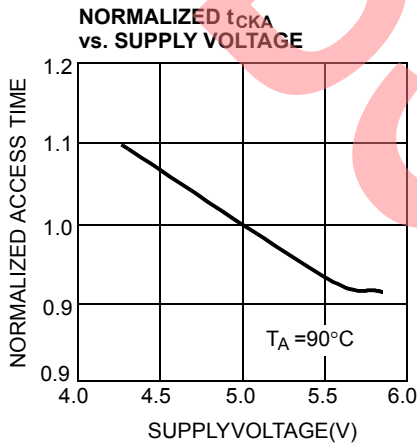
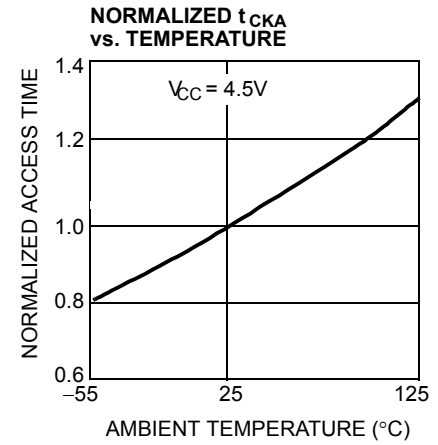
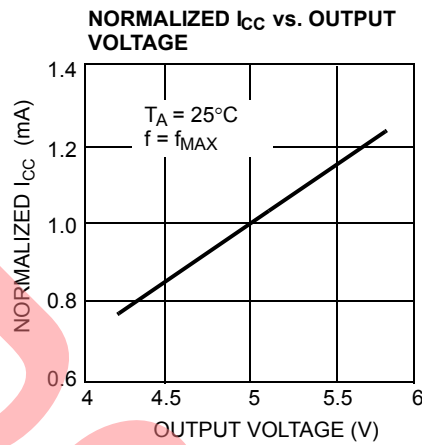
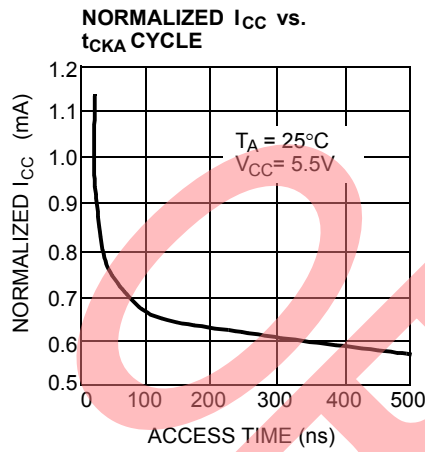
**Table 2. Program Mode Table**

| Mode            | V <sub>PP</sub> | PGM              | V <sub>FY</sub>  | D <sub>0</sub> -D <sub>15</sub> |
|-----------------|-----------------|------------------|------------------|---------------------------------|
| Program Inhibit | V <sub>PP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | High Z                          |
| Program Enable  | V <sub>PP</sub> | V <sub>ILP</sub> | V <sub>IHP</sub> | Data                            |
| Program Verify  | V <sub>PP</sub> | V <sub>IHP</sub> | V <sub>ILP</sub> | Data                            |

**Table 3. Configuration Mode Table**

| Mode                 | V <sub>PP</sub> | PGM              | V <sub>FY</sub>  | A <sub>2</sub>  | D <sub>0</sub> -D <sub>15</sub> |
|----------------------|-----------------|------------------|------------------|-----------------|---------------------------------|
| Program Inhibit      | V <sub>PP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub> | High Z                          |
| Program Control Word | V <sub>PP</sub> | V <sub>ILP</sub> | V <sub>IHP</sub> | V <sub>PP</sub> | Control Word                    |
| Verify Control Word  | V <sub>PP</sub> | V <sub>IHP</sub> | V <sub>ILP</sub> | V <sub>PP</sub> | Control Word                    |


**Figure 1. Programming Pinout**

**Typical DC and AC Characteristics**


**Ordering Information**

| Speed (ns) | Ordering Code | Package Name | Package Type                        | Operating Range |
|------------|---------------|--------------|-------------------------------------|-----------------|
| 25         | CY7C276-25HC  | H67          | 44-Pin Windowed Leaded Chip Carrier | Commercial      |
|            | CY7C276-25JC  | J67          | 44-Lead Plastic Leaded Chip Carrier |                 |
| 30         | CY7C276-30JC  | J67          | 44-Lead Plastic Leaded Chip Carrier | Commercial      |

**MILITARY SPECIFICATIONS**  
**Group A Subgroup Testing**
**DC Characteristics**

| Parameter | Subgroups |
|-----------|-----------|
| $V_{OH}$  | 1, 2, 3   |
| $V_{OL}$  | 1, 2, 3   |
| $V_{IH}$  | 1, 2, 3   |
| $V_{IL}$  | 1, 2, 3   |
| $I_{IX}$  | 1, 2, 3   |
| $I_{OZ}$  | 1, 2, 3   |
| $I_{CC}$  | 1, 2, 3   |

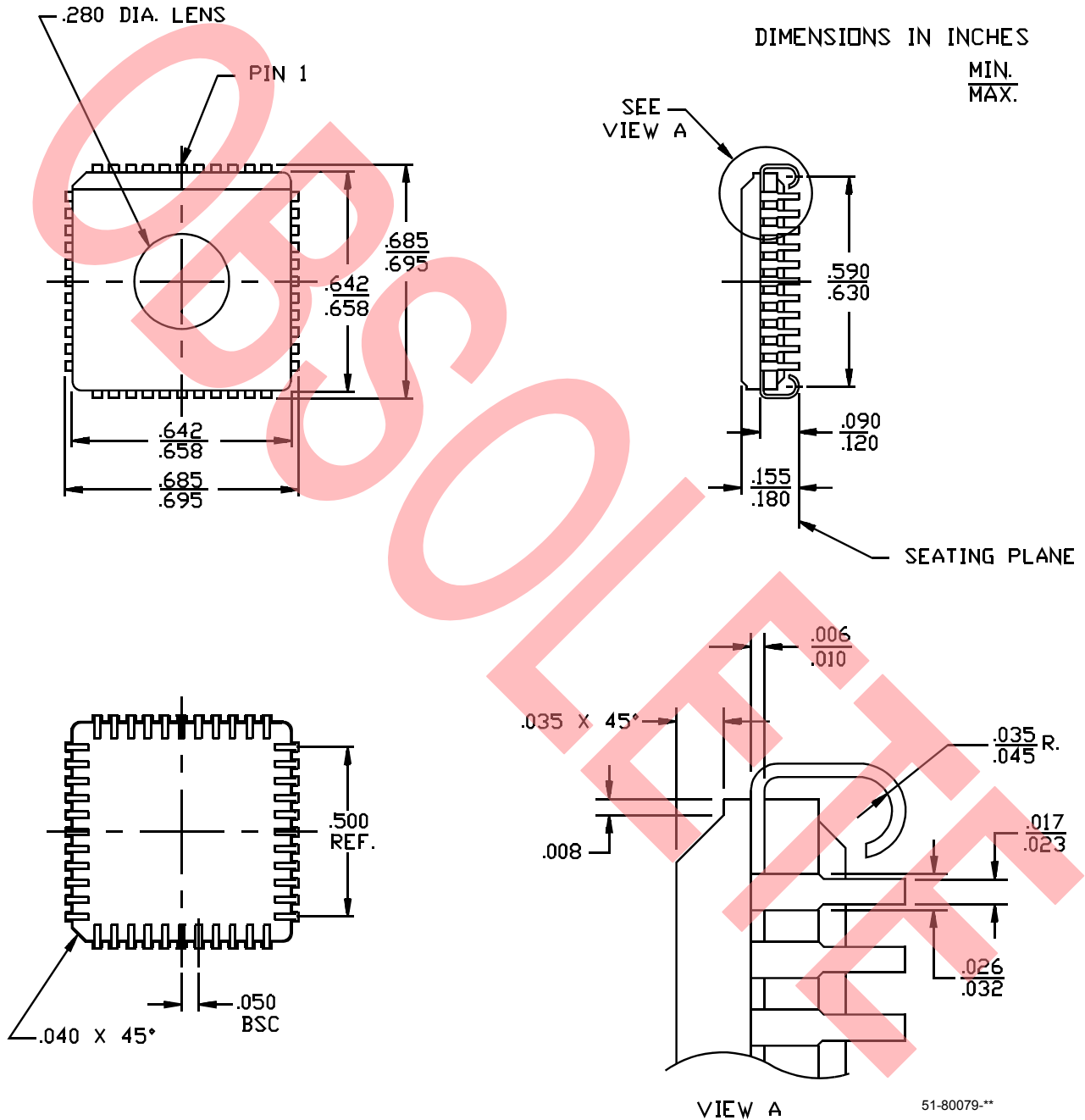
**Switching Characteristics**

| Parameter  | Subgroups       |
|------------|-----------------|
| $t_{AA}$   | 7, 8, 9, 10, 11 |
| $t_{CSOV}$ | 7, 8, 9, 10, 11 |
| $t_{OEV}$  | 7, 8, 9, 10, 11 |

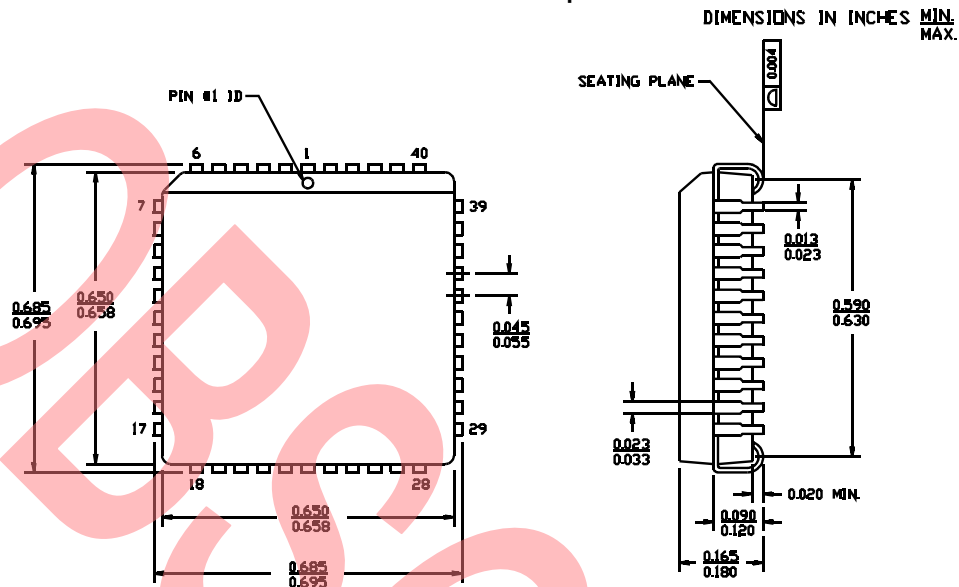


Package Diagrams

44-Pin Windowed Leaded Chip Carrier H67



**Package Diagrams** (continued)

**44-Lead Plastic Leaded Chip Carrier J67**


51-85003-\*A

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## Document History Page

| Document Title: CY7C276 16K x 16 Reprogrammable PROM<br>Document Number: 38-04004 |                   |                     |                 |  |
|---|-------------------|---------------------|-----------------|--|
| REV.  | ECN NO.           | Issue Date          | Orig. of Change | Description of Change  |
| **  | 113860            | 03/06/02            | DSG             | Change from Spec number: 38-00183 to 38-04004                              |
| *A  | 118900            | 10/09/02            | GBI             | Update ordering information  |
| *B  | <del>122245</del> | <del>12/27/02</del> | RBI             | Add power up requirements to Maximum Ratings information                   |
| *C  | 504720            | See ECN             | PCI             | Obsolete Device. Datasheet to be removed from Cypress web and spec. system |