CY7C261
CY7C263/CY7C264

8K x 8 Power-Switched and Reprogrammable PROM

Features

- CMOS for optimum speed/power
- Windowed for reprogrammability
- High speed
  - — 20 ns (Commercial)
  - — 25 ns (Military)
- Low power
  - — 660 mW (Commercial)
  - — 770 mW (Military)
- Super low standby power (7C261)
  - — Less than 220 mW when deselected
  - — Fast access: 20 ns
- EPROM technology 100% programmable
- Slim 300-mil or standard 600-mil packaging available
- 5V ± 10% V_{CC}, commercial and military
- Capable of withstanding greater than 2001V static discharge
- TTL-compatible I/O
- Direct replacement for bipolar PROMs

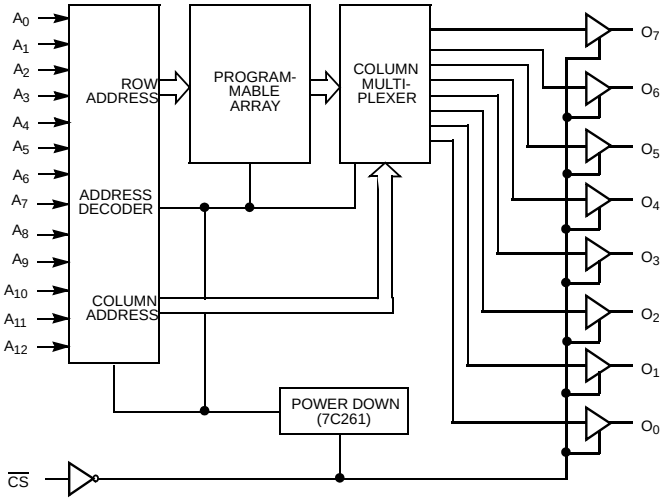
Functional Description

The CY7C261, CY7C263, and CY7C264 are high-performance 8192-word by 8-bit CMOS PROMs. When deselected, the CY7C261 automatically powers down into a low-power standby mode. It is packaged in a 300-mil-wide package. The CY7C263 and CY7C264 are packaged in 300-mil-wide and 600-mil-wide packages respectively, and do not power down when deselected. The reprogrammable packages are equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C261, CY7C263, and CY7C264 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

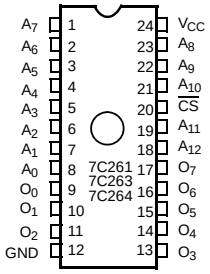
Read is accomplished by placing an active LOW signal on $\overline{CS}$. The contents of the memory location addressed by the address line (A_0–A_{12}) will become available on the output lines (O_0–O_7).

Logic Block Diagram

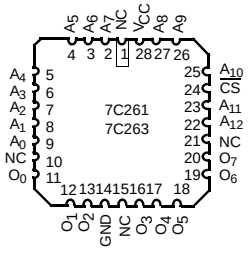


Pin Configurations

DIP/Flatpack Top View



LCC/PLCC (Opaque Only) Top View



For an 8K x 8 Registered PROM, see theCY7C265.

Selection Guide

		7C261-20 7C263-20 7C264-20	7C261-25 7C263-25 7C264-25	7C261-35 7C263-35 7C264-35	7C261-45 7C263-45 7C264-45	7C261-55 7C263-55 7C264-55	Unit
Maximum Access Time		20	25	35	45	55	ns
Maximum Operating Current	Commercial	120	120	100	100	100	mA
	Military		140	120	120	120	mA
Maximum Standby Current (7C261 only)	Commercial	40	40	30	30	30	mA
	Military		40	30	30	30	mA

Maximum Ratings[1]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperatures.....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12).....–0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State.....–0.5V to +7.0V

DC Input Voltage.....–3.0V to + 7.0V

DC Program Voltage (Pin 19 DIP, Pin 23 LCC).....13.0V

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Latch-Up Current.....>200 mA

UV Exposure.....7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[2]	–55°C to + 125°C	5V ± 10%

Notes
1. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. T_A is the “instant on” case temperature.

Electrical Characteristics Over the Operating Range[3,4]

Parameter	Description	Test Conditions		7C261-20, 25 7C263-20, 25 7C264-20, 25		7C261-35, 45, 55 7C263-35, 45, 55 7C264-35, 45, 55		Unit
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4				V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA				2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA (6 mA Mil)			0.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA					0.4	V
V_{IH}	Input HIGH Level			2.0		2.0		V
V_{IL}	Input LOW Level				0.8		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		–10	+10	–10	+10	µA
V_{CD}	Input Diode Clamp Voltage			Note 4		Note 4		
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC} Output Disabled	Com'l	–10	+10	–10	+10	µA
			Mil	–40	+40	–40	+40	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		–20	–90	–20	–90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., f = Max. I_{OUT} = 0 mA	Com'l		120		100	mA
			Mil		140		120	
I_{SB}	Standby Supply Current (7C261)	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}	Com'l		40		30	mA
			Mil		40		30	
V_{PP}	Programming Supply Voltage			12	13	12	13	V
I_{PP}	Programming Supply Current				50		50	mA
V_{IHP}	Input HIGH Programming Voltage			4.75		4.75		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4	V

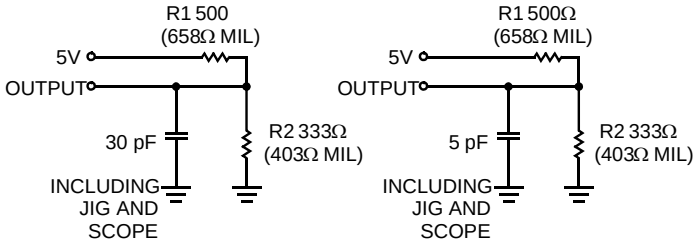
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

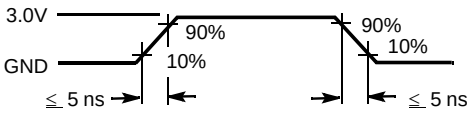
Notes
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms[4]

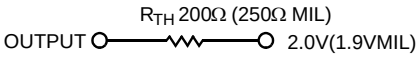
Test Load for -20 through -30 speeds



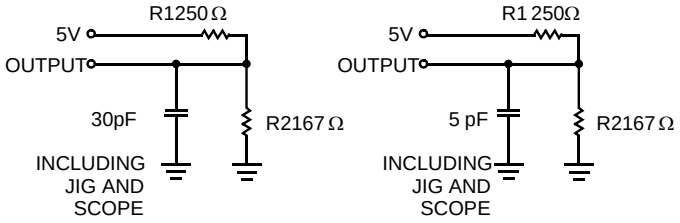
(a) Normal Load **(b) High Z Load**



Equivalent to: THÉVENIN EQUIVALENT

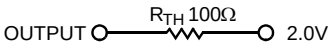


Test Load for -35 through -55 speeds



(c) Normal Load **(d) High Z Load**

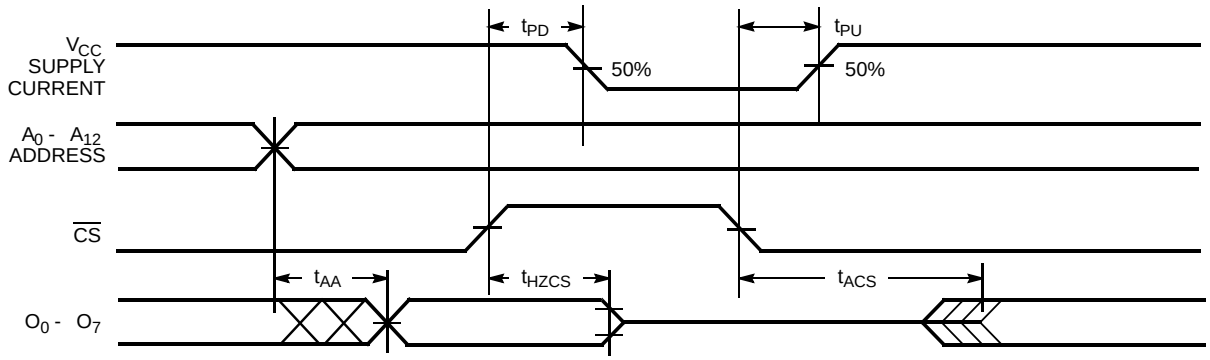
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range [1,3,4]

Parameter	Description	7C261-20 7C263-20 7C264-20		7C261-25 7C263-25 7C264-25		7C261-35 7C263-35 7C264-35		7C261-45 7C263-45 7C264-45		7C261-55 7C263-55 7C264-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		20		25		35		45		55	ns
t_{HZCS1}	Chip Select Inactive to High Z (7C263 and 7C264)		12		12		20		30		35	ns
t_{HZCS2}	Chip Select Inactive to High Z (7C261)		20		25		35		45		55	ns
t_{ACS1}	Chip Select Active to Output Valid (7C263 and 7C264)		12		12		20		30		35	ns
t_{ACS2}	Chip Select Active to Output Valid (7C261)		20		25		35		45		55	ns
t_{PU}	Chip Select Active to Power-Up (7C261)	0		0		0		0		0		ns
t_{PD}	Chip Select Inactive to Power-Down (7C261)		20		25		35		45		55	ns

Switching Waveforms[4]



Erasure Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the devices in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The 7C261 or 7C263 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Operating Modes

Read

Read is the normal operating mode for programmed device. In this mode, all signals are normal TTL levels. The PROM is addressed with a 13-bit field, a chip select, (active LOW), is applied to the $\overline{CS}$ pin, and the contents of the addressed location appear on the data out pins.

Program, Program Inhibit, Program Verify

These modes are entered by placing a high voltage V_{PP} on pin 19, with pins 18 and 20 set to V_{ILP}. In this state, pin 21 becomes a latch signal, allowing the upper 5 address bits to be latched into an onboard register, pin 22 becomes an active LOW program ($\overline{PGM}$) signal and pin 23 becomes an active LOW verify ($\overline{VFY}$) signal. Pins 22 and 23 should never be active LOW at the same time. The PROGRAM mode exists when $\overline{PGM}$ is LOW, and $\overline{VFY}$ is HIGH. The verify mode exists when the reverse is true, $\overline{PGM}$ HIGH and $\overline{VFY}$ LOW and the program inhibit mode is entered with both $\overline{PGM}$ and $\overline{VFY}$ HIGH. Program inhibit is specifically provided to allow data to be placed on and removed from the data pins without conflict

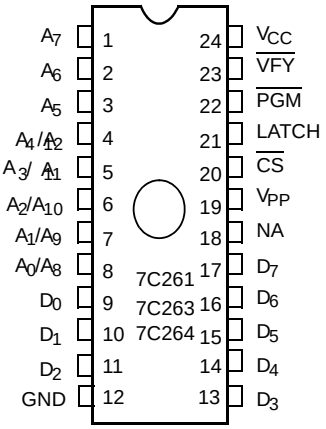
Table 1. Mode Selection

Mode	Read or Output Disable / Program	Pin Function[6, 7] A_{12}	A_{11}	A_{10}	A_9	A_8	$\overline{CS}$	O_7–O_0
		NA	V_{PP}	LATCH	PGM	VFY	CS	D_7–D_0
Read		A_{12}	A_{11}	A_{10}	A_9	A_8	V_{IL}	O_7–O_0
Output Disable		A_{12}	A_{11}	A_{10}	A_9	A_8	V_{IH}	High Z
Program		V_{ILP}	V_{PP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	D_7–D_0
Program Inhibit		V_{ILP}	V_{PP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	High Z
Program Verify		V_{ILP}	V_{PP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	O_7–O_0
Blank Check		V_{ILP}	V_{PP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	O_7–O_0

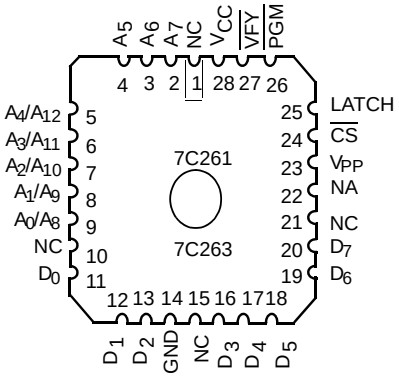
Notes
6. X = "don't care" but not to exceed V_{CC} ±5%.
7. Addresses A_8-A_{12} must be latched through lines A_0-A_4 in programming modes.

Figure 1. Programming Pinouts

DIP/Flatpack
Top View



LCC/PLCC (Opaque only)
Top View

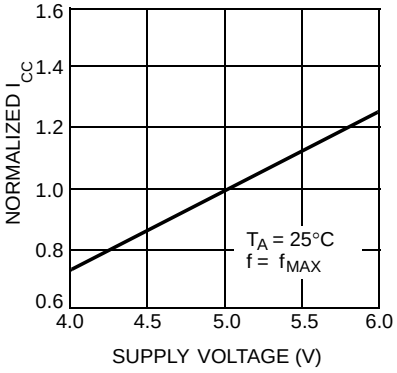


Programming Information

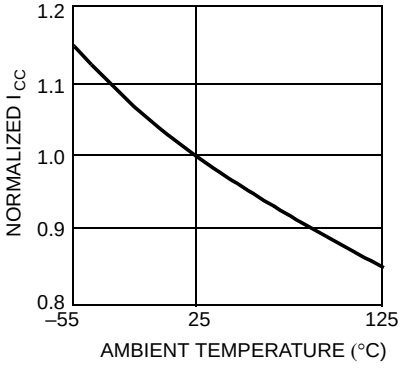
Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Typical DC and AC Characteristics

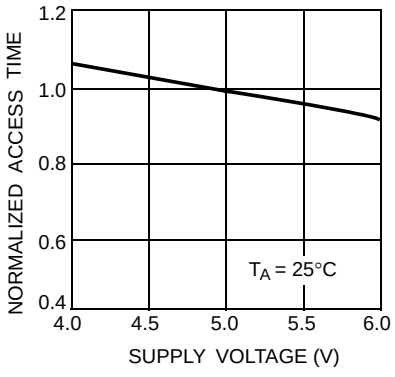
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



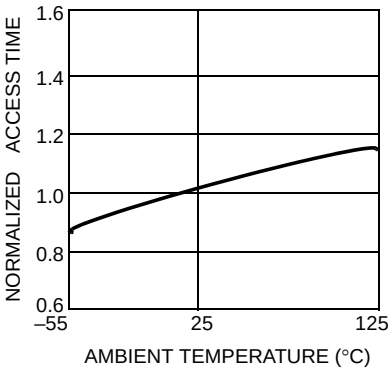
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



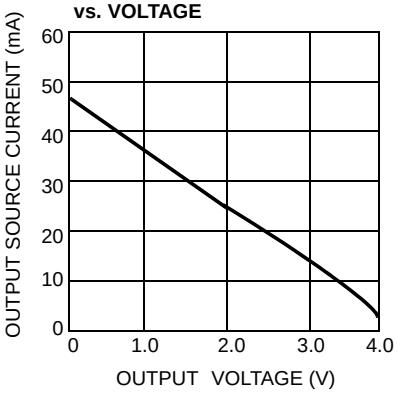
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



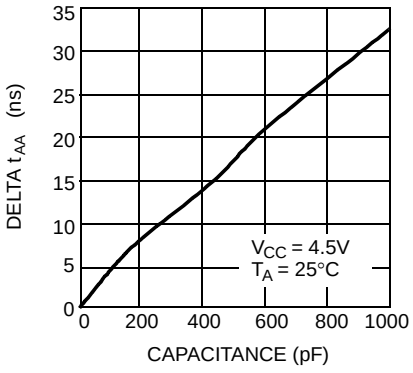
NORMALIZED ACCESS TIME vs. TEMPERATURE



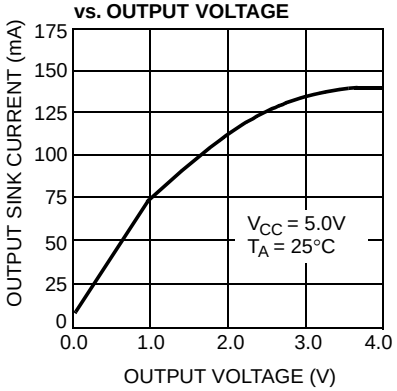
OUTPUT SOURCE CURRENT vs. VOLTAGE



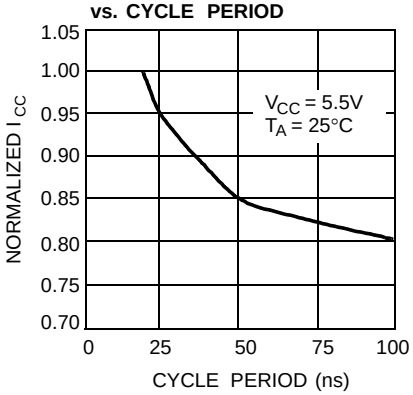
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED SUPPLY CURRENT vs. CYCLE PERIOD



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C261-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C261-20WC	W14	24-Lead (300-Mil) Windowed CerDIP	
25	CY7C261-25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C261-25PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7C261-25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	Military
35	CY7C261-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C261-35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
45	CY7C261-45PC	P13	224-Lead (300-Mil) Molded DIP	Commercial
	CY7C261-45WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C261-45WMB	W14	24-Lead (300-Mil) Windowed CerDIP	Military
55	CY7C261-55WC	W14	24-Lead (300-Mil) Windowed CerDIP	Commercial
20	CY7C263-20JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C263-20WC	W14	24-Lead (300-Mil) Windowed CerDIP	
25	CY7C263-25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C263-25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	CY7C263-25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	Military
	CY7C263-25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
35	CY7C263-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C263-35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
55	CY7C263-55JI	J64	28-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C263-55WMB	W14	24-Lead (300-Mil) Windowed CerDIP	Military
35	CY7C264-35PC	P11	24-Lead (600-Mil) Molded DIP	Commercial
45	CY7C264-45WC	W12	24-Lead (600-Mil) Windowed CerDIP	Commercial
	CY7C264-45WMB	W12	24-Lead (600-Mil) Windowed CerDIP	Military
55	CY7C264-55WC	W12	24-Lead (600-Mil) Windowed CerDIP	Commercial

MILITARY SPECIFICATION

Group A Subgroup Testing

DC Characteristics

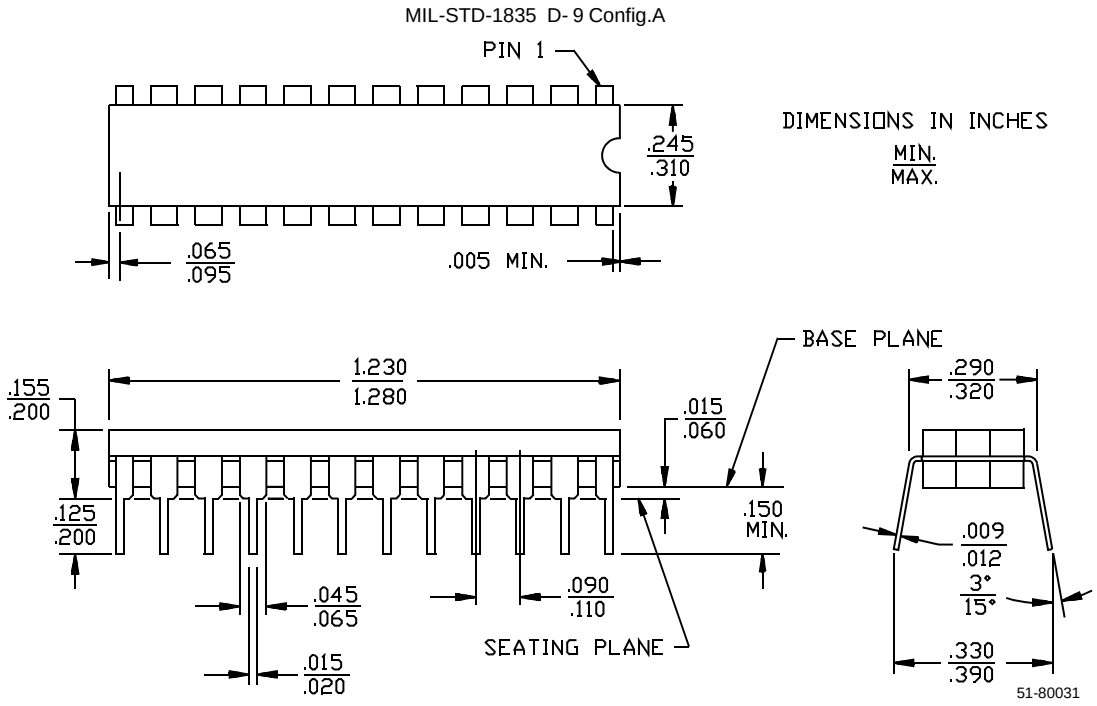
Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}[8]	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{ACS1}[9]	7, 8, 9, 10, 11
t_{ACS2}[8]	7, 8, 9, 10, 11

Package Diagrams

Figure 2. 24-Lead (300-Mil) CerDIP D14



Notes
8. 7C261 only.
9. 7C263 and 7C264 only.

Package Diagrams (continued)

Figure 3. 28-Lead Plastic Leaded Chip Carrier J64

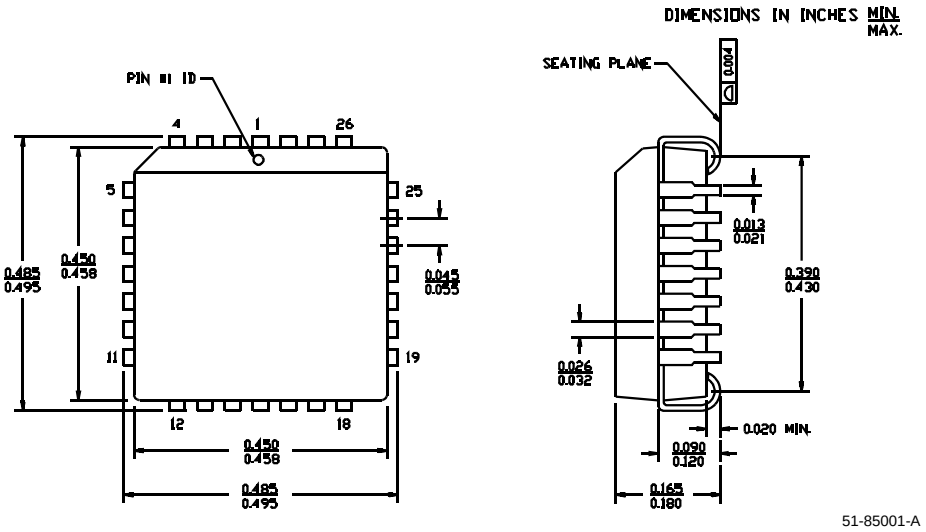
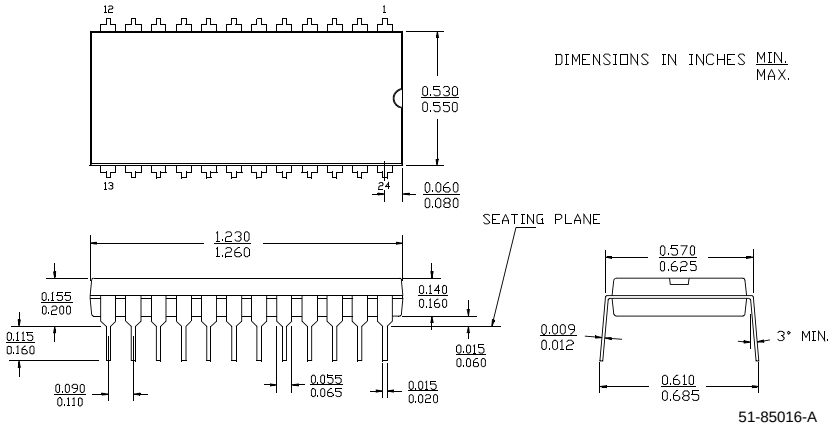


Figure 4. 24-Lead (600-Mil) Molded DIP P11



Package Diagrams (continued)

Figure 5. 24-Lead (300-Mil) PDIP P13

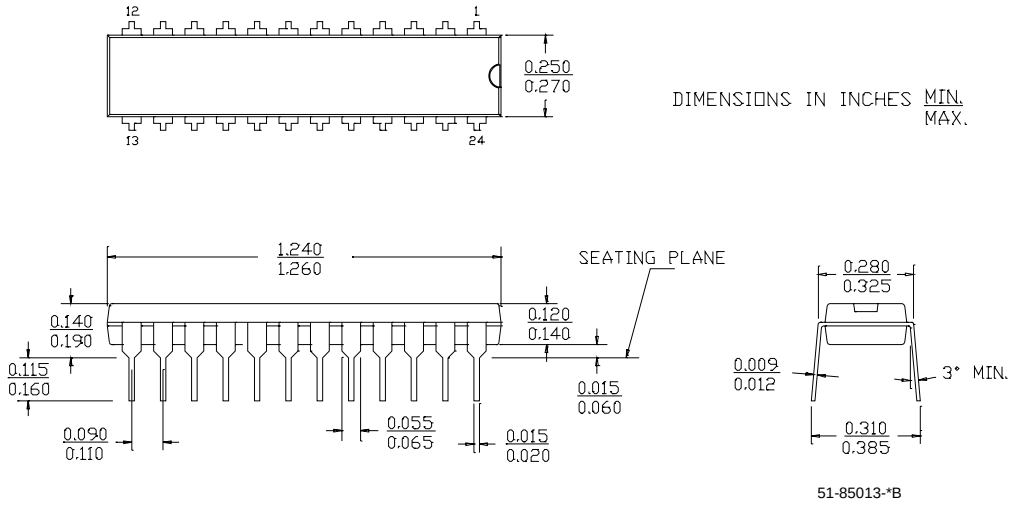
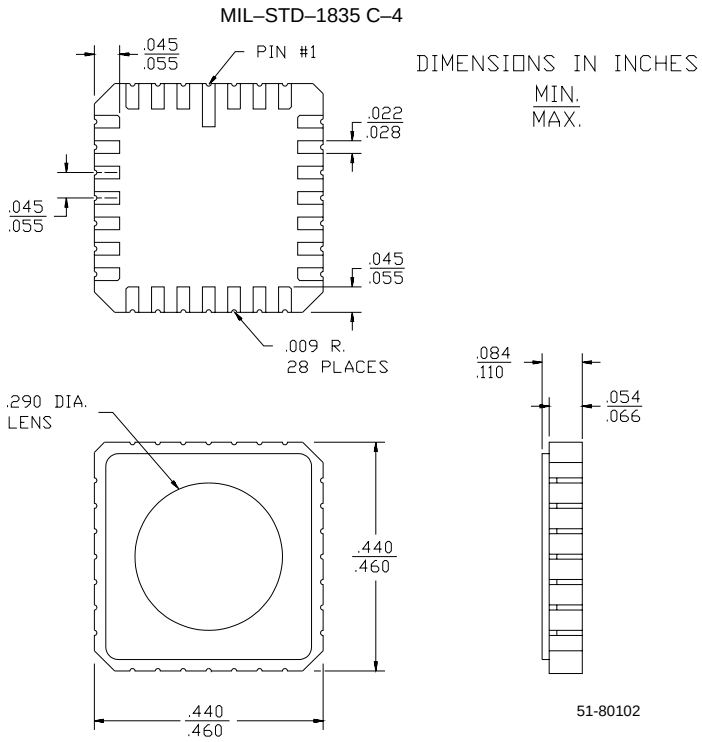
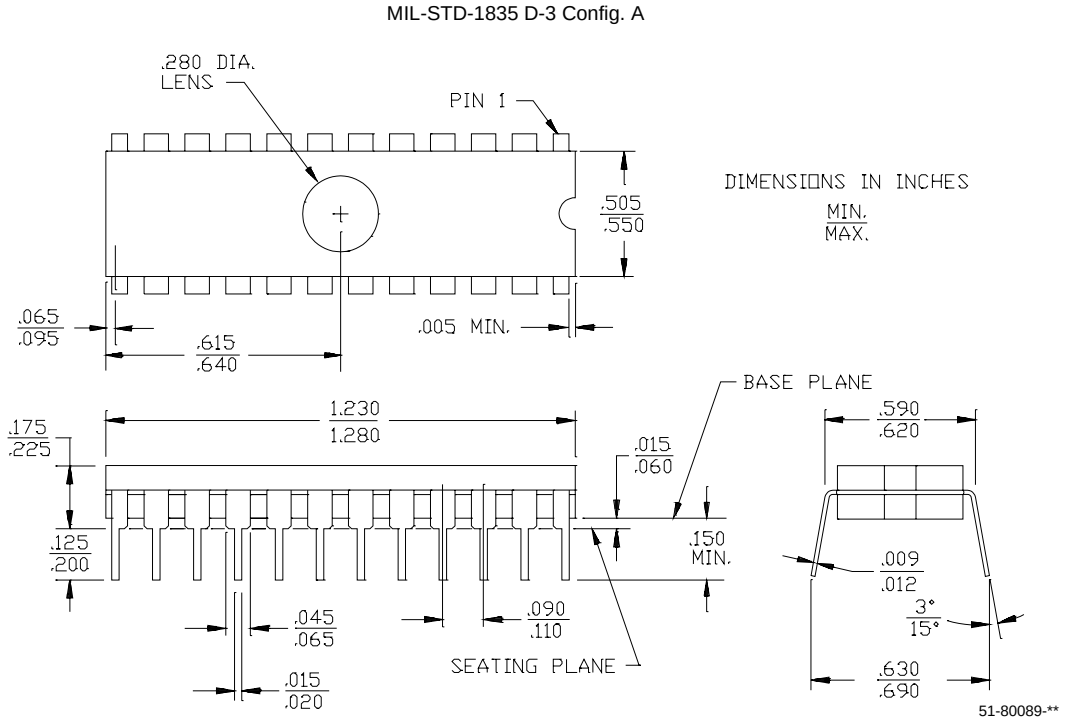


Figure 6. 28-Pin Windowed Leadless Chip Carrier Q64



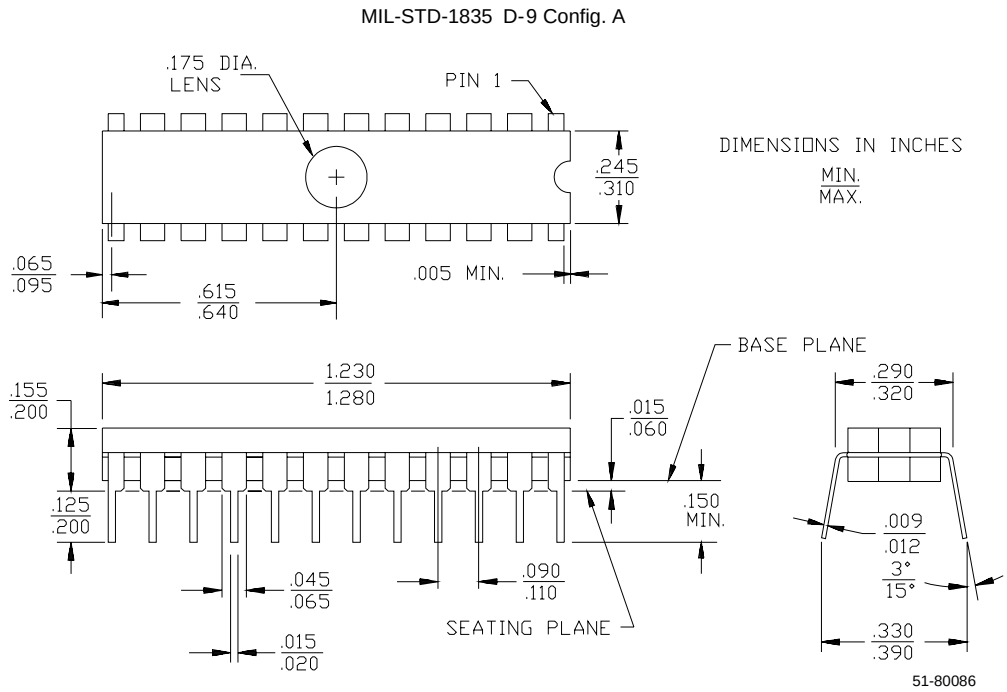
Package Diagrams (continued)

Figure 7. 24-Lead (600-Mil) Windowed CerDIP W12



Package Diagrams (continued)

Figure 8. 24-Lead (300-Mil) Windowed CerDIP W14



Document History Page

Document Title: CY7C261 CY7C263/CY7C264 8K x 8 Power Switched and Reprogrammable PROM Document Number: 38-04010				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	113866	3/6/02	DSG	Changed from Spec number: 38-00005 to 38-04010
*A	118895	10/09/02	GBI	Updated Ordering Information
*B	122251	12/28/02	RBI	Added power up requirements to Maximum Ratings information
*C	499542	See ECN	PCI	Updated Ordering Information