HIGH-SPEED 2K x 8 REGISTERED CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  - — 25 ns Setup
  - — 12 ns Clock to Output
- **Low Power Consumption**
- **Fast Programming**
- **Programmable Synchronous or Asynchronous Output Enable**
- **DESC SMD Nos. 5962-88735/5962-87529**
- **Pin Compatible with AM27S45 and CY7C245**
- **Immune to Latch-UP**
  - — Up to 200 mA
- **ESD Protection Exceeds 2000 V**
- **Programmable Asynchronous Initialize Register**

GENERAL DESCRIPTION

The WS57C45 is an extremely High Performance 16K UV Erasable Registered CMOS RPROM. It is a direct drop-in replacement for such devices as the AM27S45 and CY7C245.

To meet the requirements of systems which execute and fetch instructions simultaneously, an 8-bit parallel data register has been provided at the output which allows RPROM data to be stored while other data is being addressed.

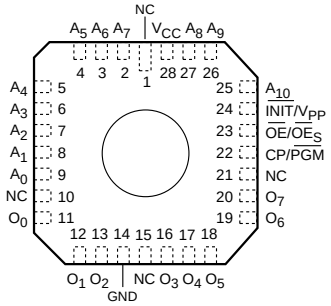
An asynchronous initialization feature has been provided which enables a user programmable 2049th word to be placed on the outputs independent of the system clock. This feature can be used to force an initialize word or provide a preset or clear function.

A further advantage of the WS57C45 over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This enables the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C45 RPROM in a windowed package is 100% tested with worst case test patterns both before and after assembly.

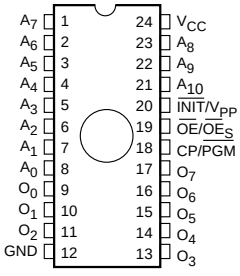
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP/Plastic DIP/ Flatpack



PRODUCT SELECTION GUIDE

PARAMETER	WS57C45-25	WS57C45-35	WS57C45-45
Set Up Time (Max)	25 ns	35 ns	45 ns
Clock to Output (Max)	12 ns	15 ns	25 ns

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ABSOLUTE MAXIMUM RATINGS*

Storage Temperature.....–65° to + 150°C
Voltage on any Pin with
Respect to Ground .....–0.6V to +7V
V_{PP} with Respect to Ground.....–0.6V to + 14V
ESD Protection.....>2000V

*NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 10%
Industrial	–40°C to +85°C	+5V ± 10%
Military	–55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	V_{CC} = 5.5 V, f = 0 MHz (Note 1), Output Not Loaded Add 2 mA/MHz for AC Operation	Comm'l		20	mA
			Industrial		30	mA
			Military		30	mA
I_{CC2}	V_{CC} Active Current (TTL)	V_{CC} = 5.5 V, f = 0 MHz (Note 1), Output Not Loaded Add 2 mA/MHz for AC Operation	Comm'l		25	mA
			Industrial		35	mA
			Military		35	mA
I_{LI}	Input Leakage Current	V_{IN} = 5.5V or Gnd		–10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		–10	10	µA

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \le 0.8V$, $V_{IH} \ge 2.0V$.
3. This parameter is only sampled and is not 100% tested.

CAPACITANCE(4)

SYMBOL	PARAMETER	CONDITIONS	MAX	UNITS
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0 V	5	pF
C_{OUT}	Output Capacitance		8	pF

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C45-25		WS57C45-35		WS57C45-45		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address Setup to Clock High	t_{SA}	25		35		45		ns
Address Hold From Clock High	t_{HA}	0		0		0		ns
Clock High to Valid Output	t_{CO}		12		15		25	ns
Clock Pulse Width	t_{PWC}	15		20		20		ns
$\overline{OE}_S$ Setup to Clock High	t_{SOE_S}	12		15		15		ns
$\overline{OE}_S$ Hold From Clock High	t_{HOE_S}	5		5		5		ns
Delay From INIT to Valid Output	t_{DI}		20		20		35	ns
$\overline{INIT}$ Recovery to Clock High	t_{RI}	15		20		20		ns
$\overline{INIT}$ Pulse Width	t_{PWI}	15		20		25		ns
Active Output From Clock High	t_{LZC}		15		20		30	ns
Inactive Output From Clock High	t_{HZC}		15		20		30	ns
Active Output From $\overline{OE}$ Low	t_{LZOE}		15		20		30	ns
Inactive Output From $\overline{OE}$ High	t_{HZOE}		15		20		30	ns

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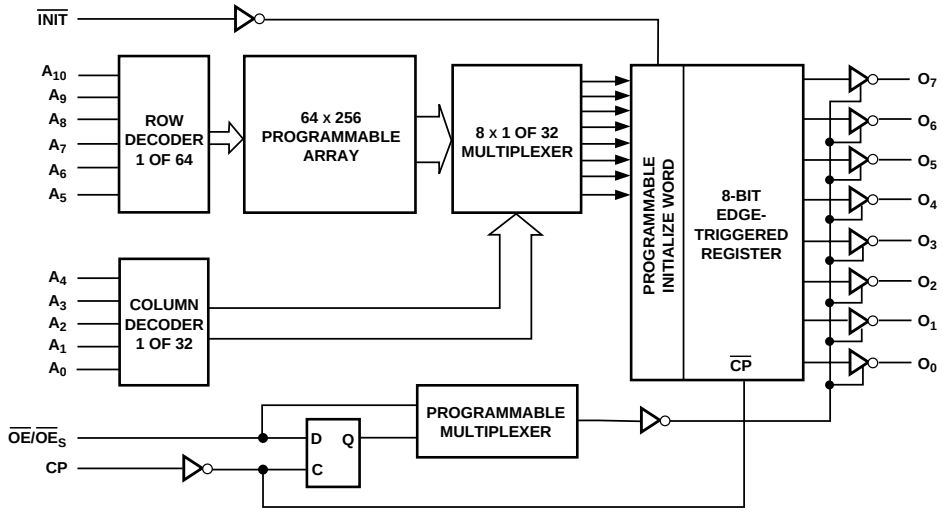
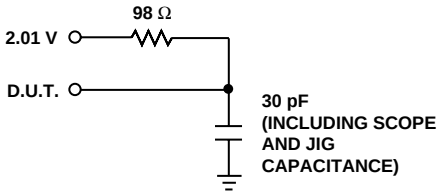
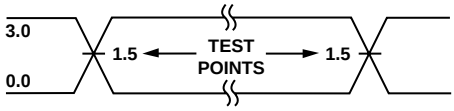
BLOCK DIAGRAM



TEST LOAD (High Impedance Test Systems)

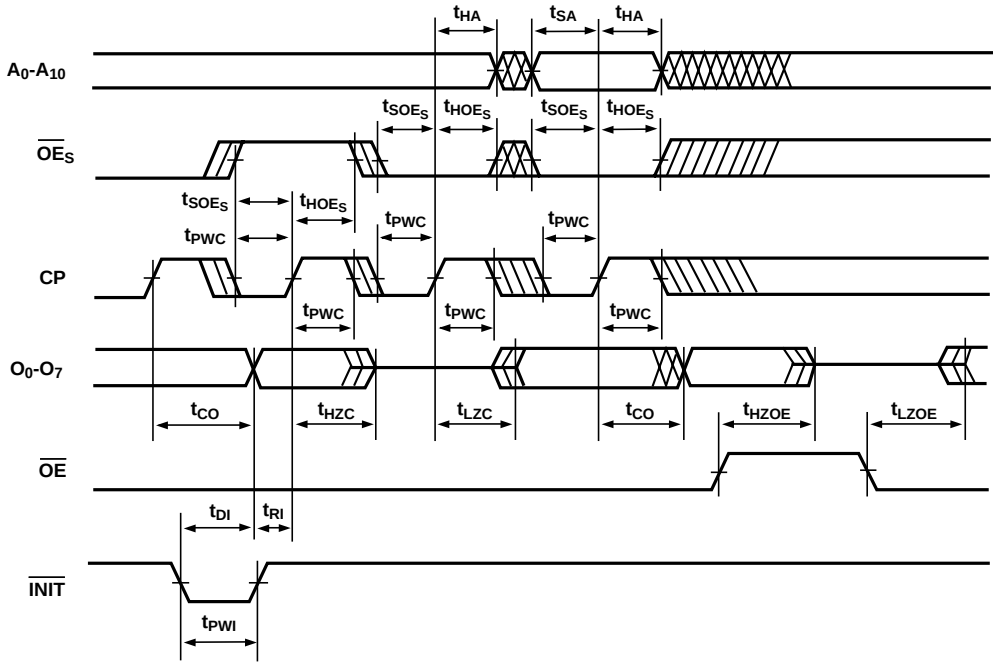


A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 3.0 V for a logic “1” and 0.0 V for a logic “0.” Timing measurements are made at 1.5 V for input and output transitions in both directions.

AC READ TIMING DIAGRAM



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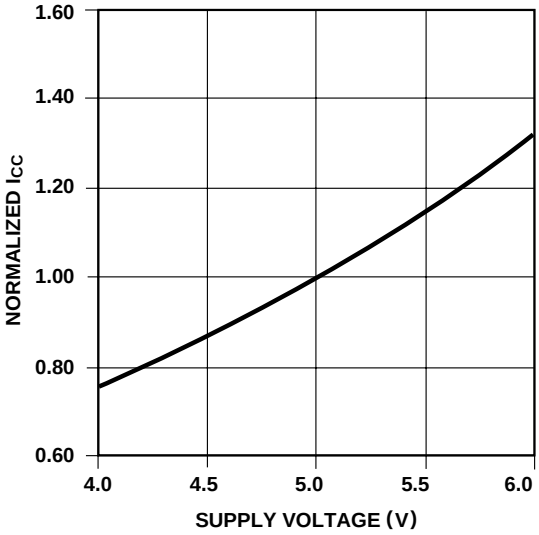
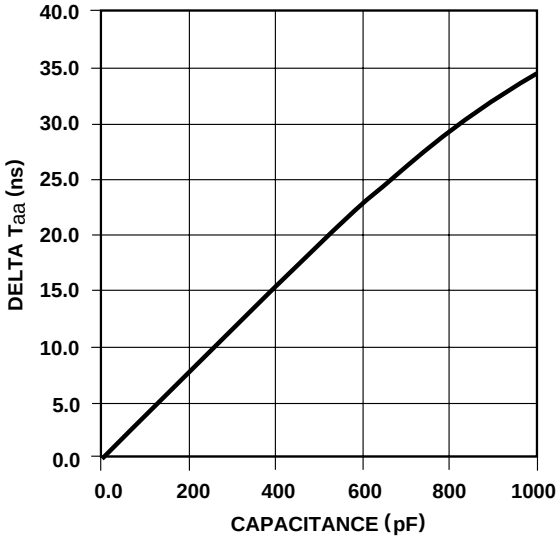
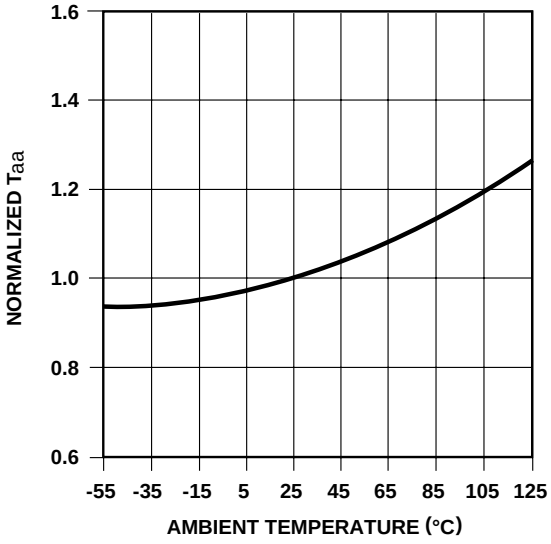
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



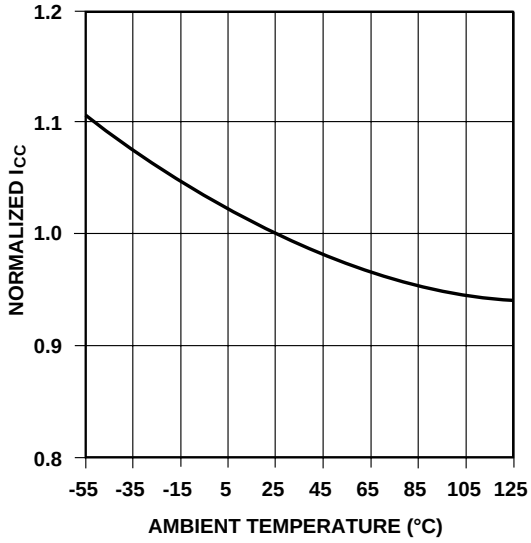
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED T_{aa} vs. AMBIENT TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



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FUNCTION DESCRIPTION

The WS57C45 is an electrically programmable read only memory produced with WSI's patented high-performance self-aligned split gate CMOS EPROM technology. It is organized as 2048 x 8 bits and is pin-for-pin compatible with bipolar TTL fuse link PROMs. The WS57C45 includes a D-type 8-bit data register on-chip which reduces the complexity and cost of microprogrammed pipelined systems where PROM data is held temporarily in a register. The circuit features a programmable synchronous ($\overline{OE}_S$) or asynchronous ($\overline{OE}$) output enable and asynchronous initialization ($\overline{INIT}$).

The programmed state of the enable pin ($\overline{OE}_S$ or $\overline{OE}$) will dictate the state of gthe outputs at power up. If $\overline{OE}_S$ has been programmed, the outputs will be in the OFF or high impedance state. If $\overline{OE}$ has been programmed, the outputs will be OFF or high impedance only if the $\overline{OE}$ input is HIGH. Data is read by applying the address to inputs $A_{10} - A_0$ and a LOW to the enable input. The data is retrieved and loaded into the master section of the 8-bit data register during the address set-up time. The data is transferred to the slave output of the data register at the next LOW to HIGH clock (CP) transition. Then the output buffers present the data on the outputs ($O_7 - O_0$).

When using the asynchronous enable ($\overline{OE}$), the output buffers may be disabled at any time by switching the enable input to a logic HIGH. They may be re-enabled by switching the enable to a logic LOW.

When using the sychronous enable ($\overline{OE}_S$), the outputs revert to a high impedance or OFF state at the next positive clock edge following the $\overline{OE}_S$ input transition to a HIGH state. The output will revert to the active state following a positive clock edge when the $\overline{OE}_S$ input is at a LOW state. The address and synchronous enable inputs are free to change following a positive clock edge since the output will not change until the next low to high clock transition. This enables accessing the next data location while previously addressed data is present on the outputs.

To avoid race conditions and simplify system timing, the 8-bit edge triggered data register clock is derived directly from the system clock.

The WS57C45 has an asynchronous initialize input ($\overline{INIT}$). This function can be used during power-up and time-out periods to implement functions such as a start address or initialized bus control word. The $\overline{INIT}$ input enables the contents of a 2049th 8-bit word to be loaded directly into the output data register. The INIT input can be used to load any 8-bit data pattern into the register since each bit is programmable by the user. When unprogrammed, activating $\overline{INIT}$ will result in clearing the register (outputs LOW). When all bits are programmed, actrivating $\overline{INIT}$ results in PRESETting the register (outputs HIGH).

When activated LOW, the $\overline{INIT}$ input results in an immediate load of the 2049th word into both the master and slave sections of the output register. This is independent of any other input including the clock (CP) input. The initialize data will be present at the outputs after the asynchronous enable ($\overline{OE}$) is taken to a LOW state.

Programming Information

Apply power to the WS57C45 for normal read mode operation with CP/$\overline{PGM}$, $\overline{OE}$/$\overline{OE}_S$ and $\overline{INIT}/V_{PP}$ at V_{IH}. Then take $\overline{INIT}/V_{PP}$ to V_{PP}. The part is then in the program inhibit mode operation and the output lines are in a high impedance state. Refer to Figure 5. As shown in Figure 5, address, program and verify one byte of data. Repeat this sequence for each location to be programmed.

When intelligent programming is used, the program pulse width is 1 ms in length. Each address location is programmed and verified until it verifies correctly up to and including 5 times. After the location verifies, an additional programming pulse should be applied that is X1 times in duration of the sum of the previous programming pulses before proceeding on to the next address and repeating the process.

Initialization Byte Programming

The WS57C45 has a 2049th byte of data that can be used to initialize the value of the data register. This byte contains the value "0" when it is shipped from the factory. The user must program the 2049th byte with a value other than "0" for data register initialization if that value is not desired. Except for the following details, the user may program the 2049th byte in the same manner as the other 2048 bytes. First, since all 2048 addresses are used up, a super voltage address feature is used to enable an additional address. The actual address includes V_{PP} on A_1 and V_{IL} on A_2. Refer to the Mode Selection table. The programming and verification of the Initial Byte is accomplished operationally by performing an initialize function.

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Synchronous Enable Programming

The WS57C45 contains both a synchronous and asynchronous enable feature. The part is delivered configured in the asynchronous mode and only requires alteration if the synchronous mode is required. This is accomplished by programming an on-chip EPROM cell. Similar to the Initial Byte, this function is enabled and addressed by using a super voltage. Referring to the Mode Selection table, V_{PP} is applied to A_1 followed by V_{IH} applied to A_2. This procedure addresses the EPROM cell that programs the synchronous enable feature. The EPROM cell is programmed with a 10 ms program pulse on CP/$\overline{PGM}$. It does not require any data since there is no selection as to how synchronous enable may be programmed, only if it is to be programmed.

Synchronous Enable Verification

The WS57C45's synchronous enable function is verified operationally. Apply power for read operation with $\overline{OE}/\overline{OE}_S$ and $\overline{INIT}/V_{PP}$ at V_{IH} and take the clock (CP/$\overline{PGM}$) from V_{IL} to V_{IH}. The output data bus should be in a high impedance state. Next take $\overline{OE}/\overline{OE}_S$ to V_{IL}. The outputs will remain in the high impedance state. Take the clock (CP/$\overline{PGM}$) from V_{IL} to V_{IH} and the outputs will now contain the data that is present. Take $\overline{OE}/\overline{OE}_S$ to V_{IH}. The output should remain driven. Clocking CP/$\overline{PGM}$ once more from V_{IL} to V_{IH} should place the outputs again in a high impedance state.

Blank Check

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C45 has all 2048 bytes in the '0' state. "1's" are loaded into the WS57C45 through the procedure of programming.

MODE		PIN FUNCTION					OUTPUTS
	READ OR OUTPUT DISABLE	A_2	CP/$\overline{PGM}$	($\overline{OE}/\overline{OE}_S$)/$\overline{VFY}$	$\overline{INIT}/V_{PP}$	A_1	
Read (Note 6)		X	X	V_{IL}	V_{IH}	X	Data Out
Output Disable		X	X	V_{IH}	V_{IH}	X	High Z
Program (Notes 5 & 7)		X	V_{IL}	V_{IH}	V_{PP}	X	Data In
Program Verify (Notes 5 & 7)		X	V_{IH}	V_{IL}	V_{PP}	X	Data Out
Program Inhibit (Notes 5 & 7)		X	V_{IH}	V_{IH}	V_{PP}	X	High Z
Intelligent Program (Notes 5 & 7)		X	V_{IL}	V_{IH}	V_{PP}	X	Data In
Program Synch Enable (Note 7)		V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{PP}	High Z
Program Initial Byte (Note 7)		V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{PP}	Data In
Initial Byte Read		X	X	V_{IL}	V_{IL}	X	Data Out

NOTES: 5. X = Don't Care but not to exceed V_{PP}.
6. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
7. During programming and verification, all unspecified pins to be at V_{IL}.

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FIGURE 5. PROM PROGRAMMING WAVEFORMS

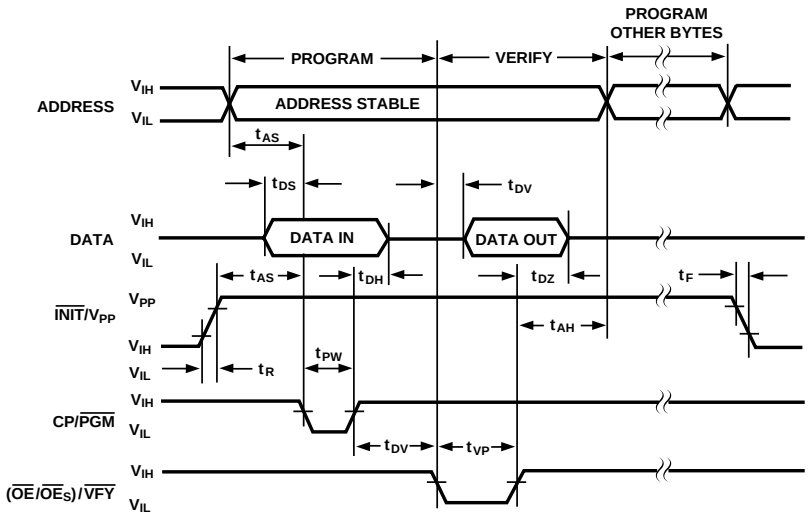


FIGURE 6. INITIAL BYTE PROGRAMMING WAVEFORMS

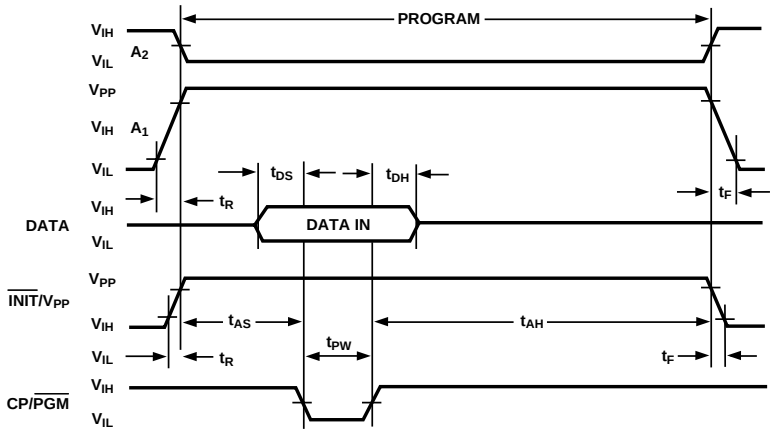
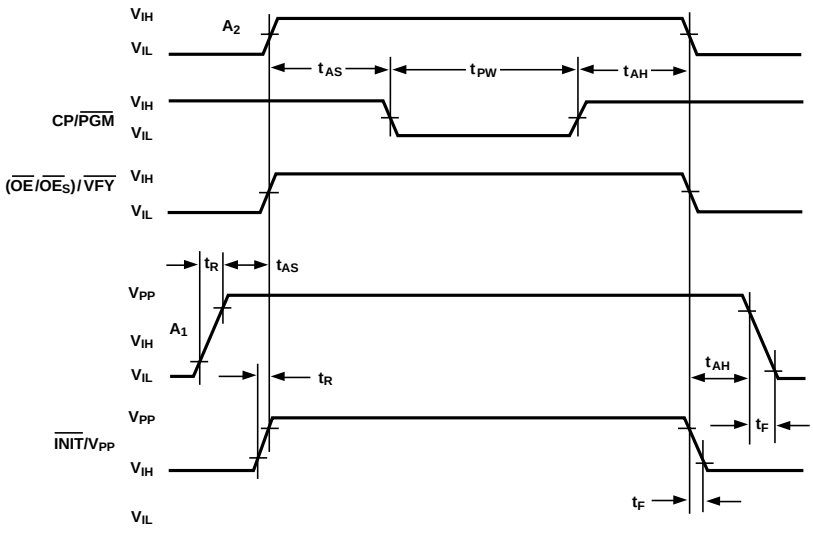


FIGURE 7. PROGRAM SYNCHRONOUS ENABLE



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PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6 V ± 0.25 V, V_{PP} = 13.5 ± 0.5 V)

SYMBOLS	PARAMETER	MIN	MAX	UNITS
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse		60	mA
I_{CC}	V_{CC} Supply Current		25	mA
V_{IL}	Input Low Voltage	–0.1	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = –4 mA)	2.4		V

NOTE: 8. V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6 V ± 0.25 V, V_{PP} = 13.5 ± 0.5 V)

SYMBOLS	PARAMETER	MIN	MAX	UNITS
t_{PW}	Programming Pulse Width	0.1	10	ms
t_{AS}	Address Setup Time	1.0		µs
t_{DS}	Data Setup Time	1.0		µs
t_{AH}	Address Hold Time	1.0		µs
t_{DH}	Data Hold Time	1.0		µs
t_R, t_F	V_{PP} Rise and Fall Time	1.0		µs
t_{VD}	Delay to $\overline{VFY}$	1.0		µs
t_{VP}	$\overline{VFY}$ Pulse Width	2.0		µs
t_{DV}	$\overline{VFY}$ Data Valid		1.0	µs
t_{DZ}	$\overline{VFY}$ HIGH to High Z		1.0	µs

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ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C45-25T	25	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C45-35KMB*	35	24 Pin CERDIP, 0.3"	K1	Military	MIL-STD-883C
WS57C45-35S	35	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C45-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C45-35TMB*	35	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C45-45KMB*	45	24 Pin CERDIP, 0.3"	K1	Military	MIL-STD-883C
WS57C45-45TMB*	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

NOTE: The actual part marking will not include the initials "WS."

*SMD product. See section 4 for DESC SMD numbers.

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS57C45 is programmed using Algorithm A shown on page 5-3.

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