

## 54F/74F398 • 54F/74F399 Quad 2-Port Register

### General Description

The 'F398 and 'F399 are the logical equivalents of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. The 'F399 is the 16-pin version of the 'F398, with only the Q outputs of the flip-flops available.

### Features

- Select inputs from two data sources
- Fully positive edge-triggered operation
- Both true and complement outputs—'F398
- Guaranteed 4000V minimum ESD protection—'F399

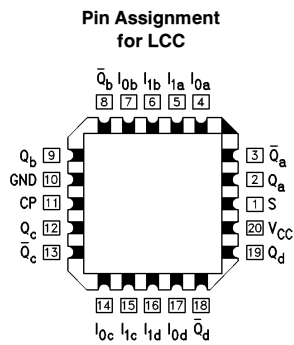
Commercial	Military	Package Number	Package Description
74F398PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F398DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F398SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
	54F398FM (Note 2)	W20A	20-Lead Cerpack
	54F398LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C
74F399PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F399DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F399SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F399SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F399FM (Note 2)	W20A	20-Lead Cerpack
	54F399LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

**Note 1:** Devices also available in 13" reel. Use suffix = SCX and SJX.

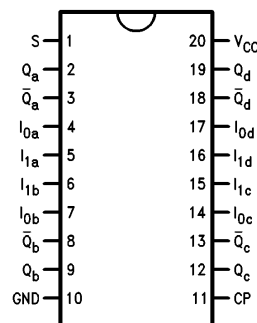
**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

### Connection Diagrams

'F398



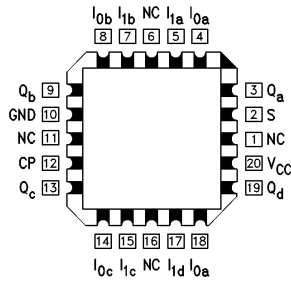
**Pin Assignment for DIP, SOIC and Flatpak**



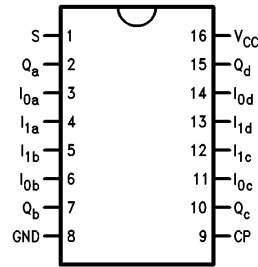
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## Connection Diagrams (Continued)

'F399

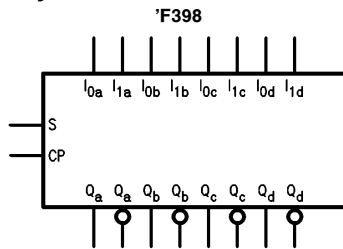


TL/F/9533-7

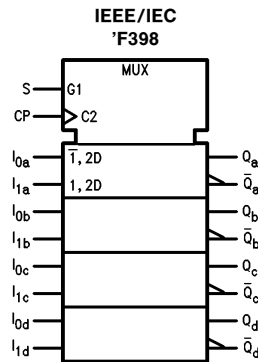


TL/F/9533-8

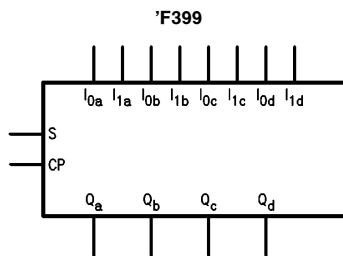
## Logic Symbols



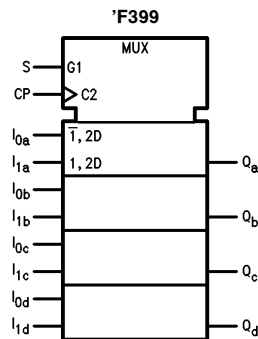
TL/F/9533-2



TL/F/9533-1



TL/F/9533-4



TL/F/9533-3

## Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
S	Common Select Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$I_{0a}-I_{0d}$	Data Inputs from Source 0	1.0/1.0	20 $\mu$ A/ -0.6 mA
$I_{1a}-I_{1d}$	Data Inputs from Source 1	1.0/1.0	20 $\mu$ A/ -0.6 mA
$Q_a-Q_d$	Register True Outputs	50/33.3	-1 mA/20 mA
$\bar{Q}_a-\bar{Q}_d$	Register Complementary Outputs ('F398)	50/33.3	-1 mA/20 mA

## Functional Description

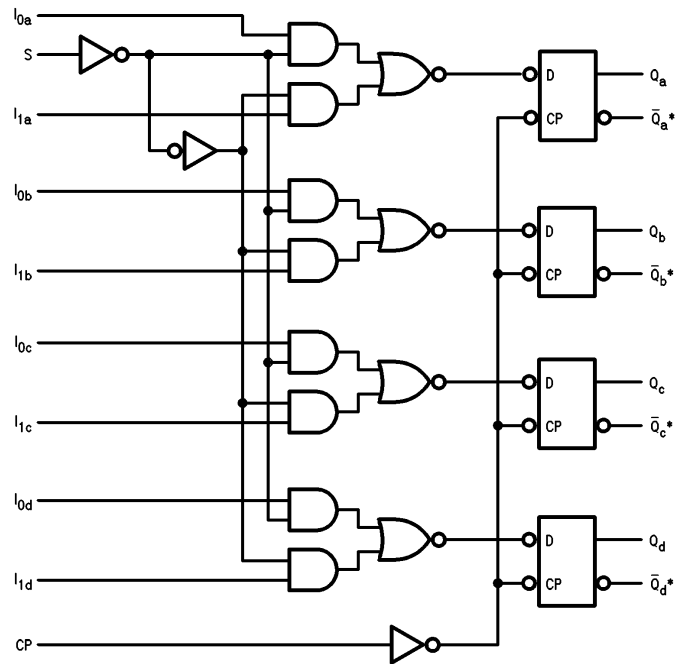
The 'F398 and 'F399 are high-speed quad 2-port registers. They select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs ( $I_{0x}$ ,  $I_{1x}$ ) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The 'F398 has both Q and  $\bar{Q}$  outputs.

Function Table

Inputs			Outputs	
S	$I_0$	$I_1$	Q	$\bar{Q}^*$
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition  
 l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition  
 X = Immaterial  
 \*'F398 only

## Logic Diagram



TL/F/9533-9

\*\*F398 Only

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +175°C
Plastic	–55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	–0.5V to V <sub>CC</sub>
TRI-STATE® Output	–0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

ESD Last Passing Voltage (Min)—F399 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	–55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage	0.8			V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage	–1.2			V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = –1 mA I <sub>OH</sub> = –1 mA I <sub>OH</sub> = –1 mA
		74F 10% V <sub>CC</sub>	2.5				
		74F 5% V <sub>CC</sub>	2.7				
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			–0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		–60	–150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current (F398)		25	38	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current (F398)		25	38	mA	Max	V <sub>O</sub> = LOW
I <sub>CCH</sub>	Power Supply Current (F399)		22	34	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current (F399)		22	34	mA	Max	V <sub>O</sub> = LOW

## AC Electrical Characteristics

Symbol	Parameter	74F			54F		74F		Units	
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f <sub>max</sub>	Input Clock Frequency	100	140		80		100		MHz	
t <sub>PLH</sub> t <sub>pHL</sub>	Propagation Delay CP to Q or $\bar{Q}$	3.0*	5.7	7.5	3.0	9.5	3.0	8.5	10.0	ns

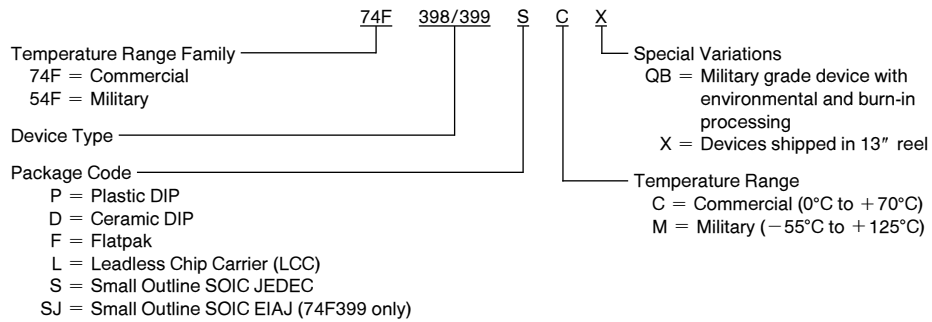
\*F398 3.3 ns

## AC Operating Requirements

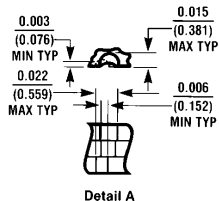
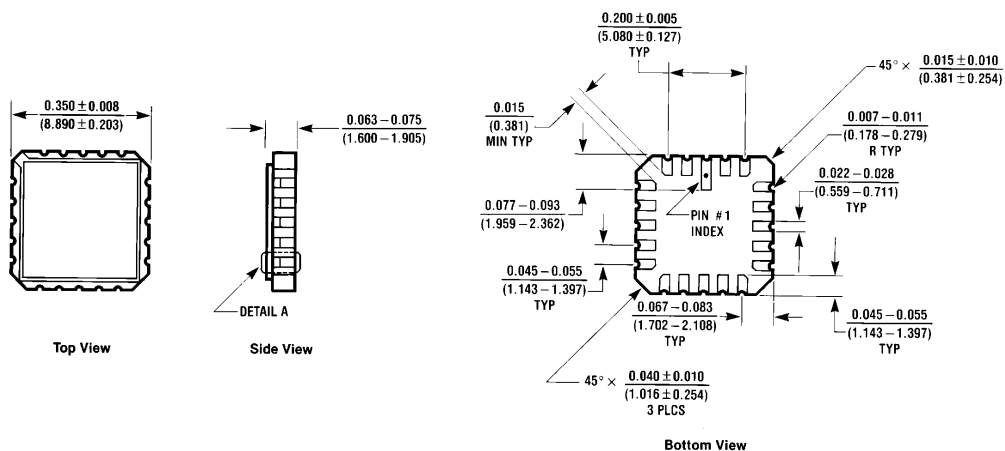
Symbol	Parameter	74F		54F		74F		Units
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com		
		Min	Max	Min	Max	Min	Max	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW I <sub>n</sub> to CP	3.0		4.5		3.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW I <sub>n</sub> to CP	1.0		1.5		1.0		
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW S to CP (*F398)	7.5		10.5		8.5		ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW S to CP (*F399)	7.5		9.5		8.5		
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW S to CP	0		0		0		ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP Pulse Width HIGH or LOW	4.0		4.0		4.0		
		5.0		7.0		5.0		

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

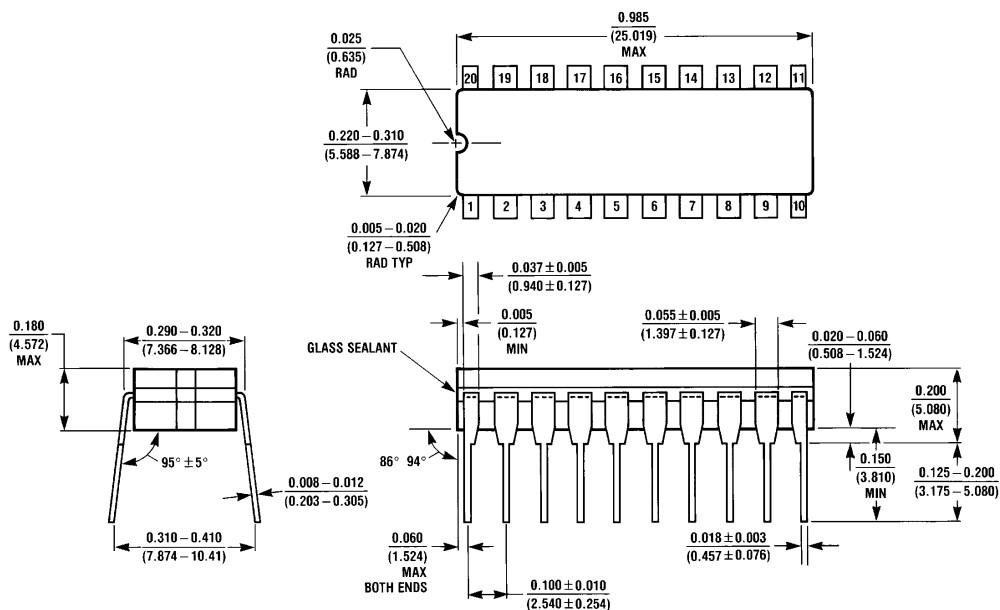


# Physical Dimensions inches (millimeters)



**20-Lead Ceramic Leadless Chip Carrier (L)**  
 NS Package Number E20A

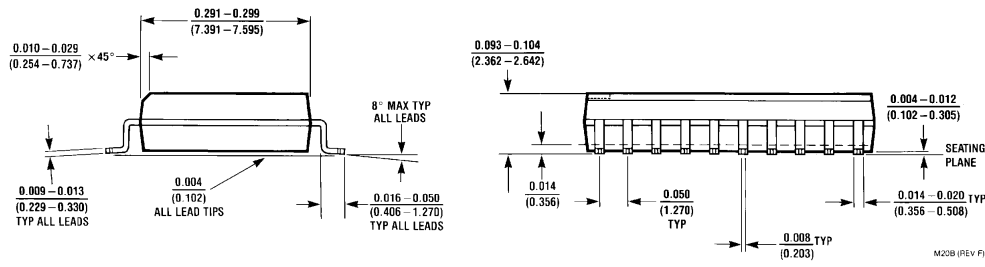
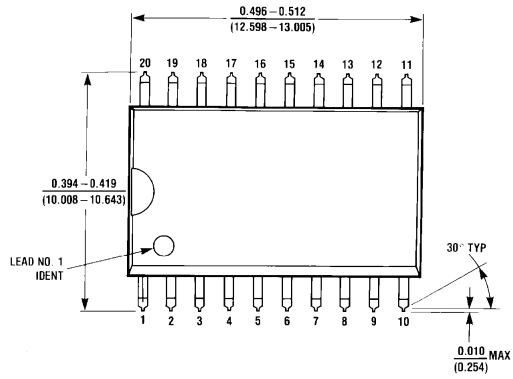
E20A (REV D)



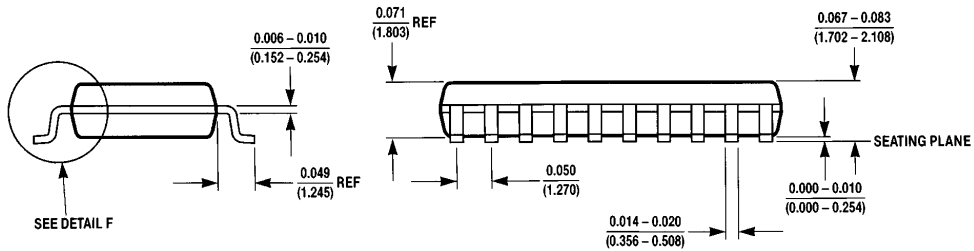
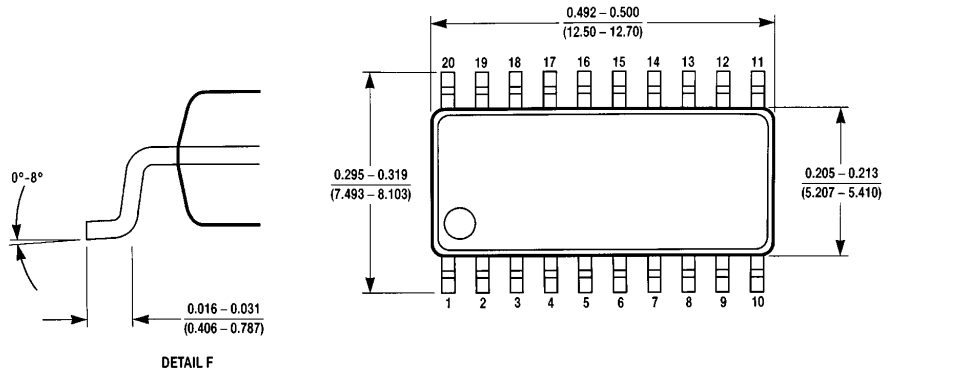
**20-Lead Ceramic Dual-In-Line Package (D)**  
 NS Package Number J20A

J20A (REV M)

**Physical Dimensions** inches (millimeters) (Continued)



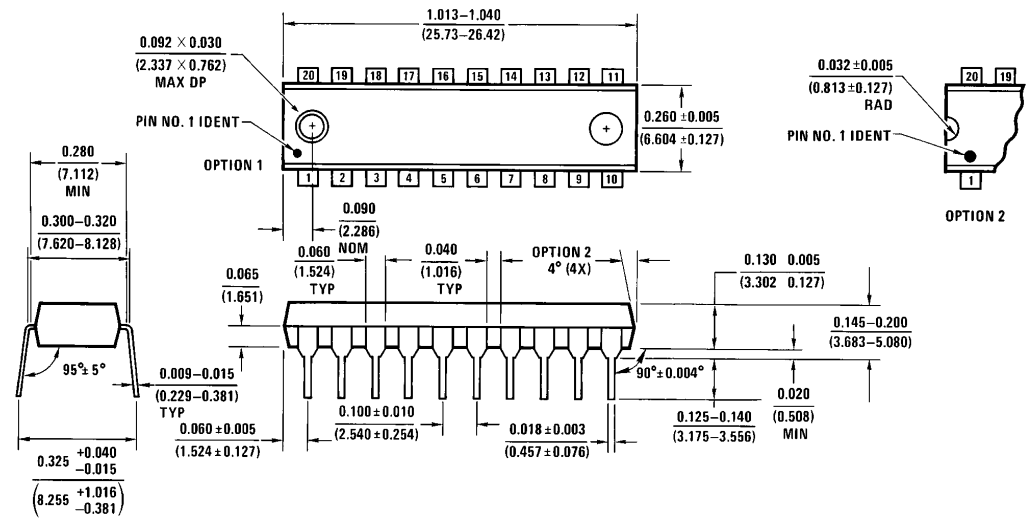
**20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)  
NS Package Number M20B**



**20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)  
NS Package Number M20D**



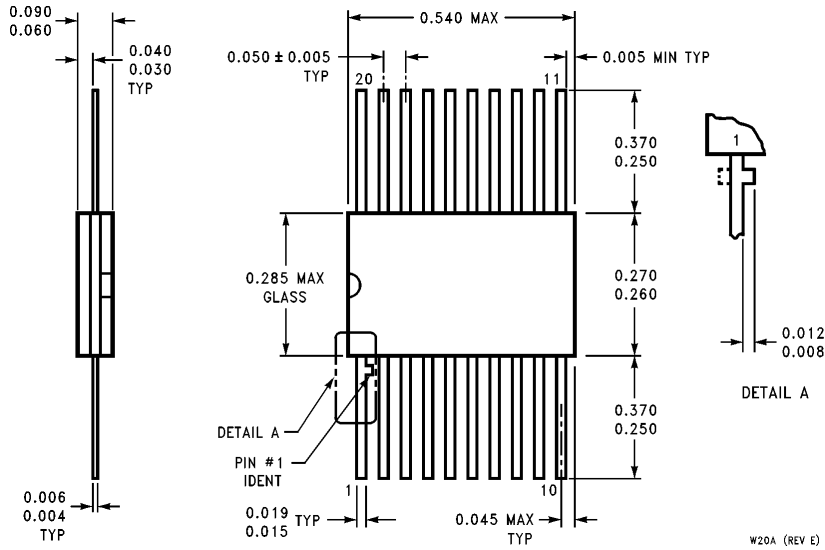
**Physical Dimensions** inches (millimeters) (Continued)



**20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)**  
**NS Package Number N20A**

N20A (REV G)

**Physical Dimensions** inches (millimeters) (Continued)



**20-Lead Ceramic Flatpak (F)  
NS Package Number W20A**

W20A (REV E)

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