3.3V CMOS 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

IDT74ALVC162831

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.40mm pitch TVSOP package
- Extended commercial range of – 40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range
- V_{CC} = 2.7V to 3.6V, Extended Range
- V_{CC} = 2.5V ±0.2V
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVC162831:

- Balanced Output Drivers: ±12mA
- Low switching noise

APPLICATIONS:

- Memory subsystems
- PC motherboards and servers
- Workstations
- Telecommunication applications

DESCRIPTION:

This 1-bit to 4-bit address register/driver is built using advanced dual metal CMOS technology. This device is ideal for use in applications in which a single address bus is driving four separate memory locations. The ALVC162831 can be used as a buffer or a register, depending on the logic level of the select ($\overline{SEL}$) input.

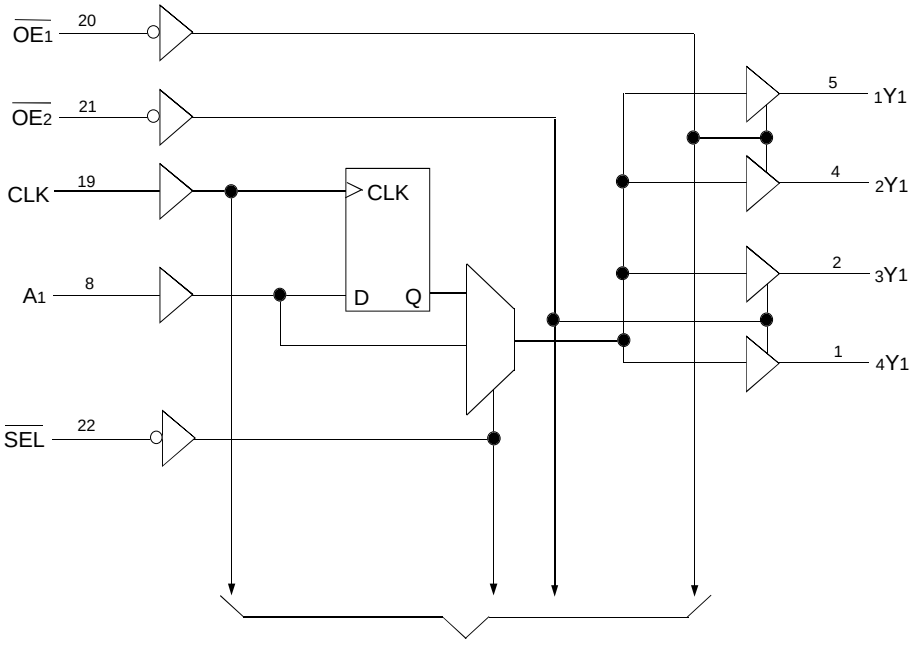
When $\overline{SEL}$ is logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output-enable ($\overline{OE}$) controls. Each $\overline{OE}$ controls two groups of nine outputs. When $\overline{SEL}$ is logic low, the device is in the register mode. The register is an edge-triggered D-type flip-flop. On the positive transition of the clock (CLK) input, data set up at the A inputs is stored in the internal registers. $\overline{OE}$ controls operate the same as in buffer mode.

When $\overline{OE}$ is logic low, the outputs are in a normal logic state (high or low logic level). When $\overline{OE}$ is logic high, the outputs are in a high-impedance state.

$\overline{SEL}$ and $\overline{OE}$ do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The ALVC162831 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive ±12mA at the designated threshold levels.

FUNCTIONAL BLOCK DIAGRAM



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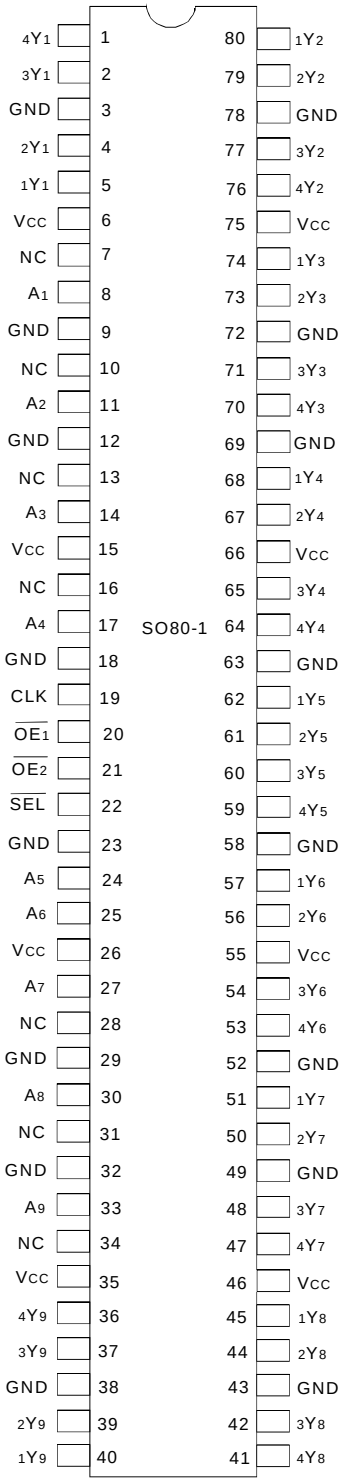
PIN CONFIGURATION



TVSOP TOP VIEW

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	– 0.5 to + 4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	– 0.5 to V_{CC} + 0.5	V
T_{STG}	Storage Temperature	– 65 to + 150	°C
I_{OUT}	DC Output Current	– 50 to + 50	mA
I_{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	± 50	mA
I_{OK}	Continuous Clamp Current, $V_O < 0$	– 50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	9	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	7	9	pF

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NOTE:
1. As applicable to the device type.

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PIN DESCRIPTION

Pin Names	Description
$\overline{OEx}$	3-State Output Enable Inputs (Active LOW)
CLK	Register Input Clock
$\overline{SEL}$	Select Input
Ax	Data Inputs
xYx	3-State Outputs
NC	No Internal Connection

FUNCTION TABLE (1)

Inputs				Outputs
$\overline{OEx}$	$\overline{SEL}$	CLK	Ax	xYx
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
   Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = – 40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	V_{CC} = 3.6V	V_I = V_{CC}	—	—	± 5	µA
I_{IL}	Input LOW Current	V_{CC} = 3.6V	V_I = GND	—	—	± 5	
I_{OZH}	High Impedance Output Current	V_{CC} = 3.6V	V_O = V_{CC}	—	—	± 10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	± 10	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V V_{IN} = GND or V_{CC}		—	0.1	40	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} – 0.6V, other inputs at V_{CC} or GND		—	—	750	µA

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NOTE:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

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OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 4mA	1.9	—	
			I_{OH} = – 6mA	1.7	—	
		V_{CC} = 2.7V	I_{OH} = – 4mA	2.2	—	
			I_{OH} = – 8mA	2	—	
		V_{CC} = 3.0V	I_{OH} = – 6mA	2.4	—	
			I_{OH} = – 12mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 4mA	—	0.4	
			I_{OL} = 6mA	—	0.55	
		V_{CC} = 2.7V	I_{OL} = 4mA	—	0.4	
			I_{OL} = 8mA	—	0.6	
		V_{CC} = 3.0V	I_{OL} = 6mA	—	0.55	
			I_{OL} = 12mA	—	0.8	

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NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V_{CC} = 2.5V ± 0.2V	V_{CC} = 3.3V ± 0.3V	Unit
			Typical	Typical	
C_{PD}	Power Dissipation Capacitance Outputs enabled	C_L = 0pF, f = 10Mhz	119	132	pF
C_{PD}	Power Dissipation Capacitance Outputs disabled		22	25	pF

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SWITCHING CHARACTERISTICS(1)

Symbol	Parameter	Vcc = 2.5V ± 0.2V		Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}		150	—	150	—	150	—	MHz
t_{PLH} t_{PHL}	Propagation Delay Ax to xYx	1.1	4.7		4.8	1.5	4.3	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{SEL}$ to xYx	1.1	6		6.2	1.5	4.8	ns
t_{PLH} t_{PHL}	Propagation Delay CLK to xYx	1	5.3		5.3	1.4	4.7	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$x to xYx	1	5.9		5.9	1.1	5.1	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$x to xYx	1	5.4		5.4	1.6	5.1	ns
t_W	Pulse Duration, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t_{SU}	Setup Time, Ax data before CLK↑	2	—	2	—	1.6	—	ns
t_H	Hold Time, Ax data after CLK↑	0.7	—	0.5	—	1.1	—	ns
$t_{SK(o)}$	Output Skew(2)	—	—	—	—	—	500	ps

NOTES:
1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

SWITCHING CHARACTERISTICS FROM, 0°C TO 65°C, C_L = 5pF

Symbol	Parameter	Vcc = 3.3V ± 0.15V		Unit
		Min.	Min.	
t_{PLH} t_{PHL}	Propagation Delay CLK to xYx	1.9	4.5	ns

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TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 3.3V±0.3V	$V_{CC}^{(1)}$= 2.7V	$V_{CC}^{(2)}$= 2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

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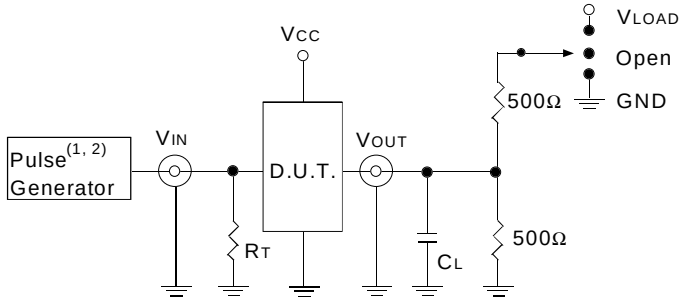
TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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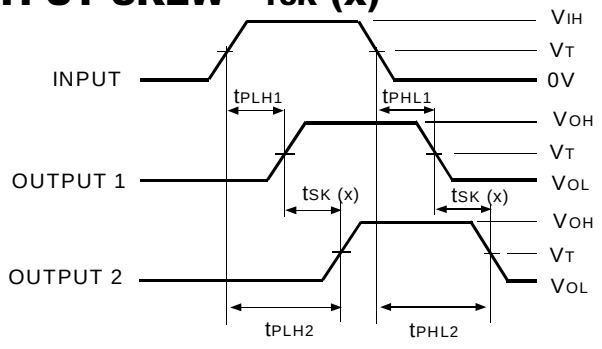
OUTPUT SKEW - t_{SK} (x)



$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

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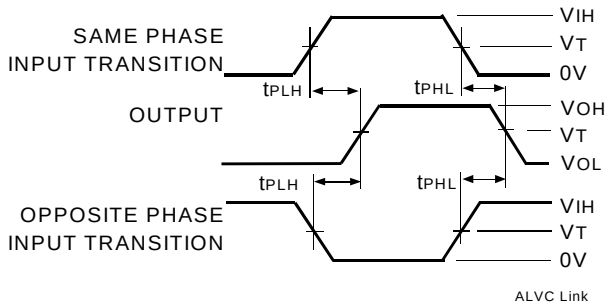
NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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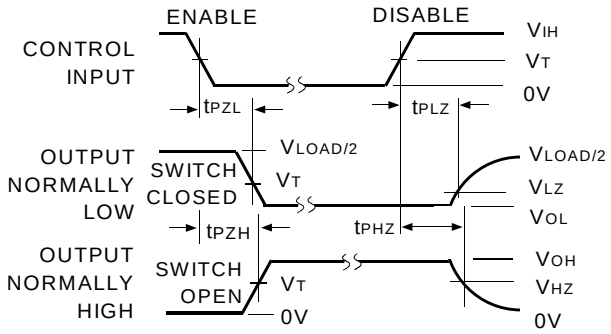
ENABLE AND DISABLE TIMES



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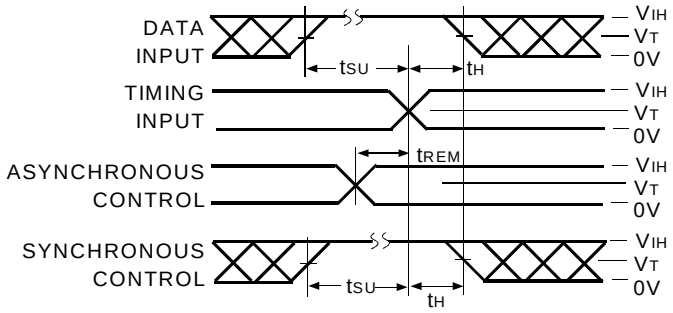
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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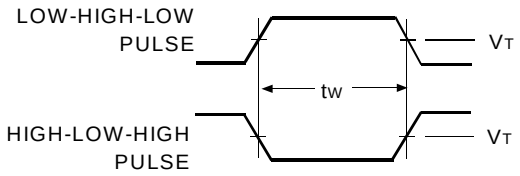
PULSE WIDTH



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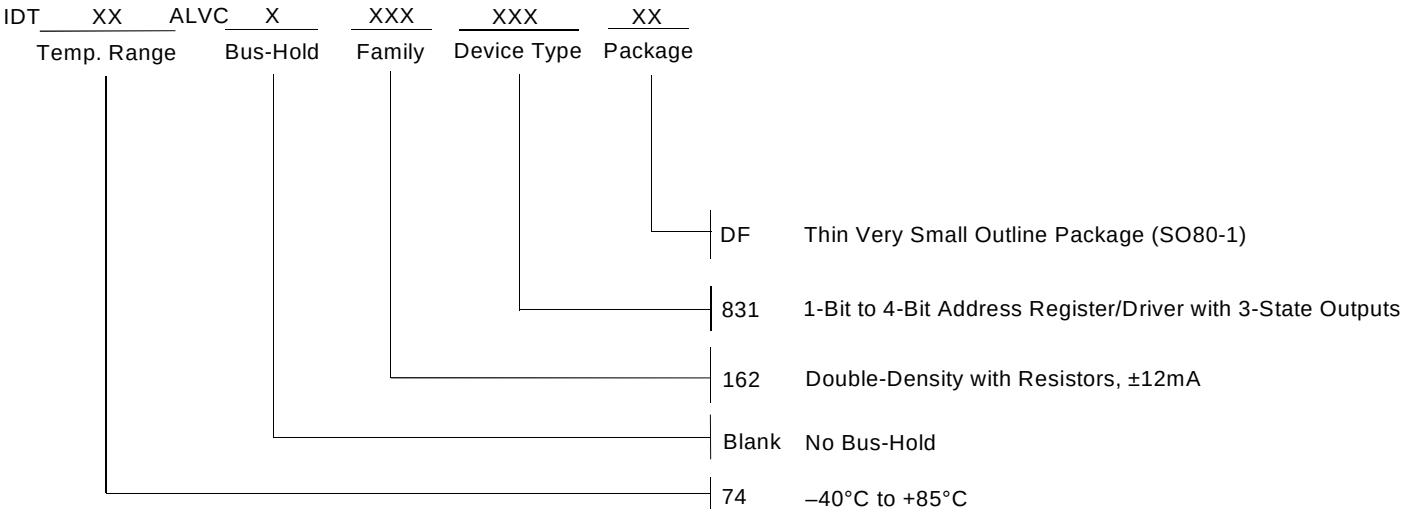
ORDERING INFORMATION



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